ULTRA THIN BODY 22nm SOI N-MOSFET (The Effect of Sidewall Spacer Oxide Thickness to the Device Performance)

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JUNE 2017

DECLARATION

"I hereby declare that this report is the result of my own work except for quotes as cited in the references."

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DECLARATION

"I hereby declare that I have read this thesis and in my opinion this report is sufficient in terms of the scope and quality for the award of Bachelor Degree of Electronic Engineering (Industrial Electronic)

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Dedicated to my beloved mother and father, my siblings and my colleagues who had been support me to complete this project.

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ABSTRACT

Currently, Ultra-Thin Body (UTB) fully depleted (FD) silicon-on-insulator (SOI) MOSFETs were of much interest because of advantageous features such as near-ideal gate swing and high drive current. This project is to investigate Ultra-Thin Body the effect of sidewall spacer oxide thickness to improve device performance. 4nm, 5nm, 6nm, 7nm, and 8nm are the different sidewall spacer oxide thickness that has been used in this research. The differences sidewall spacer oxide thickness does have a effect in the device performance. The tools utilize is Technology Computer Aided Design (TCAD). In TCAD software , silvaco's deckbuild ATHENA and ATLAS were used to design the physical structure of ultra-thin body hence obtaining its characteristics. The design structure will be go through a step by step fabrication process which parameter and value are stated in International Technology Roadmap for Semiconductor (ITRS). Then I-V characteristics of the UTB can be analyse by using ATLAS to show the particular performance of current device created.

ABSTRAK

Pada masa kini, *Ultra Thin Body Silicon On Insulator* (UTB SOI) untuk *Fully Depleted* (FD) MOSFET mempunyai banyak ciri-ciri yang menarik dan berfaedah seperti, hampir *ideal gate swing* dan keadaan elektrik *Ion* yang tinggi . Projek ini adalah untuk mengkaji *Ultra Thin Body MOSFET* bagi meningkatkan prestasi peranti. 4nm, 5nm, 6nm, 7nm, and 8nm ialah perbezaan *Sidewall Spacer Oxide Thickness* yang digunakan untuk kajian ini. Dengan menggunakan *Sidewall Spacer Oxide Thickness* yang berbeza memberikan impak kepada peranti. Perisian yang digunakan untuk membuat projek ini adalah Technology Computer Aided Design (TCAD). Dalam perisian TCAD, terdapat SILVACO ATHENA dan ATLAS yang telah digunakan untuk mereka bentuk struktur fizikal *Ultra Thin Body* dan sekaligus memperolehi ciri-ciri struktur yg dingini. Struktur reka bentuk akan dilakukan secara beperingkat di dalam proses fabrikasi dengan merujuk nilai yang dinyatakan dalam *International Technology Roadmap for Semiconductor* (ITRS). Seterusnya ciri-ciri I-V UTB boleh dianalisis dengan menggunakan ATLAS untuk menunjukkan prestasi tertentu dalam peranti yang direka.

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LIST OF ABBREVIATIONS

UTB	-	Ultra-Thin Body
IC	-	Integrated Circuit
nm	-	Nano meter
SOI	-	Silicon On Insulator
FD	-	Fully Depleted
PD	-	Partially Depleted
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-Channel MOSFET
SS	-	Sub-Threshold Slope
DIBL	-	Drain-Induced Barrier Lowering
Si	-	Silicon
BOX	-	Buried Oxide
TCAD	-	Technology Computer Aided Design
2D	-	Two Dimension
AC	-	Alternating Current
DC	-	Direct Current
ITRS	-	International Technology Roadmap Semiconductor

LIST OF SYMBOLS

VTH	-	Threshold Voltage
VGS	-	Gate-To-Source Voltage
LG	-	Gate Length
TSI	-	Junction Depth
ID	-	Drain Current
VD	-	Drain Voltage
ION	-	Drive Current
IOFF	-	Leakage Current
SS	-	Sub-Threshold Voltage
EOT	-	Equivalent Oxide Thickness

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CHAPTER I

INTRODUCTION

1.0 Introduction

Ultra-Thin Body Silicon On Insulator (UTB SOI MOSFET) is a semiconductor device that provide a better performance and flexibility compare to any other conventional MOSFET .This research is to study on Ultra-Thin Body Silicon On Insulator (UTB SOI) which the structure in fully depleted.. Silicon on insulator (SOI) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance.

In this research Fully Depleted Ultra-Thin Body Silicon on Insulator (FD UTB SOI) are used because it has many advantages compare to other conventional MOSFET. FDSOI devices has a very thin film so the less depletion charges happens consequential in higher switching speeds. For the structure this device using titanium as a metal gate as it have better electrical characteristics gate compare to previous gate [5]. Furthermore when adding a buried oxide through the structure of Ultra-Thin Body the junction capacitance slightly reduce which may result in faster switching. Then the gate are stake up by a layer of silicon dioxide. The study is extend to the effect of sidewall spacer oxide thickness variation to see the

performance of the device. The tools utilize 22nm N-MOSFET will be simulate by silvaco and t-cad simulator and i-v characteristics obtain by using atlas software.

Silvaco is one of the device simulator which allow method of fabrication, and simulation for semiconductor devices. For this research Athena and Atlas is used. Athena is a general purpose 1D, 2D process simulator for applications including Etching and Deposition, Implantation, Annealing, and Stress simulation. While Atlas is a 2D and 3D device simulator that performs DC, AC, and transient analysis for silicon, binary, ternary, and quaternary material-based devices.

1.1 Objective

The objectives of this project are:

- To design the UTB 22nm SOI MOSFET with the optimum performance in regarding to drive current, gate leakage and voltage threshold .
- To analyze IV characteristic due to sidewall spacer oxide thickness variation
- To examine a comprehensive simulation study of fully depleted ultra-thin body silicon on insulator (FD-UTB SOI) at nanometer regime.

1.2 Problem Statement

- Sidewall spacer oxide thickness in 'ON' or 'OFF' state current one of the concern that affect the performance of the device.
- UTB SOI is design to eliminate gate leakage problem which drain lot of current in electronic devices.

1.3 Scope of Project

- Focus on UTB 22nm SOI MOSFET.
- Utilize T-cad and Silvaco simulation tool use to obtain I-V characteristic such as voltage threshold, drive current and gate leakage.

1.4 Importance Of The Project

- To improve the experimental results already attained by engineers, and to propose new areas for development.
- UTB can be used in microelectronics industry and high performance radio frequency application such as satellite .
- UTB also making industry to create tiny integrated circuit but with variable functions
- Giving reliable performance and flexibility compare to other MOSFET

1.5 Project Outline

In chapter 1, overall idea of what this project about but in summary. It consist of introduction elements such as objective, problem statement, scope and important of the project.

For chapter 2, it is to define each of the key terns including definition and terminology that are related to the topic. All case studies and facts are collected to support the evidence of the research

Next, chapter 3 will describe project flow from the beginning of the research until end. It specify what tools or software that need to be utilize in order to get structure and characteristics result.

In chapter 4, discussion about five different sidewall spacer oxide thickness is made which is 4nm, 5nm, 6nm, 7nm and 8nm. Then each sidewall spacer oxide thickness give it different I-V analysis which then will be discuss further.

Lastly for chapter 5, based on the result obtained in chapter 4 comparison is made to see if objective in chapter 1 is achieve. A few recommendation is stated for better improvement in future research.

CHAPTER II

LITERATURE REVIEW

2.0 Introduction

To even start the project, the basic ideas of how this project were conduct with referring to previous study in detail. The literature review consist of concept and ideas about the overall of the project.

2.1 Background Studies

2.1.1 Fully Depleted Silicon-On-Insulator (FD-SOI)

Fully Depleted Silicon on Insulator (FD-SOI) technology depend on an ultra-thin layer of silicon over a Buried Oxide (commonly called BOx) as shown in figure 2.1. Transistors fabricated into this top silicon layer are Ultra-Thin Body devices and have distinctive, extremely attractive characteristics. Two flavour of buried oxide can be used: standard thickness (typically 145nm thick as classically in volume production PD-SOI digital chips today), or ultra-thin BOx, for example 10 or 25nm (UTBOx, Ultra-Thin Buried Oxide) [1].

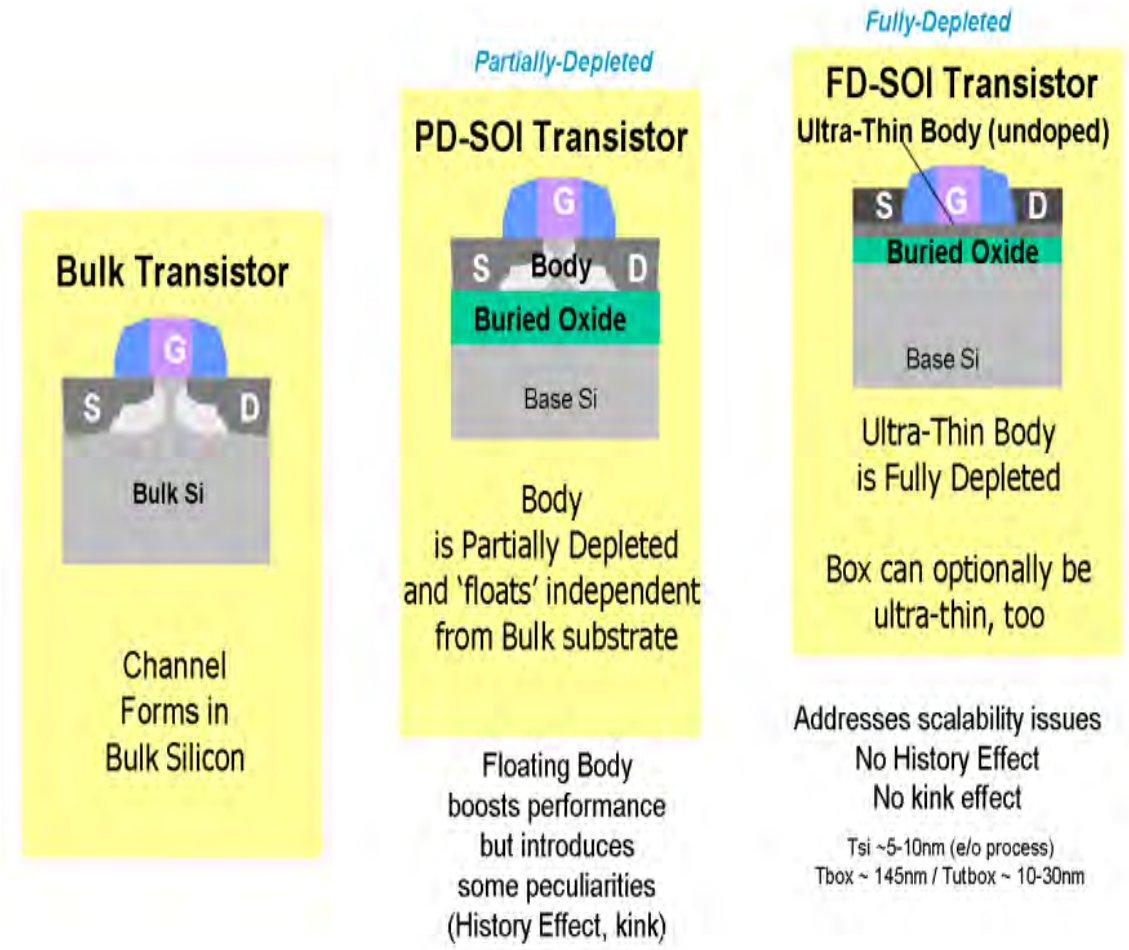

Figure 2.1: ***FD-SOI Transistors vs. Bulk and PD-SOI Transistors***

Ultra thin body (UTB) SOI devices are in between the utmost promising candidates for MOSFET in nano scale regime . These devices can work in Fully Depleted (FD) regime and thus decrease short channel effects, leakage current and uphold good scaling capability. Figure 2.2 shows structures offer to decrease parasitic capacitance and eradicate latch up. However due to the presence of a buried silicon dioxide layer, these devices suffer from self-heating . This is due to the fact that the thermal conductivity of silicon-dioxide (SiO2) is smaller than that of silicon. In addition, use of ultra thin Si layer body increases self-heating effect drastically, because as the Si film becomes thinner, the heat dissipation by the source/drain region becomes more restricted. This raises the thermal resistance. Thus thin film's temperature increases. Self-heating is responsible for performance degradation in SOI MOSFETs. Fully depleted is the depletion region covers the whole thickness of