

ULTRA THIN BODY 22nm SOI N-MOSFET (The Effect of Sidewall Spacer Oxide
Thickness to the Device Performance)

AMEEN NURZIKRI BIN MUNJANI

This report is submitted in partial fulfillment of the requirements for the award of
The Bachelor Degree of Electronic Engineering (Industrial Electronic)

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka (UTeM)

JUNE 2017

DECLARATION

“I hereby declare that this report is the result of my own work except for quotes as cited in the references.”

Signature:

Author : AMEEN NURZIKRI BIN MUNJANI

Date : 2 JUNE 2017

DECLARATION

"I hereby declare that I have read this thesis and in my opinion this report is sufficient in terms of the scope and quality for the award of Bachelor Degree of Electronic Engineering (Industrial Electronic)

Signature : 

Supervisor's Name: MDM. NIZA BENTI MOHD IDRIS

Date : 2 JUNE 2017

Dedicated to my beloved mother and father, my siblings and my colleagues who had been support me to complete this project.

ACKNOWLEDGEMENTS

“In the name of Allah, Most Gracious, Most Merciful”

First and for most, praise to Allah S.W.T, because of His bless that giving me to complete my Final Year Project and thesis in a given time without having any difficulties. The special thanks go to my helpful supervisor, Mdm Niza Bt Mohd Idris for the valuable guidance and advice. She inspired me greatly to work in this project. Her willingness to motivate me contributed tremendously to my project for showing me some example that related to the topic of my project.

I also take this opportunity to express a deep sense of gratitude to Universiti Teknikal Malaysia Melaka for giving me chance to undergo this Final Year Project as partial fulfillment for my Degree. Thanks again to Universiti Teknikal Malaysia Melaka for providing me with a good environment and facilities to complete this project

Finally, an honorable mention goes to my families and friends, especially Muhammad Sadiq Bin Sazali for their understandings, opinion, knowledges and supports in completing this project. Without helps of the particular that mentioned above, I could face many difficulties while to complete this project.

ABSTRACT

Currently, Ultra-Thin Body (UTB) fully depleted (FD) silicon-on-insulator (SOI) MOSFETs were of much interest because of advantageous features such as near-ideal gate swing and high drive current. This project is to investigate Ultra-Thin Body the effect of sidewall spacer oxide thickness to improve device performance. 4nm, 5nm, 6nm, 7nm, and 8nm are the different sidewall spacer oxide thickness that has been used in this research. The differences sidewall spacer oxide thickness does have a effect in the device performance. The tools utilize is Technology Computer Aided Design (TCAD). In TCAD software , silvaco's deckbuild ATHENA and ATLAS were used to design the physical structure of ultra-thin body hence obtaining its characteristics. The design structure will be go through a step by step fabrication process which parameter and value are stated in International Technology Roadmap for Semiconductor (ITRS). Then I-V characteristics of the UTB can be analyse by using ATLAS to show the particular performance of current device created.

ABSTRAK

Pada masa kini, *Ultra Thin Body Silicon On Insulator* (UTB SOI) untuk *Fully Depleted* (FD) MOSFET mempunyai banyak ciri-ciri yang menarik dan berfaedah seperti, hampir *ideal gate swing* dan keadaan elektrik *Ion* yang tinggi . Projek ini adalah untuk mengkaji *Ultra Thin Body MOSFET* bagi meningkatkan prestasi peranti. 4nm, 5nm, 6nm, 7nm, and 8nm ialah perbezaan *Sidewall Spacer Oxide Thickness* yang digunakan untuk kajian ini. Dengan menggunakan *Sidewall Spacer Oxide Thickness* yang berbeza memberikan impak kepada peranti. Perisian yang digunakan untuk membuat projek ini adalah Technology Computer Aided Design (TCAD). Dalam perisian TCAD, terdapat SILVACO ATHENA dan ATLAS yang telah digunakan untuk mereka bentuk struktur fizikal *Ultra Thin Body* dan sekaligus memperoleh ciri-ciri struktur yg dingini. Struktur reka bentuk akan dilakukan secara beperingkat di dalam proses fabrikasi dengan merujuk nilai yang dinyatakan dalam *International Technology Roadmap for Semiconductor* (ITRS). Seterusnya ciri-ciri I-V UTB boleh dianalisis dengan menggunakan ATLAS untuk menunjukkan prestasi tertentu dalam peranti yang direka.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	PROJECT TITLE	i
	REPORT STATUS VERIFICATION FORM	ii
	DECLARATION	iii
	SUPERVISOR DECLARATION	iv
	DEDICATION	v
	ACKNOWLEDGEMENT	vi
	ABSTRACT	vii
	ABSTRAK	viii
	TABLE OF CONTENT	xii
	LIST OF TABLE	xiii
	LIST OF FIGURES	xv
	ABBREVIATIONS	xvi
	LIST OF SYMBOLS	xviii
	LIST OF APPENDICES	xix
I	INTRODUCTION	
	1.0 Project Overview	1
	1.1 Project Objectives	2
	1.2 Problem Statement	2
	1.3 Scope of Project	2

1.4	Importance of the Project	3
1.5	Project Outline	3

II LITERATURE REVIEW

2.0	Introduction	4
2.1	Background Study	4
2.1.1	Fully Depleted Silicon-On-Insulator (FD-SOI)	4
2.1.2	Short Channel Effect in MOSFET	6
2.1.3	I-V Characteristics	8
2.1.4	Threshold Voltage	10
2.1.5	Effect of Sidewall Spacer Thickness	11
2.1.6	FD-UTB-SOI Compare to FinFETs	12
2.1.7	ITRS Projection on Fully Depleted SOI for Next Generation	13

III PROJECT METHODOLOGY

3.0	Introduction	15
3.1	Flowchart	15
3.2	Simulation Using Silvaco TCAD	17
3.2.1	ATHNEA	17
3.2.2	ATLAS	17
3.2.3	Deckbuild	17
3.2.4	Tonyplot	17
3.3	Step By Step of Fabrication Simulation	18

IV RESULTS AND DISCUSSION

4.0	Introduction	35
4.1	Specifications of The Device Based on ITRS	35
4.2	Result of 4nm Spacer Oxide	36
4.2.1	Ultra Thin Body Structure	36
4.2.2	Graph Transfer Curve for High Drain Voltage (0.87V)	38
4.2.3	Graph Transfer Curve for Low Drain Voltage (0.05V)	40
4.2.4	Overlay Graph of High Drain and Low Drain Voltage	42
4.3	Result of 5nm Spacer Oxide	44
4.3.1	Ultra Thin Body Structure	44
4.3.2	Graph Transfer Curve for High Drain Voltage (0.87V)	45
4.3.3	Graph Transfer Curve for Low Drain Voltage (0.05V)	47
4.3.4	Overlay Graph of High Drain and Low Drain Voltage	49
4.4	Result of 6nm Spacer Oxide	51
4.4.1	Ultra Thin Body Structure	51
4.4.2	Graph Transfer Curve for High Drain Voltage (0.87V)	52

4.4.3	Graph Transfer Curve for Low Drain Voltage (0.05V)	54
4.4.4	Overlay Graph of High Drain and Low Drain Voltage	56
4.5	Result of 7nm Spacer Oxide	58
4.5.1	Ultra Thin Body Structure	58
4.6.2	Graph Transfer Curve for High Drain Voltage (0.87V)	59
4.5.3	Graph Transfer Curve for Low Drain Voltage (0.05V)	61
4.5.4	Overlay Graph of High Drain and Low Drain Voltage	63
4.6	Result of 8nm Spacer Oxide	65
4.6.1	Ultra Thin Body Structure	65
4.6.2	Graph Transfer Curve for High Drain Voltage (0.87V)	66
4.6.3	Graph Transfer Curve for Low Drain Voltage (0.05V)	68
4.6.4	Overlay Graph of High Drain and Low Drain Voltage	70
4.7	Comparison of Results	71

V	CONCLUSION AND RECOMMENDATION	
5.0	Introduction	74
5.1	Conclusion	74
5.2	Recommendation	75
VI	REFERENCES	77
	APPENDIX A	79
	APPENDIX B	82
	APPENDIX C	85
	APPENDIX D	88

LIST OF TABLES

NO	TITLE	PAGE
2.1	The long term year (2010-2024) projection of some critical parameters for UTB-FD, low power operation	11
4.1	Specifications of the Device Based on ITRS	25
4.6	Comparison of ITRS value and Experimental Value	56

LIST OF FIGURES

NO	TITLE	PAGE
2.1	FD-SOI Transistors vs. Bulk and PD-SOI Transistors	4
2.2	Configuration of Fully Depleted N-channel SOI MOSFET	5
2.3	DIBL effect	7
2.4	Characterize N-MOS	8
2.5	n-type and p-type MOSFETs with an aluminum gate metal	8
2.6	Comparison ON current between high drain voltage and low drain voltage	9
2.7	UTB-SOI Compare with FinFET	10
3.2	Project Flowchart	14
3.3	Initial Structure	16
3.4	Deposition of Buried oxide layer	16
3.5	Deposition of Silicon Layer	17
3.6	Mask Layer	17
3.7	Etching of Mask Layer	18
3.8	Threshold Voltage Adjust Implantation	18
3.9	Etching The Rest of Mask Layer	19
3.10	EOT Deposition	19
3.11	Metal Gate Deposition	20
3.12	Desired Gate Length Layer	20
3.13	Deposition of Sidewall Spacer Oxide	21
3.14	Sidewall spacer oxide etching	21

3.15	Dry Etching Process Towards Sidewall Spacer	22
3.16	Aluminium Deposition	22
3.17	Etching Aluminium	23
3.18	Mirror Right	23
3.19	Specify Electrode Name	24
4.1	Ultra-Thin Body Structure	26
4.2	Ultra-Thin Body Structure With Contour and Electrode	26
4.3	Linear Graph	27
4.4	Log Graph	27
4.5	Linear + Log Graph	28
4.6	Linear Graph	29
4.7	Log Graph	29
4.8	Linear + Log Graph	30
4.9	Overlay Graph of Linear	31
4.10	Overlay Graph of Log	31
4.11	Ultra-Thin Body Structure	32
4.12	Ultra-Thin Body Structure With Contour and Electrode	32
4.13	Linear Graph	33
4.14	Log Graph	33
4.15	Linear + Log Graph	34
4.16	Linear Graph	35
4.17	Log Graph	35
4.18	Linear + Log Graph	36
4.19	Overlay Graph of Linear	37
4.20	Overlay Graph of Log	37
4.21	Ultra-Thin Body Structure	38
4.22	Ultra-Thin Body Structure With Contour and Electrode	38
4.23	Linear Graph	39
4.24	Log Graph	39
4.25	Linear + Log Graph	40
4.26	Linear Graph	41

4.27	Log Graph	41
4.28	Linear + Log Graph	42
4.29	Overlay Graph of Linear	43
4.30	Overlay Graph of Log	43
4.31	Ultra-Thin Body Structure	44
4.32	Ultra-Thin Body Structure With Contour and Electrode	44
4.33	Linear Graph	45
4.34	Log Graph	45
4.35	Linear + Log Graph	46
4.36	Linear Graph	47
4.37	Log Graph	47
4.38	Linear + Log Graph	48
4.39	Overlay Graph of Linear	49
4.40	Overlay Graph of Log	49
4.41	Ultra-Thin Body Structure	50
4.42	Ultra-Thin Body Structure With Contour and Electrode	50
4.43	Linear Graph	51
4.44	Log Graph	51
4.45	Linear + Log Graph	52
4.46	Linear Graph	53
4.47	Log Graph	53
4.48	Linear + Log Graph	54
4.49	Overlay Graph of Linear	55
4.50	Overlay Graph of Log	55
4.51	Comparison of ON current between high drain and Low drain	57
4.52	Comparison of OFF current between high drain and Low drain	58

LIST OF ABBREVIATIONS

UTB	-	Ultra-Thin Body
IC	-	Integrated Circuit
nm	-	Nano meter
SOI	-	Silicon On Insulator
FD	-	Fully Depleted
PD	-	Partially Depleted
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-Channel MOSFET
SS	-	Sub-Threshold Slope
DIBL	-	Drain-Induced Barrier Lowering
Si	-	Silicon
BOX	-	Buried Oxide
TCAD	-	Technology Computer Aided Design
2D	-	Two Dimension
AC	-	Alternating Current
DC	-	Direct Current
ITRS	-	International Technology Roadmap Semiconductor

LIST OF SYMBOLS

VTH	-	Threshold Voltage
VGS	-	Gate-To-Source Voltage
LG	-	Gate Length
TSI	-	Junction Depth
ID	-	Drain Current
VD	-	Drain Voltage
ION	-	Drive Current
IOFF	-	Leakage Current
SS	-	Sub-Threshold Voltage
EOT	-	Equivalent Oxide Thickness

LIST OF APPENDICES

NO	TITLE	PAGE
A	ATHENA INPUT FILE : Ultra-Thin Body 22nm SOI N-MOSFET with 4nm length of Thickness of Sidewall Spacer Oxide	64
B	ATHENA INPUT FILE : Ultra-Thin Body 22nm SOI N-MOSFET with 5nm length of Thickness of Sidewall Spacer Oxide	67
C	ATHENA INPUT FILE : Ultra-Thin Body 22nm SOI N-MOSFET with 6nm length of Thickness of Sidewall Spacer Oxide	70
D	ATHENA INPUT FILE : Ultra-Thin Body 22nm SOI N-MOSFET with 7nm length of Thickness of Sidewall Spacer Oxide	73

CHAPTER I

INTRODUCTION

1.0 Introduction

Ultra-Thin Body Silicon On Insulator (UTB SOI MOSFET) is a semiconductor device that provide a better performance and flexibility compare to any other conventional MOSFET .This research is to study on Ultra-Thin Body Silicon On Insulator (UTB SOI) which the structure in fully depleted.. Silicon on insulator (SOI) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance.

In this research Fully Depleted Ultra-Thin Body Silicon on Insulator (FD UTB SOI) are used because it has many advantages compare to other conventional MOSFET. FDSOI devices has a very thin film so the less depletion charges happens consequential in higher switching speeds. For the structure this device using titanium as a metal gate as it have better electrical characteristics gate compare to previous gate [5]. Furthermore when adding a buried oxide through the structure of Ultra-Thin Body the junction capacitance slightly reduce which may result in faster switching. Then the gate are stake up by a layer of silicon dioxide. The study is extend to the effect of sidewall spacer oxide thickness variation to see the

performance of the device. The tools utilize 22nm N-MOSFET will be simulate by silvaco and t-cad simulator and i-v characteristics obtain by using atlas software.

Silvaco is one of the device simulator which allow method of fabrication, and simulation for semiconductor devices. For this research Athena and Atlas is used. Athena is a general purpose 1D, 2D process simulator for applications including Etching and Deposition, Implantation, Annealing, and Stress simulation. While Atlas is a 2D and 3D device simulator that performs DC, AC, and transient analysis for silicon, binary, ternary, and quaternary material-based devices.

1.1 Objective

The objectives of this project are:

- To design the UTB 22nm SOI MOSFET with the optimum performance in regarding to drive current, gate leakage and voltage threshold .
- To analyze IV characteristic due to sidewall spacer oxide thickness variation
- To examine a comprehensive simulation study of fully depleted ultra-thin body silicon on insulator (FD-UTB SOI) at nanometer regime.

1.2 Problem Statement

- Sidewall spacer oxide thickness in ‘ON’ or ‘OFF’ state current one of the concern that affect the performance of the device.
- UTB SOI is design to eliminate gate leakage problem which drain lot of current in electronic devices.

1.3 Scope of Project

- Focus on UTB 22nm SOI MOSFET.
- Utilize T-cad and Silvaco simulation tool use to obtain I-V characteristic such as voltage threshold, drive current and gate leakage.

1.4 Importance Of The Project

- To improve the experimental results already attained by engineers, and to propose new areas for development.
- UTB can be used in microelectronics industry and high performance radio frequency application such as satellite .
- UTB also making industry to create tiny integrated circuit but with variable functions
- Giving reliable performance and flexibility compare to other MOSFET

1.5 Project Outline

In chapter 1, overall idea of what this project about but in summary. It consist of introduction elements such as objective, problem statement, scope and important of the project.

For chapter 2, it is to define each of the key terns including definition and terminology that are related to the topic. All case studies and facts are collected to support the evidence of the research

Next, chapter 3 will describe project flow from the beginning of the research until end. It specify what tools or software that need to be utilize in order to get structure and characteristics result.

In chapter 4, discussion about five different sidewall spacer oxide thickness is made which is 4nm, 5nm, 6nm, 7nm and 8nm. Then each sidewall spacer oxide thickness give it different I-V analysis which then will be discuss further.

Lastly for chapter 5, based on the result obtained in chapter 4 comparison is made to see if objective in chapter 1 is achieve. A few recommendation is stated for better improvement in future research.

CHAPTER II

LITERATURE REVIEW

2.0 Introduction

To even start the project, the basic ideas of how this project were conducted with referring to previous study in detail. The literature review consists of concepts and ideas about the overall of the project.

2.1 Background Studies

2.1.1 Fully Depleted Silicon-On-Insulator (FD-SOI)

Fully Depleted Silicon on Insulator (FD-SOI) technology depends on an ultra-thin layer of silicon over a Buried Oxide (commonly called BOX) as shown in figure 2.1. Transistors fabricated into this top silicon layer are Ultra-Thin Body devices and have distinctive, extremely attractive characteristics. Two flavours of buried oxide can be used: standard thickness (typically 145nm thick as classically in volume production PD-SOI digital chips today), or ultra-thin BOX, for example 10 or 25nm (UTBOX, Ultra-Thin Buried Oxide) [1].

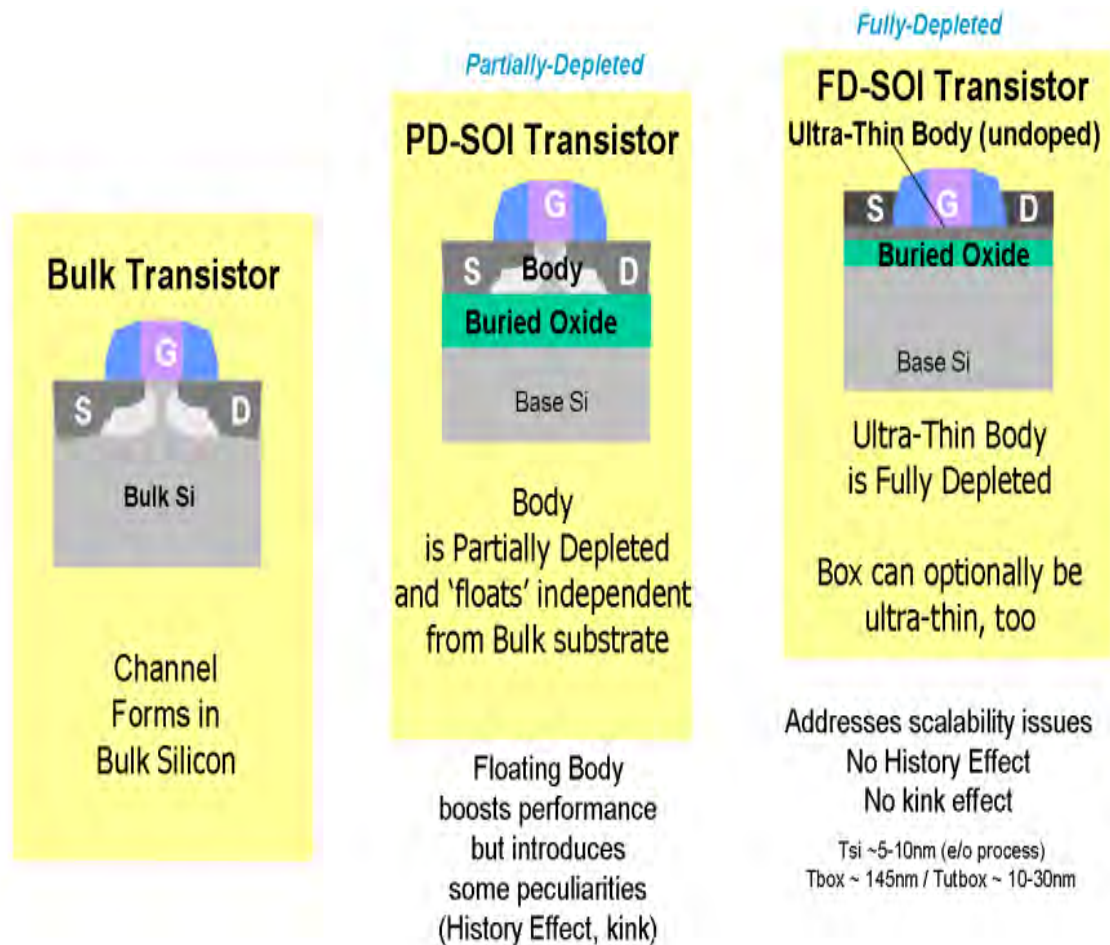


Figure 2.1: FD-SOI Transistors vs. Bulk and PD-SOI Transistors

Ultra thin body (UTB) SOI devices are in between the utmost promising candidates for MOSFET in nano scale regime . These devices can work in Fully Depleted (FD) regime and thus decrease short channel effects, leakage current and uphold good scaling capability. Figure 2.2 shows structures offer to decrease parasitic capacitance and eradicate latch up. However due to the presence of a buried silicon dioxide layer, these devices suffer from self-heating . This is due to the fact that the thermal conductivity of silicon-dioxide (SiO₂) is smaller than that of silicon. In addition, use of ultra thin Si layer body increases self-heating effect drastically, because as the Si film becomes thinner, the heat dissipation by the source/drain region becomes more restricted. This raises the thermal resistance. Thus thin film's temperature increases. Self-heating is responsible for performance degradation in SOI MOSFETs. Fully depleted is the depletion region covers the whole thickness of