A STUDY OF THE CASCADED H-BRIDGE MULTILEVEL INVERTER BASED ON SUPERCAPACITOR FOR HARMONIC REDUCTION

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I declare that the project report entitled “A Study of Cascaded H-Bridge Multilevel Inverter Based on Super Capacitor for Harmonic Reduction” is the results from my own research except as cited in the references.

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Date : 8 June 2016

I hereby declare that I have read through this report and found that is comply the partial fulfillment for awarding the degree of Bachelor of Electrical Engineering (Industrial Power)

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Date : 8 June 2016

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ABSTRACT

This project present a study of cascaded H-bridge multilevel inverter based on supercapacitor to reduce harmonic for high power applications. Applications of multilevel converters are able to reduce the number of harmonics contained in the system of electrical network. This study deals seven-level cascaded H-Bridge multilevel inverter with sinusoidal pulse width modulation (SPWM) controller and two type of energy storage comprises of supercapacitor and DC supply for reduction of the harmonic in the electrical network. This paper also deals with simulation of seven-level cascaded H-Bridge multilevel inverter in MATLAB/SIMULINK environment.

The proposed system designed using MATLAB/SIMULINK consists of a supercapacitor and DC supply as energy storage. The controller based on sinusoidal pulse width modulation was applied to the inverter. The design to change the modulation index from 0.5 to 1.0 also is used at controller to monitor the supercapacitor performance to reduce the harmonic is also discussed. The various performances of simulation results between super-capacitor and DC supply have been investigated. The Total Harmonic Distortion (THDv) of the inverter output voltage is measured where two types of energy storages (DC supply and super capacitor) are applied to the inverter input. It can be observed that the THD voltage output of the inverter for the super capacitor is considerably lower than the DC supply that is exceed 90% and meet the needs of supercapacitor considered low at 5% as specified by IEEE 519 standard on harmonic distortion level.

ABSTRAK

Projek ini membentangkan kajian penyongsang bertingkat cascaded H-Bridge berdasarkan superkapasitor bagi mengurangkan harmonik untuk aplikasi kuasa tinggi. Aplikasi penyonsang bertingkat dapat mengurangkan bilangan harmonik yang terkandung dalam sistem rangkaian elektrik. Kajian ini membincangkan tujuh peringkat penyongsang bertingkat cascaded H-Bridge dengan pengawal sinusoidal modulasi lebar denyut (SPWM) dan dua jenis penyimpanan tenaga terdiri daripada superkapasitor dan bekalan DC untuk mengurangkan harmonik dalam rangkaian elektrik. Kertas kerja ini juga berkaitan dengan simulasi tujuh peringkat penyongsang bertingkat cascaded H-Bridge dalam persekitaran / SIMULINK MATLAB.

Sistem yang dicadangkan dan direka menggunakan MATLAB / SIMULINK terdiri daripada superkapasitor dan bekalan DC sebagai penyimpanan tenaga. Pengawal berdasarkan sinusoidal lebar denyut modulasi telah digunakan untuk penyongsang. reka bentuk untuk menukar indeks pemodulatan dari 0.5 hingga ke 1.0 juga digunakan pada pengawal untuk memantau prestasi superkapasitor untuk mengurangkan harmonik juga dibincangkan. Pelbagai prestasi dan keputusan simulasi antara superkapasitor dan bekalan DC telah disiasat. Jumlah herotan harmonic (THDv) daripada voltan keluaran penyongsang diukur di mana dua jenis penyimpanan tenaga (DC bekalan dan super kapasitor) digunakan untuk input penyongsang. Ia boleh diperhatikan bahawa keluaran voltan THD daripada penyongsang untuk superkapasitor adalah jauh lebih rendah daripada bekalan DC yang melebihi 90% dan memenuhi keperluan untuk superkapasitor dianggap rendah pada kadar 5% yang ditetapkan oleh IEEE 519 standard pada tahap herotan harmonik.

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Multilevel inverter is mainly use in desired single or three phase voltage waveform. The desired output voltage is obtained by combining several direct current (DC) sources. The most common independent sources used are solar cells, fuel cells, batteries and super capacitors. Nowadays, there are three famous of multilevel voltage source inverters exist such as neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs)[1]. Among this inverter, cascaded multilevel inverter reaches the higher output voltage and power level and the higher reliability due to its performance. The cascaded H-bridge multilevel inverter have been applied where high power and power quality are essential, for example, static synchronous compensators active filter and reactive power compensation applications, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging. If the number of switches is increase, it will increase voltage. The circuit will become complex if the voltage stresses and switching losses is increase. By using the proposed multilevel inverter, the number of switches will reduce significantly and hence the efficiency will improve. In high power applications, to reach the maximum energy efficiency, the harmonic of the output waveforms has to be reduced as much as possible in order to avoid distortion in the grid [2].

1.2 Problem Statement

Based on previous work that has been done, most researchers focus on the harmonic that occur on load and less concerned about the harmonics that occur at the power source. Power sources such as batteries, solar and other sources of DC supply which has a high Total Harmonic Distortion (THD) in term of voltage. Thus, this study is to change the power source from DC supply to supercapacitor and monitor it performance for harmonic reduction in output of cascaded H-Bridge multilevel inverter by using MATLAB/SIMULINK.

1.3 Objectives

The objectives of this project are:

1. To study the concept of cascade H-Bridge multilevel inverter.
2. To compare the output voltage at cascaded H-Bridge multilevel inverter based on DC supply and supercapacitor for harmonic reduction.

1.4 Project Scope

In this study, the main focused of this project is to study of stage level of cascaded H-Bridge multilevel inverter based on supercapacitor for harmonic reduction in electrical system. This project also compares the effectiveness in term of the energy storage between DC supply and supercapacitor for harmonic reduction in term of voltage in electrical network.

1.5 Expected outcome of the project

In this study, this project is to monitor the performance of DC supply and supercapacitor for harmonic mitigation based on cascaded H-Bridge multilevel inverter.

CHAPTER 2

LITERATURE REVIEW

2.1 Theory and basic principle

In this chapter, the main focused is to discuss the related project from previous work that has been done by using cascaded H-Bridge multilevel inverter. From the work that has been done, the previous researchers use several type of direct current (DC) source such as solar cell, DC supply, and batteries. Therefore, to design and monitoring the harmonic reduction in the cascaded H-Bridge multilevel inverter based on previous work, the MATLAB SIMULINK software is used.

2.2 Inverter

Power inverters are devices which can convert electrical energy of DC form into that of AC. They come in all shapes and sizes, from low power functions such as powering a car radio to that of backing up a building in case of power outage. Inverters can come in many different varieties, differing in price, power, efficiency and purpose.

Basic circuit

Equivalent Circuit

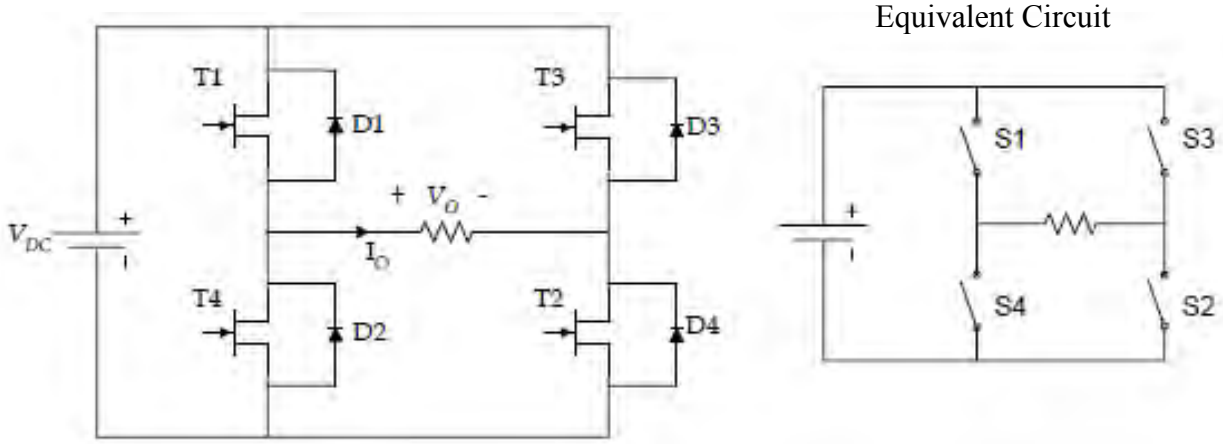

Figure 2.1: Basic circuit and equivalent circuit of inverter

The purpose of a DC/AC power inverter is typically to take DC power supplied by a battery, such as a 12 volt car battery, and transform it into a 120 volt AC power source operating at 60 Hz, emulating the power available at an ordinary household electrical outlet.

On the market today are two different types of power inverters, modified sine wave and pure sine wave generators. These inverters differ in their outputs, providing varying levels of efficiency and distortion that can affect electronic devices in different ways.

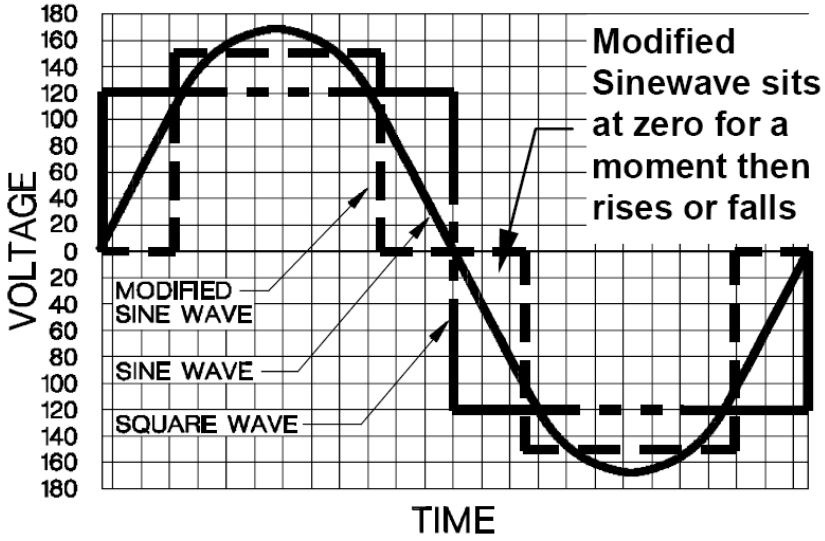

Figure 2.2: Square, Modified and Pure Sine wave

A modified sine wave is similar to a square wave but instead has a "stepping" look to it that relates more in shape to a sine wave. This can be seen in Figure 2.2, which displays how a modified sine wave tries to emulate the sine wave itself. The waveform is easy to produce because it is just the product of switching between three values at set frequencies, thereby leaving out the more complicated circuitry needed for a pure sine wave.

The modified sine wave inverter provides a cheap and easy solution to powering devices that need AC power. It does have some drawbacks as not all devices work properly on a modified sine wave, products such as computers and medical equipment are not resistant to the distortion of the signal and must be run off of a pure sine wave power source.

Pure sine wave inverters are able to simulate precisely the AC power that is delivered by a wall outlet. Usually sine wave inverters are more expensive then modified sine wave generators due to the added circuitry. This cost, however, is made up for in its ability to provide power to all AC electronic devices, allow inductive loads to run faster and quieter, and reduce the audible and electric noise in audio equipment, TV's and fluorescent lights.

2.2.1 How Does It Work?

Figure 2.3 show the component involves which is four Insulated Gate Bipolar Transistor (IGBT) to operate this H-Bridge inverter.

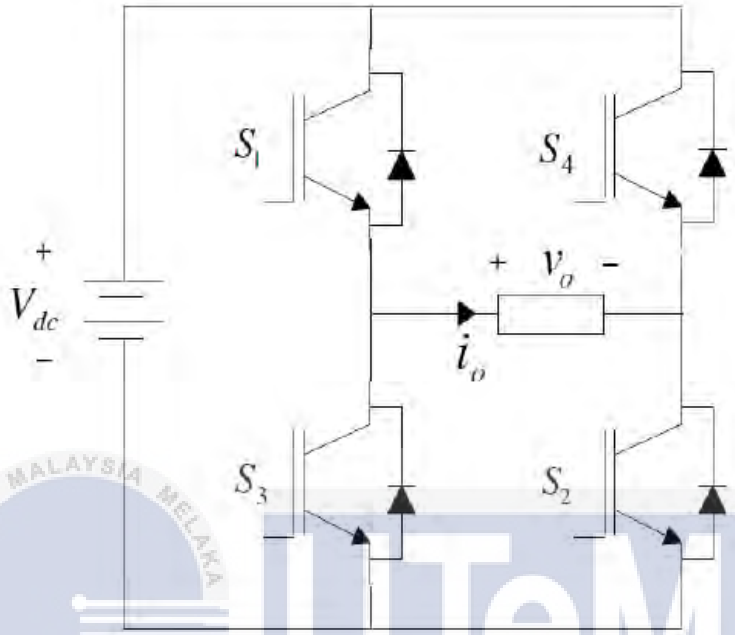

Figure 2.3 Schematic Diagram of basic H-Bridge inverter

The above topology are analyzed under the assumption of ideal circuit conditions. Accordingly, it is assumed that the input dc voltage (Vdc) is constant and the switches are lossless. In full bridge topology has two such legs. Each leg of the inverter consists of two series connected electronic switches shown within dotted lines in the figures. Each of these switches consists of an IGBT type controlled switch across which an uncontrolled diode is put in anti-parallel manner. These switches are capable of conducting bi-directional current but they need to block only one polarity of voltage. The junction point of the switches in each leg of the inverter serves as one output point for the load.

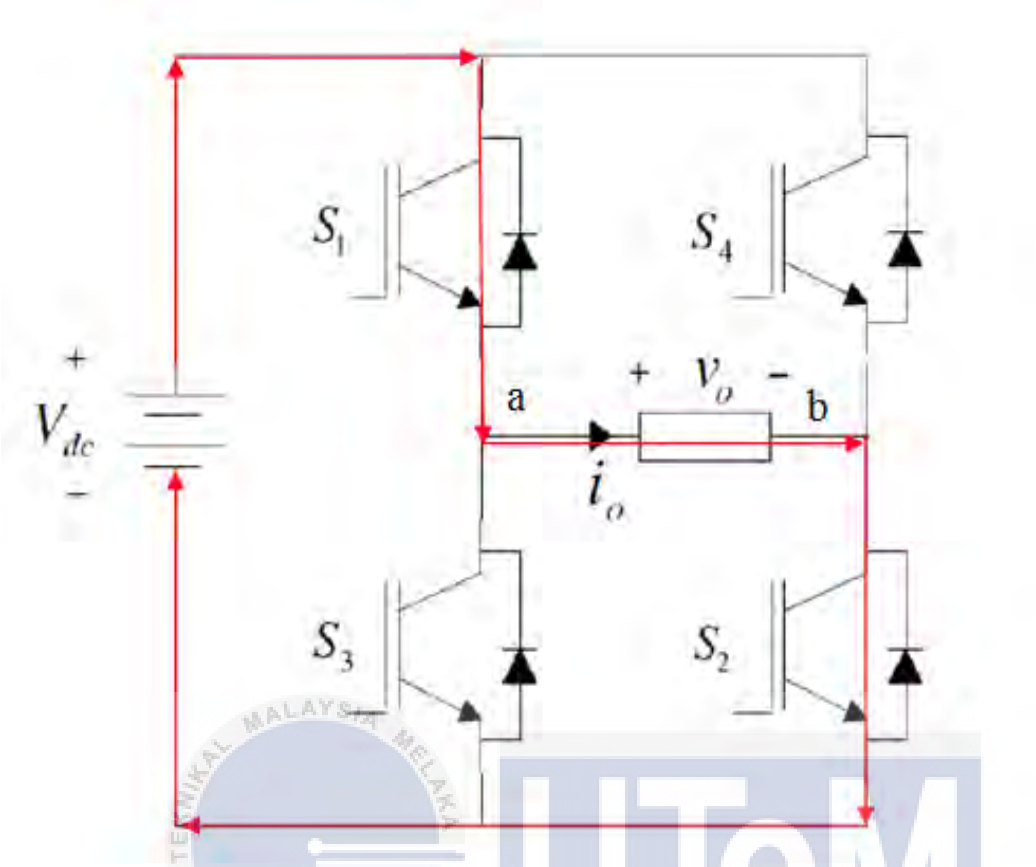

Figure 2.4: Positive cycle of basic H-Bridge inverter

Figure 2.4 show that the operation of basic H-Bridge inverter in posotive cycle.When the switches S1 and S2 are turned on simultaneously $0 \leq t \leq T1$, the the input voltage Vin appears across the load and the current flows from point a to b. S1– S2 ON, S3 – S4 OFF ==> ν o = + Vs.

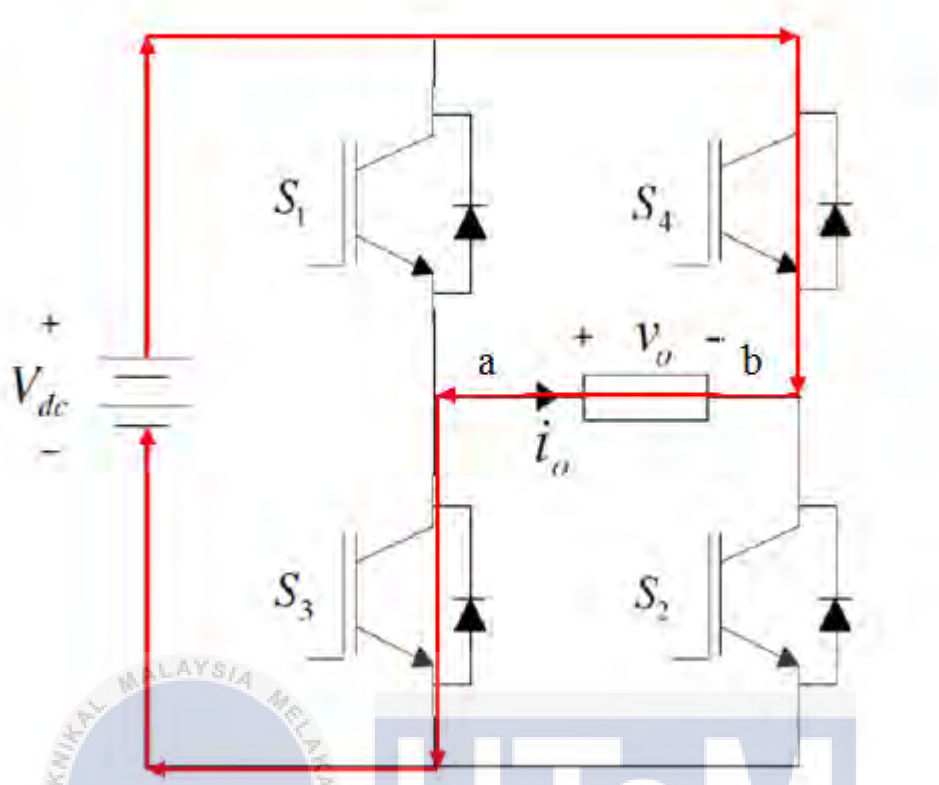

Figure 2.5: Negative cycle of basic H-Bridge inverter

Figure 2.5 shows that the operation basic H-Bridge inverter in negative cycle. If the switches S3 and S4 turned on duration T1 ≤ t ≤ T2, the voltage across the load the load is reversed and the current through the load flows from point b to a.

S1 – S2 OFF, S3 – S4 ON ==> v o = -Vs

Table 2.1 Table of switching scheme of basic H-Bridge inverter

Switching State	S_1	S_2	S_3	S_4	v_{out}
1	On	On	Off	Off	$+V_{dc}$
0	On	Off	Off	On	0
1	Off	Off	On	On	$-V_{dc}$

2.2.2 Output Waveforms

An inverter can produce square wave, modified sine wave, pulsed sine wave, or sine wave depending on circuit design. There are two basic designs for producing household plug-in voltage from a lower-voltage DC source, the first of which uses a switching boost converter to produce a higher-voltage DC and then converts to AC. The second method converts DC to AC at battery level and uses a line-frequency transformer to create the output voltage

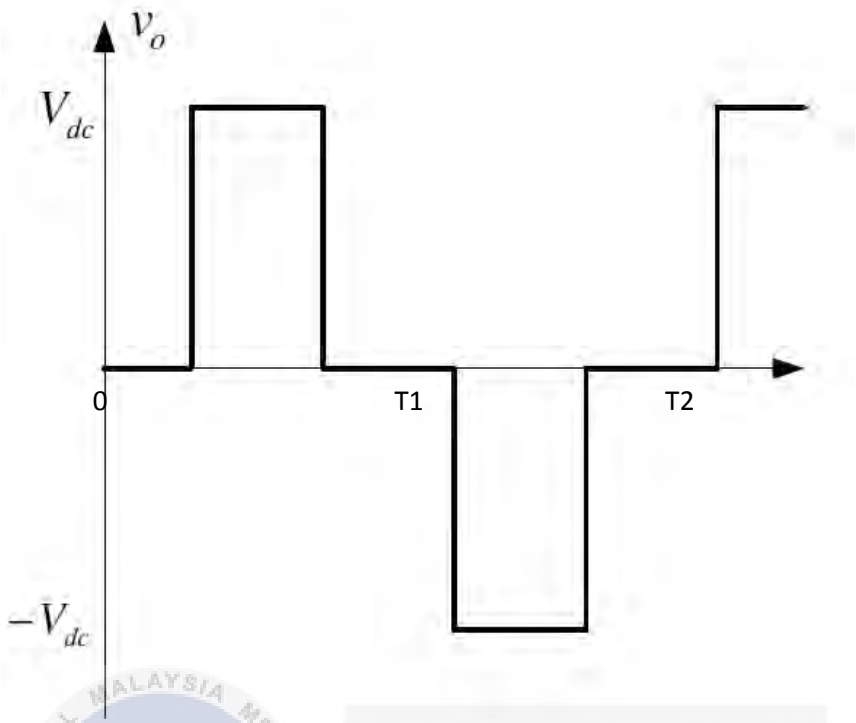

Figure 2.6: Output waveform of basic H-Bridge inverter

Based on Figure 2.6, single-phase square wave type voltage source inverter produces square shaped output voltage for a single-phase load. Such inverters have very simple control logic and the power switches need to operate at much lower frequencies compared to switches in some other types of inverters.

The first generation inverters, using thyristor switches, were almost invariably square wave inverters because thyristor switches could be switched on and off only a few hundred times in a second. In contrast, the present day switches like IGBTs are much faster and used at switching frequencies of several kilohertz. Single-phase inverters mostly use half bridge or full bridge topologies.

2.3 Multilevel Inverter

The concept of multilevel inverters (MLI) does not depend on just two, three or five levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 2.7, with lower $\frac{dy}{dt}$ and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed. To better understand multilevel inverters the more conventional three-level inverter, shown in Figure 2.8, can be investigated. It is called a three-level inverter since every phase-leg can create the three voltages $\frac{V_{dc}}{2}$, 0, - $\frac{V_{dc}}{2}$ as can be seen in the first part of Figure 2.7. A three-level inverter design is similar to that of a conventional two-level inverter but there are twice as many valves in each phase-leg. In between the upper and lower two valves there are diodes, called clamping diodes [3], [4]

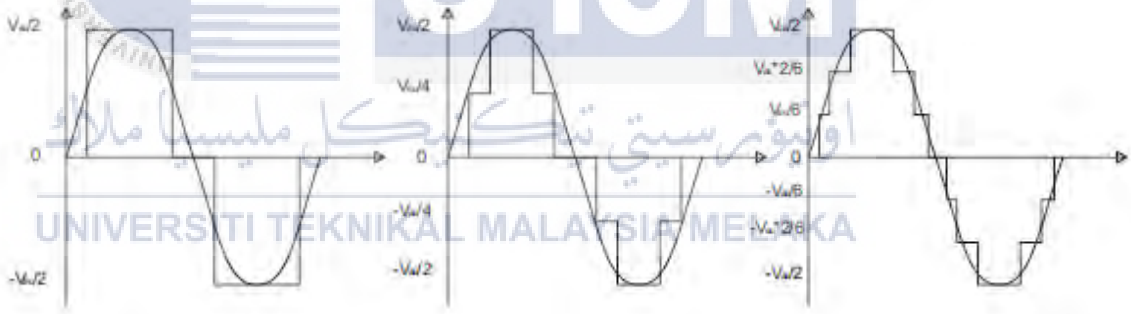

Figure 2.7: A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency.[4]

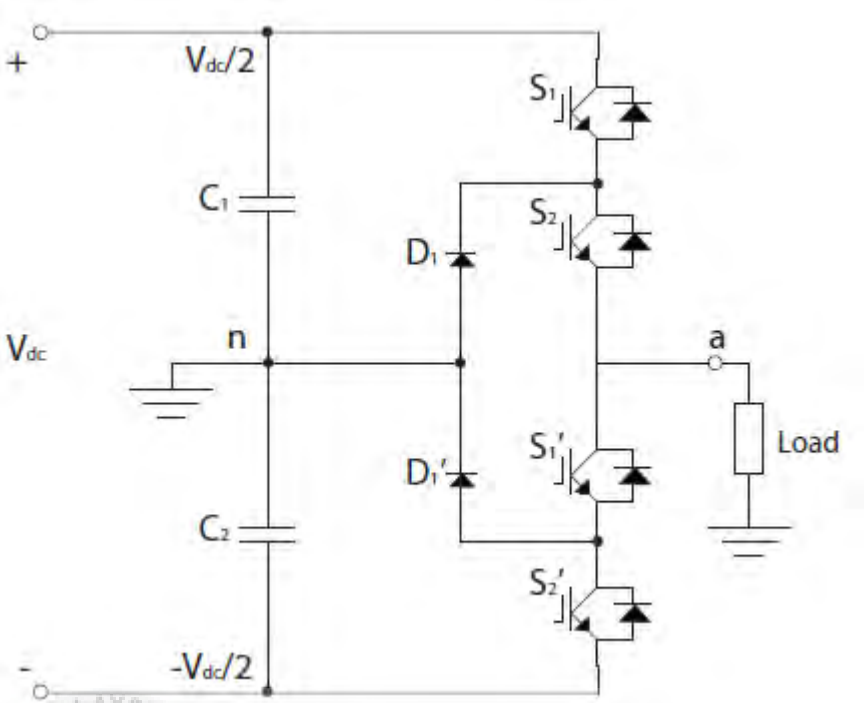

Figure 2.8: One phase leg of a three-level inverter

It connected to the neutral midpoint in between two capacitors, marked n in the figure. This capacitor build up the DC-bus, each capacitor is charged with the voltage $\frac{V_{dc}}{2}$. Together with another phase-leg an output line-to-line voltage with even more levels can be obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure 2.7, the result is a multilevel inverter with clamping diode topology. Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and $\frac{dy}{dt}$, generate smaller common-mode voltage and operate with lower switching frequency [5] compared to the more conventional two-level inverters.

With a lower switching frequency the switching losses can be reduced and the lower $\frac{dy}{dt}$ comes from that the voltage steps are smaller, as can be seen in Figure 2.7 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, topologies with different properties have been developed, some of which will be looked upon in this report. The Multilevel inverter topologies that are investigated in this work are: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs).

2.3.1 Advantages of Multilevel Inverter

The multilevel inverter has a several advantages that is, first is the common mode voltage which the multilevel inverters produce common mode voltage, reducing the stress of the motor and don't damage the motor.Second is the input current which multilevel inverters can draw input current with low distortion .Beside that, it also can make switching frequency. The multilevel inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved.Last but not least and the importart component is it can reduced harmonic distortion. Selective harmonic elimination technique along with the multi level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit.

2.4 Cascaded H-Bridge Multilevel Inverter

Cascaded H-Bridge multilevel inverter is the alternative way to eliminate the harmonic distortion because the Pulse Width Modulation (PWM) inverter does not completely eliminate the harmonic in the output waveform. The structure of a multilevel inverter based series connection on inverters three phase H-bridge will produce a sinusoidal wave voltage [1]. Direct current (DC) source is supplied in each cell of the inverter. The 2N+1 number are the number of phase voltage levels at inverter terminals or the output where N is the number of the cells or dc link voltage. The voltage across the capacitor might differ among the cell and each cell has separate dc link capacitor. So, one dc voltage source is needed for each power circuit. The number of phase voltage levels is proportional to the number of dc link capacitor. Polarity positive, negative and zero voltage may have in each of H-bridge cell. The sum of all H-bridge cell voltages is final output voltage and is symmetric with respect to neutral point, so the number of voltage levels is odd.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Insulated Gate Bipolar Transistor (IGBT), Gate Turn Off (GTO) Thyristors switched is typically used in Cascade H-bridge multilevel inverter. It has high switching frequency and these switches have a low block voltage [2]. By adjusting the switching angles, the total harmonic reduction can be optimized. Other than that, the development of cascade H-bridge inverter is cheaper than diode clamped or flying capacitor.

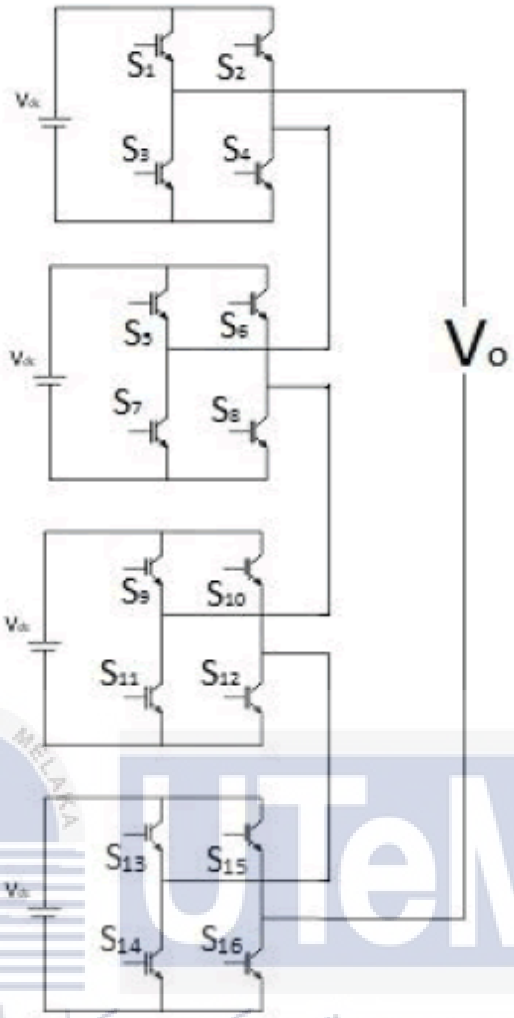

Figure 2.9: Schematic Diagram of nine-level cascaded H-Bridge multilevel inverter

2.4.1 How Does It Work?

In single phase inverter, each phase is connected to single dc source. Each level generates three voltages which are positive, negative and zero. This can be obtained by connecting the AC source with the DC output and then using different combinations of the four switches. The inverter will remain ON when two switches with the opposite positions will remain ON. It will turn OFF when all the inverters switch ON or OFF. To minimize the total harmonic distortion, switching angles are defined and implemented.

The calculations for the measurement of switching angle will remain the same. This inventor can be categorized further into the five-level cascaded H-Brige multilevel inverter, seven-level cascaded H-Brige multilevel inverter, nine-level cascaded H-Brige multilevel inverter and etc.

In five-level cascaded H-Bridge multilevel inverters, Two H-Bridge inverters are cascaded. It has five levels of output and uses eight switching devices to control.In seven-level cascaded H-Bridge multilevel inverters, Three H-Bridge inverters are cascaded. It has seven output levels and use and use 12 switching devices where nine-level cascaded H-Bridge multilevel inverters, Four H-Bridge inverters are cascaded. It has nine output levels and use and use 16 switching devices and etc.

2.4.2 Applications of Cascaded H-bridge Multilevel Inverters

Cascaded H-Bridge multilevel inverters are mostly used for static var applications i.e., in renewable resources of energy and battery based applications. Cascaded H-Bridge multilevel inverters can be applied as a delta or wye form. Best application is when used as photovoltaic cell or fuel cell. It can also be used in car batteries to run the electrical components of the car beside can be used in electrical braking system of the vehicles. Other than that, it also can use in motor drives, active filters, DC power source utilization, power factor compensators, back to back frequency link systems and interfacing with renewable energy resources.

2.4.3 Advantages of Cascade H-Bridge Multilevel Inverters.

The cascaded H-Bridge multilevel inverter has a several advantages that are the output voltages levels are doubled the number of sources. Manufacturing can be done easily and quickly, packaging and layout is modularized, easily controllable with a transformer and cheap than other multilevel inverter.

2.5 DC Supply

Direct current (DC) is a continuous electrical current flowing in one direction only as shown at Figure 2.10 This is a type of electrical current supplied if the cell voltage. As long as the polarity of the voltage at the terminals of the cell voltage is fixed and is not reversed, the cell voltage can be referred to as a direct voltage source.[6],[7]

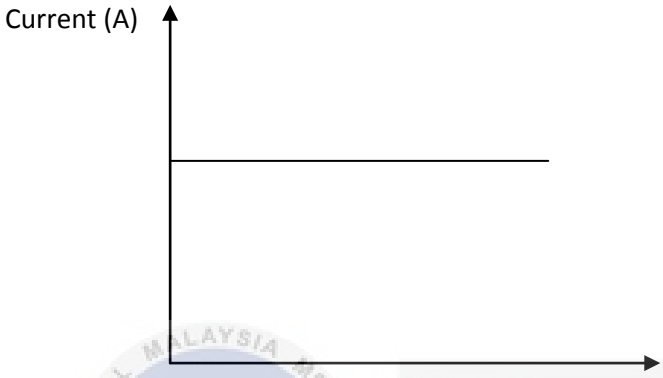

Figure 2.10: Direct current against time graph.

2.5.1 Source of Direct Current (DC)

1) Battery

Battery cell or a direct current source which it is specially designed to produce output voltage and output current exceeds a certain maximum. The potential differences produce between the cell plates depends on electrode materials but not to the physical size of electrode or electrolyte quantity. Cell output current depending on output voltage and load resistance beyond that;

$$I = \frac{V}{R}$$

Where I is the output current, V is the cell terminal voltage and R is external resistance load. However, the maximum current that can be supplied by a single cell has its limits. When this limit is reached, the terminal voltages of cells began to drop. With the current output cannot be increased. The cells are large voltage output current physics can bear larger than the small cells.

2) Solar cell

A solar cell is also a source of direct current at which sunlight can generate an electric current. Examples of appliances that use sunlight as a source of electric current is like a calculator, water heating systems in the home and etc.

2.6 Main Capacitance

The capacitance value can be calculated in two different ways. The first method is to look at the voltage derivative during charging of the super capacitor. The relation between voltage derivative and the capacitance is

$$I(t) = C \frac{d}{dt} u(t) \quad (1)$$

Where;
C = the capacitance.

Using this relation the capacitance can be calculated for different parts of the voltage curve. When high currents are used, other effects than the capacitance can affect the voltage level. These effects can cause the calculated capacitance value to be incorrect.

2.7 Supercapacitor

The supercapacitor, also known as ultracapacitor or double-layer capacitor, differs from a regular capacitor in that it has very high capacitance. A capacitor stores energy by means of a static charge as opposed to an electrochemical reaction. Applying a voltage differential on the positive and negative plates charges the capacitor. This is similar to the buildup of electrical charge when walking on a carpet. Touching an object releases the energy through the finger.

There are three types of capacitors and the most basic is the electrostatic capacitor with a dry separator. This classic capacitor has very low capacitance and is mainly used to tune radio frequencies and filtering. The size ranges from a few pico-farads (pf) to low microfarad (μF).The electrolytic capacitor provides higher capacitance than the electrostatic capacitor and is rated in microfarads (μF), which is a million times larger than a pico-farad (pf). These capacitors deploy a moist separator and are used for filtering, buffering and signal coupling.

Similar to a battery, the electrostatic capacity has a positive and negative that must be observed.The third type is the supercapacitor, rated in farads, which is thousands of times higher than the electrolytic capacitor. The supercapacitor is used for energy storage undergoing frequent charge and discharge cycles at high current and short duration.

Several types of electrodes have been tried and the most common systems today are built on the electrochemical double-layer capacitor that is carbon-based, has an organic electrolyte and is easy to manufacture.

`Figure 2.11 shows the design uses super capacitor instead of DC supply because supply is insufficient to supply real power charge and discharge conditions. Super capacitor uses circuit RC connected series formed by a capacitor constant and a resistance constant. The capacitance and the serial resistance of the super capacitor are dependent on frequency, temperature and voltage.

The simulations have been designed, the time for simulation is short and thus the effect of the temperature and voltage difference can be neglected because they are almost constant. The self-discharge has been neglected due to the same reason. The frequency variations of the super capacitor current are low enough to assume that the capacitor value is also constant, super capacitors can operate even at low temperature (e.g. -50°C). [8]

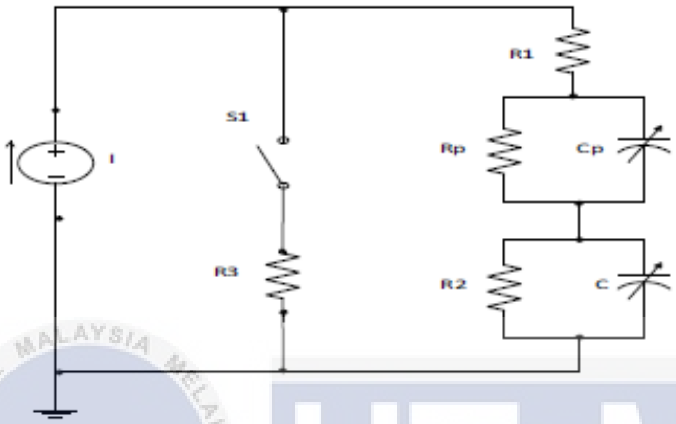

Figure 2.11: Basic circuit model of the Super capacitor (EPCOS) [9]

Super capacitor can be supplied to high voltage charge and discharge is neglected because the frequency, temperature and voltage are constant, high performance super capacitor apply modeling can reduce Total Harmonic Reduction (THD). The capacitance C is responsible for the most important phenomenon in the model. It determines how charge is handled in the circuit. The amount of energy stored and the rate of energy level variations are both determined mainly by the capacitance value. The resistance R2 that is connected in parallel with the capacitor is meant to represent the self-discharge effect. The series resistance R1 represents the losses during charge and discharge.

These losses occur because the conducting element in the super capacitor has a resistance, so the connection is not ideal. The over voltage protection provided by R3 and the switch controlling its connection to the circuit is necessary to prevent damage to the capacitor elements by balancing the voltage level.

The voltage balancing is needed because otherwise the voltage in one separate cell can increase higher than the others, resulting in gassing or explosion. This voltage difference can occur if one cell has a lower capacitance than the others, since those results in more energy being stored. The resistance Rp and the capacitance Cp are included in the circuit to model some of the fast dynamics in the behavior of the super capacitor.

$$R1 = \frac{\Delta u}{\Delta i} \tag{2}$$

$$R3 = \frac{\Delta t}{-\ln\left(\frac{v_1}{v^0}\right)C} \tag{3}$$

$$U(t) = \int \frac{i\,(t)}{c}\ dt \tag{4}$$

The creation of a first Simulink model to use the super capacitor according to the basic circuit is described in Figure 2.11. A simple circuit initial model testing is done consisting of a capacitance and resistance in parallel with a resistance in series. This base circuit manages to show the basic function of the super capacitor [10].

2.7.1 Performance comparison between supercapacitor and batteries

Table 3: Performance comparison between supercapacitor and batteries [11]

Parameter	Supercapacitor	Batteries
Energy Storage	Watt-second	Watt-Hour
Charge Method	Voltage across terminal	Constant current & voltage
Power Delivered	Rapid discharge, linear or exponential voltage decay	Constant voltage over long time period
Charge/Discharge Time	Millisecond to second	1 to 10 hours
Form Factor	small	Small to large
Weight	1g to 2g	1g to >10kg
Energy Density	1 to 5Wh/kg	8 to 600Wh/kg
Operating Voltage	2.3V-2.75V/cell	1.2V-4.2V/cell
Lifetime	>100K cycles	150-1500 cycles
Operating Temperature	-50 to + 85˚C	-20 to + 65˚C

Table 3 shows the comparison between supercapacitor with batteries. The supercapacitor used for energy storage undergoing frequent charge and discharge cycles at high current and short duration. All capacitors have voltage limits. While the electrostatic capacitor can be made to withstand high volts, the supercapacitor is confined to 2.5–2.7V. Voltages of 2.8V and higher are possible but they reduce the service life. To get higher voltages, several supercapacitors are connected in series. Serial connection reduces the total capacitance and increases the internal resistance. Strings of more than three capacitors require voltage balancing to prevent any cell from going into over-voltage.

The specific energy of the supercapacitor ranges from 1 to 5Wh/kg, 10 to 60 times less than batteries. The charge time of a supercapacitor faster than batteries. The supercapacitor cannot go into overcharge and does not require full-charge detection; the current simply stops flowing when full.

The supercapacitor can be charged and discharged virtually an unlimited number of times. Unlike the batteries, which have a defined cycle life, there is little wear and tear by cycling a supercapacitor. Age is also kinder to the supercapacitor than batteries. Under normal conditions,a supercapacitor fades from the original 100 percent capacity to 80 percent in 10 years. Applying higher voltages than specified shortens the life. The supercapacitor is forgiving in hot and cold temperatures, an advantage that cannot be met equally well by batteries.

2.7.2 Applications of supercapacitor

Supercapacitors are deployed to deliver short-term power; batteries are chosen to provide long-term energy. It have been widely used as the electrical equivalents offlywheels in machines or "energy reservoirs" that smooth out power supplies to electrical and electronic equipment. Supercapacitors can also be connected to batteries to regulate the power they supply

One common application is in wind turbines, where very large supercapacitors help to smooth out the intermittent power supplied by the wind. In electric and hybrid vehicles, supercapacitors are increasingly being used as temporary energy stores for regenerative braking (where the energy a vehicle would normally waste when it comes to a stop is briefly stored and then reused when it starts moving again).

The motors that drive electric vehicles run off power supplies rated in the hundreds of volts, which means hundreds of supercapacitors connected in series are needed to store the right amount of energy in a typical regenerative brake.

2.8 Study of Multilevel Inverter Based On MATLAB SIMULINK Modeling

This paper describes the research in the comparative study between the multi-level inverter cascading H-bridge using MATLAB SIMULINK. It describes the layout to simulate the step-by-step procedure to build the simulation model. MATLAB Simulink is a program five to nine level for modeling, simulation and analysis. It supports of systems, as in the time of linear time samples and non-linear, constant. For modeling, Simulink provides construction models and diagrams. Control block generates a PWM signal is given to the new level inverters for reduce total harmonic distortion can be calculated using equations

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_2} \quad (1)$$

Where: H_1 is the amplitudes of the fundamental component, whose frequency is w0 and *Hn* is the amplitudes of the nth harmonics at frequency nw0.

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \quad (2)$$

Let $H_{(n)} = h_n$ and $H_{1} = h$,

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{1}{n} \sum_{k=1}^{s} \cos(n\alpha)\right)^2}}{\sum_{k=1}^{s} \cos(n\alpha_k)} \quad (3)$$

The generations of gating signals with sinusoidal Pulse Width Modulation SPWM are shown in Figure a. there are sinusoidal reference waves (V_{ra}, V_{rb} and V_{rc}) each shifted by 120^o. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signal for that phase. Comparing the carrier signal with the reference phase V_{ra}, V_{rb} and V_{rc} produces g1, g2 and g5 respectively as shown in Figure b.

The instantaneous line to line output voltage is V_{ab}=V_s (g1 - g2) the output voltage as shown in Figure c, is generated by eliminating the condition that two switching devices in the same arm cannot conduct at the same time. The normalized carrier frequency *cf* should be odd multiple of three.

Thus, all phase-voltage (V_{aN}, V_{bN} and V_{cN}) are identical, but 120^0out of phase without even harmonics; moreover harmonics at frequency multiple of three are identical in amplitude and phase in all phase. For instance, if the ninth harmonics voltage in phase is:

$$v_{aN}9 = v^{\sim}9\sin(9\omega t) \quad (4)$$

The corresponding ninth harmonics in phase b will be,

$$v_{aN}9\,(t) = v^{\sim}9\sin(9\omega t - 120) = v^{\sim}9\sin(9\omega t - 1080) = v^{\sim}9\sin(9\omega t) \quad (5)$$

Thus, the ac output line voltage V_{ab} = V_{aN}- V_{bN} does not contain the ninth harmonics. Therefore, for odd multiples of three times the normalized carrier frequency *mf* , the harmonics in the ac output voltage appear at normalized frequency *fh* centered around *mf* and its multiple, specifically, at

$$n = jmf \pm k \quad (6)$$

$$n = jmf \pm k \pm 1 \quad (7)$$

The considered a good quality of the output voltage if the modulation index (MI) in the range of 0 to 0.95. In the case of MI is greater than 0.95, there is a direct correlation between the anti-wave quality and amplitude of the output voltage if the quality decreases and then increases the output voltage wave size. SPWM technology has its limitations regarding the maximum voltage that can be achieved, and the transfer of power.

In the case of a three-phase inverter, the proportion of the main ingredient to the line of maximum possible line voltage to a DC supply voltage is 86.6% and this indicates the use of poor the DC power supply. Sinusoidal (SPWM) is an effective way to reduce the lower harmonics of the system while varied output voltage. However, the low-frequency harmonic content is a minimum value.

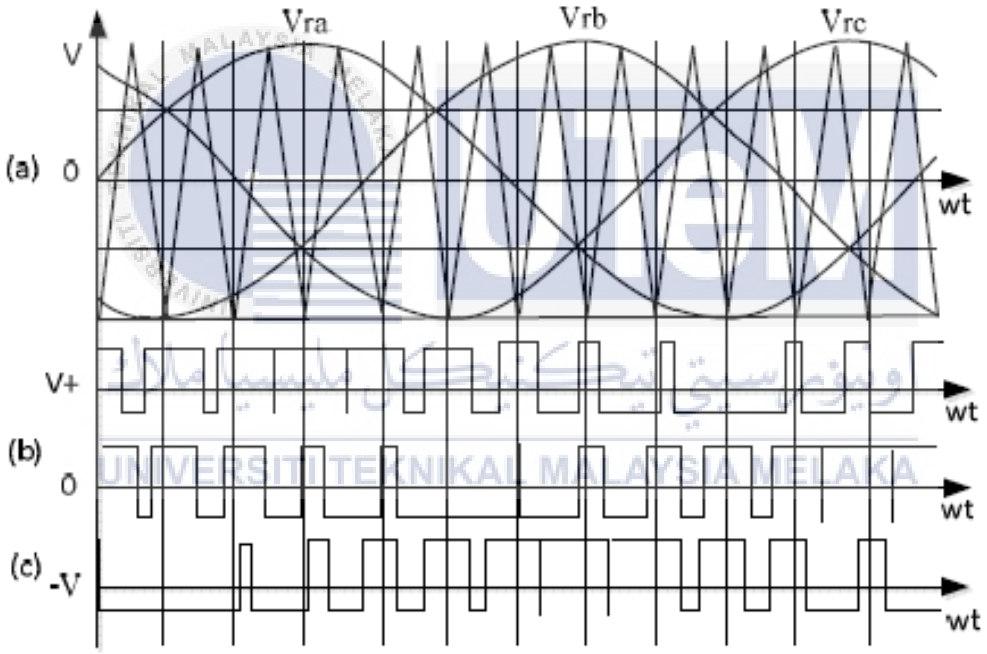

Figure 2.12: Sinusoidal Pulse Width Modulation for Three Phase Inverter [12].

2.9 Summary and discussion of the review

In this project, a modeling of a cascaded H-Bridge multilevel inverter based on supercapacitor for harmonic reduction will be design by changing the DC supply. Besides that, the performance output of this project will be monitor by comparing the previous work that has been done.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Principle of the methods or techniques use in previous work

There are so many types of energy storage applied to the cascaded H-Bridges multilevel inverter such as solar cell, direct current (DC) voltage source, batteries and many more. All those direct current (DC) voltage source that study by the previous researcher so far has no detail research and discussion about the source that apply to the cascaded H-bridge multilevel inverter [13],[14].

3.2 Description the work to be undertaken

3.2.1 Flow Chart

The flow of this project is showed in Figure 3.1. At first, after the selection of the final year project topic is done, the researchers about the a study of cascade H-Bridge multilevel inverter based on supercapacitor for harmonic reduction topic and literature review done first in order to understand more details about the overall key point of this study. This research focused about the how to reduce harmonic by using cascade H-Bridge multilevel

inverter based on supercapacitor. Figure 3.1 shows in detail about the flow of the project in the Final Year Project until Final Year Project 2

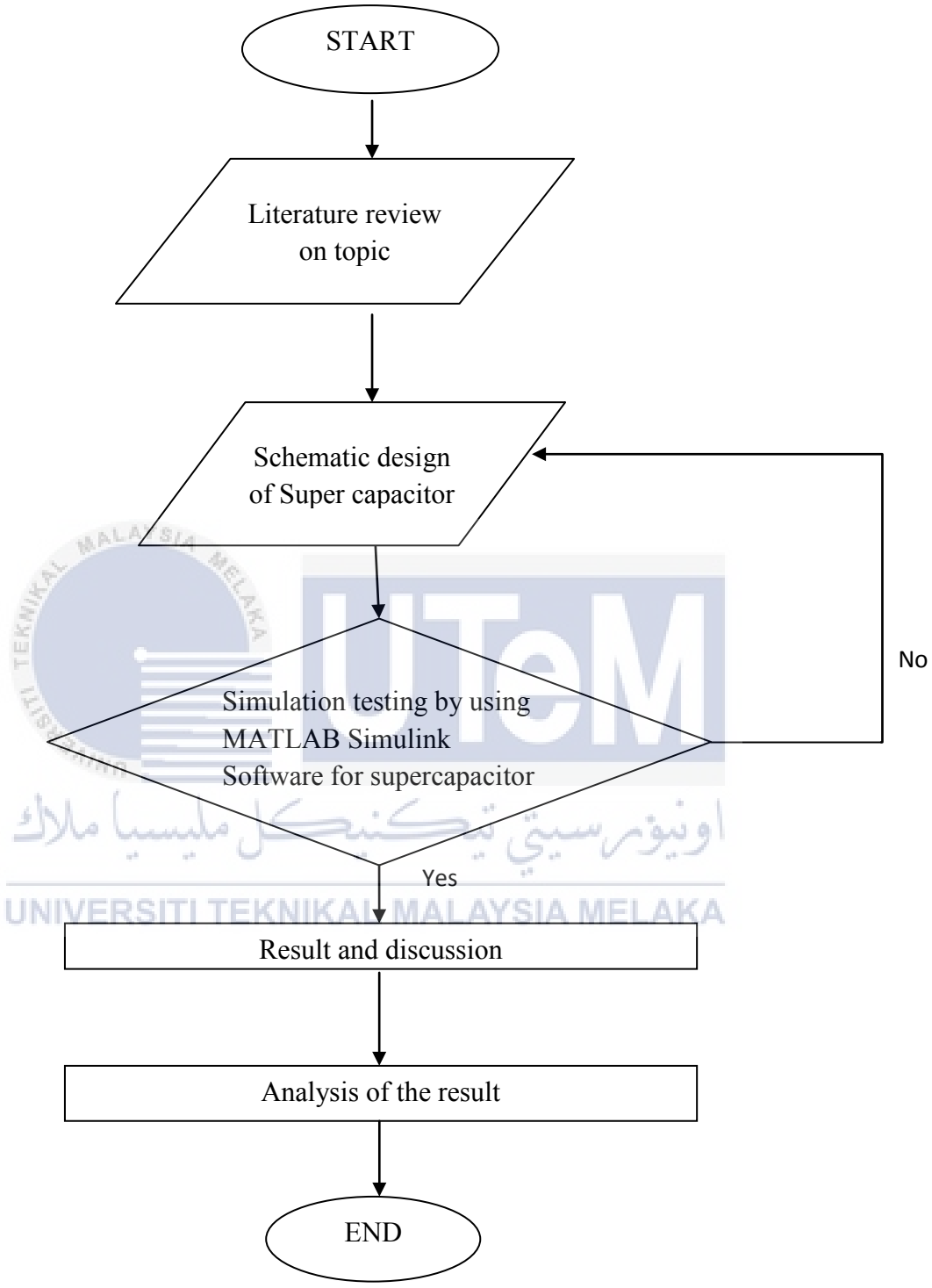

Figure 3.1: Project Flow Chart

3.3 Discussion on selected techniques and approach used

3.3.1 Modeling and simulation of a cascaded H-Bridge multilevel inverter by using MATLAB SIMULINK.

In this chapter, the principle of the methods or techniques use in previous work is using seven-level cascaded H-Bridge multilevel inverter based on 100V direct current (DC) voltage source [14]. From the FYP 1, this project only focused on monitoring the performance of the seven-level cascaded H-Bridges multilevel inverter. In FYP2, The direct current (DC) voltage source used in this seven-level cascaded H-Bridge multilevel inverter had been replaced with supercapacitor and monitors its performance.

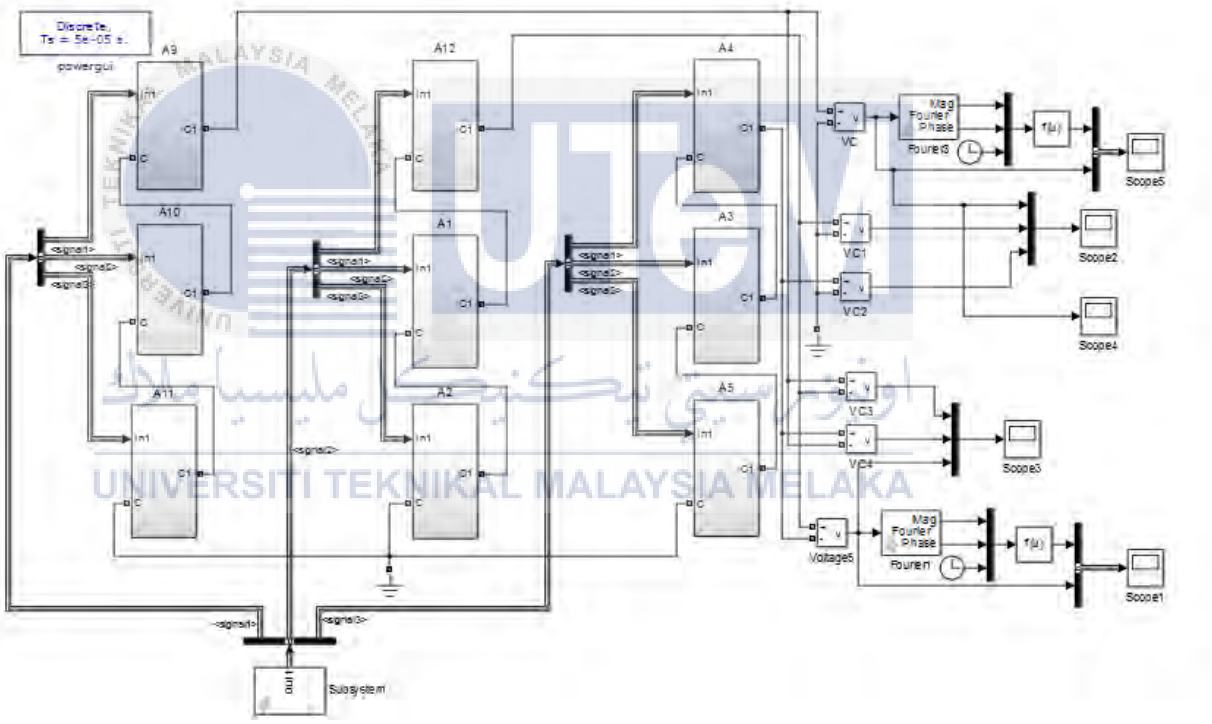

Figure 3.2: Modeling seven-level cascaded H-Bridge multilevel inverter by using MATLAB SIMULINK.

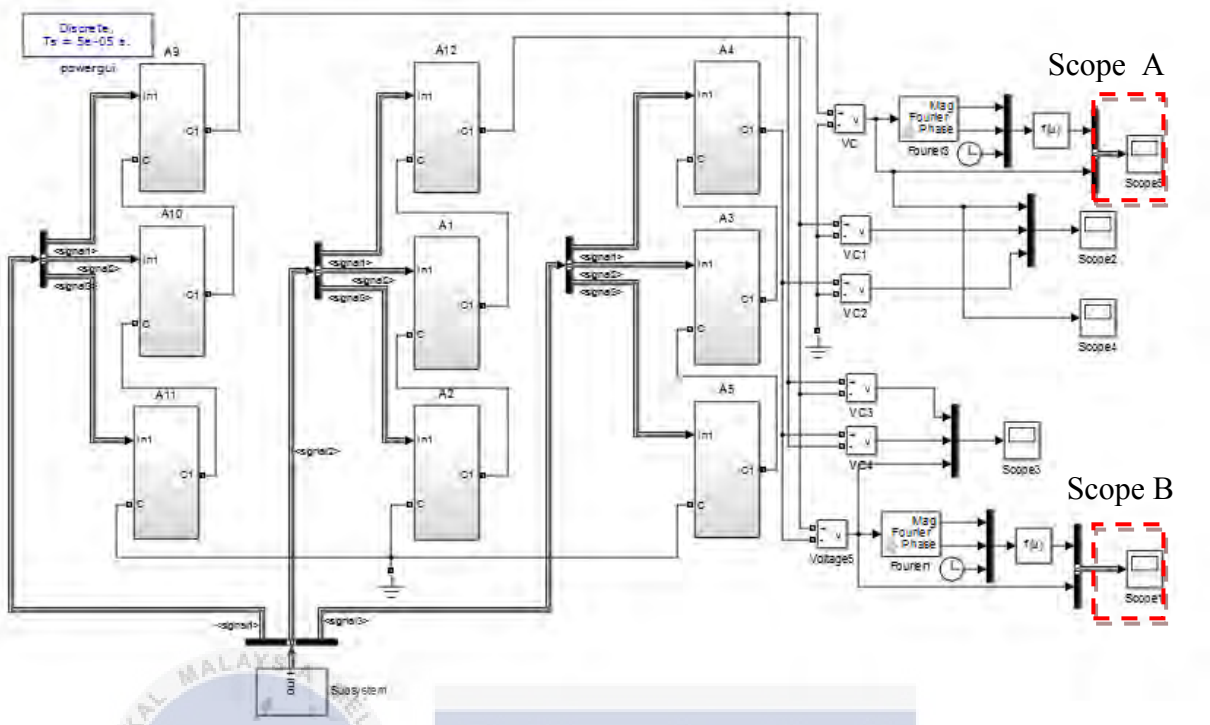

Figure 3.3: Scope for seven-level cascaded H-Bridge multilevel inverter by using MATLAB SIMULINK

Figure 3.3 show the scope for seven-level cascaded H-Bridge multilevel inverter by using MATLAB SIMULINK. It consist line to phase voltage scope A at top of figure at line to line voltage scope B at the bottom of the figure.

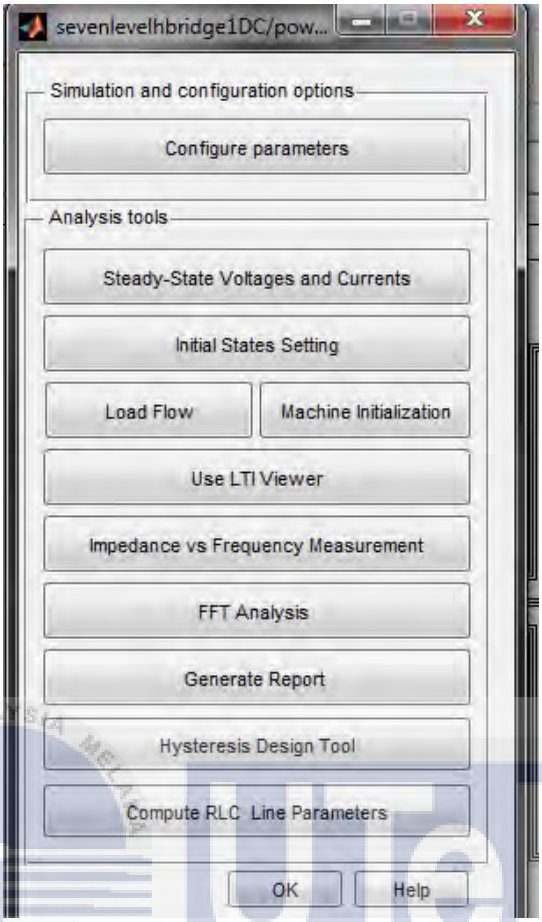

Figure 3.4: Analysis Tools in powergui

Figure 3.4 shows the analysis tools that use in MATLAB SIMULINK for this project; the Fast Fourier (FFT) Analysis tool is selected. It is use to see the signal waveform and Total Harmonic Distortion (THD) as shown at Figure 3.5 and Figure3.6.

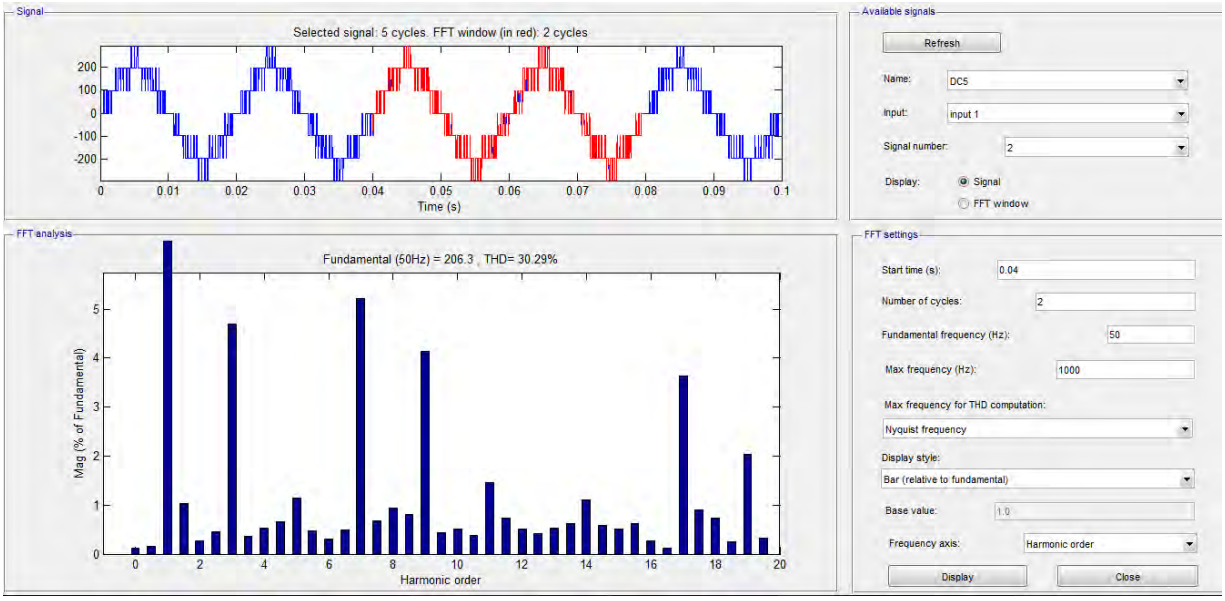

Figure 3.5: Simulation of seven-level cascaded H-Bridge multilevel inverter signal by using Fast Fourier (FFT) Analysis Tool.

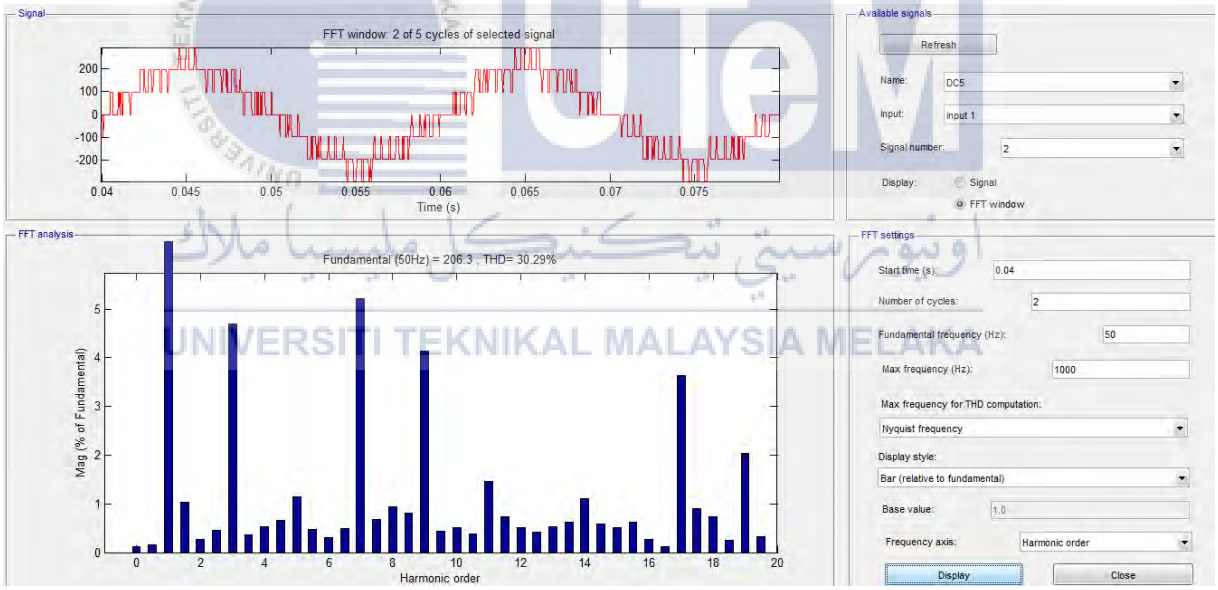

Figure 3.6: Simulation of seven-level cascaded H-Bridge multilevel inverter FFT window by using Fast Fourier (FFT) Analysis Tool

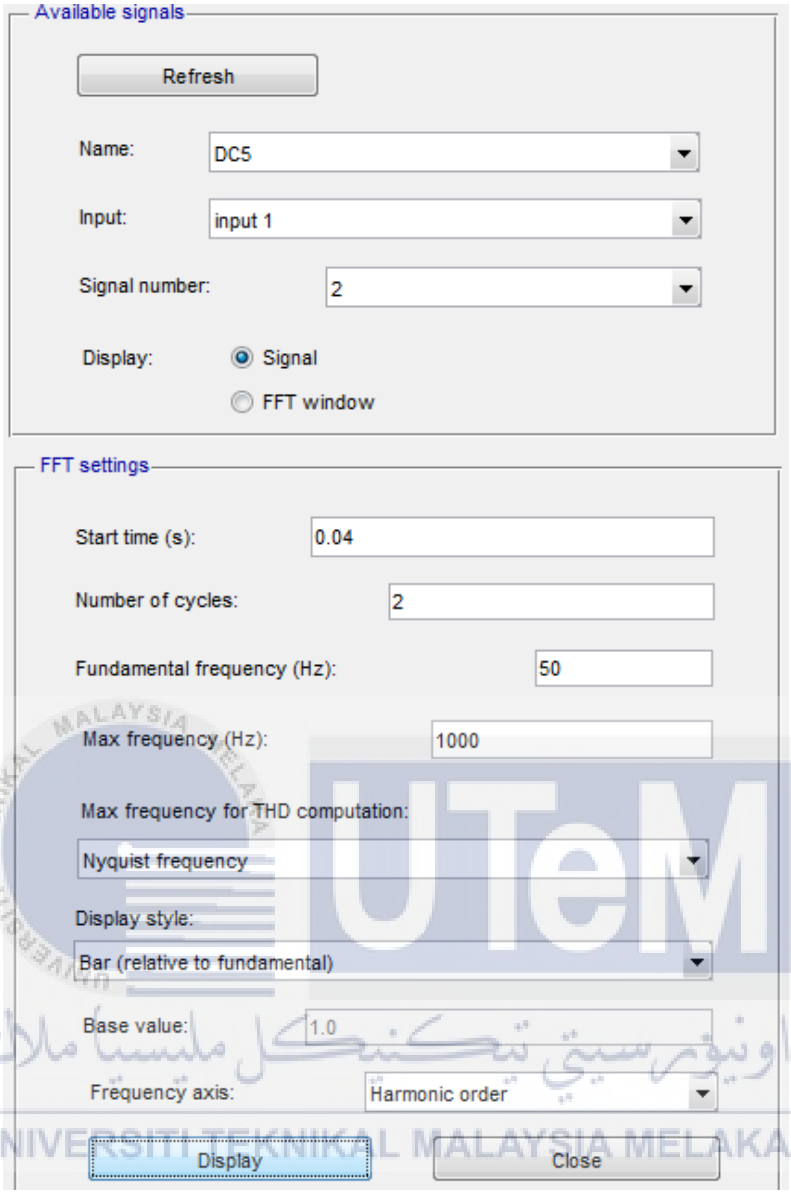

Figure 3.7: Available signal and FFT settings in FFT Analysis tools

Figure 3.7 show the available signal that set for the scope for the DC supply and Super capacitor to monitor the waveform. The signal number is the signal that has in the waveform such as voltage reference and harmonic. In FFT setting, this project is set 0.04 second for DC supply and 0.3 second for super capacitor.

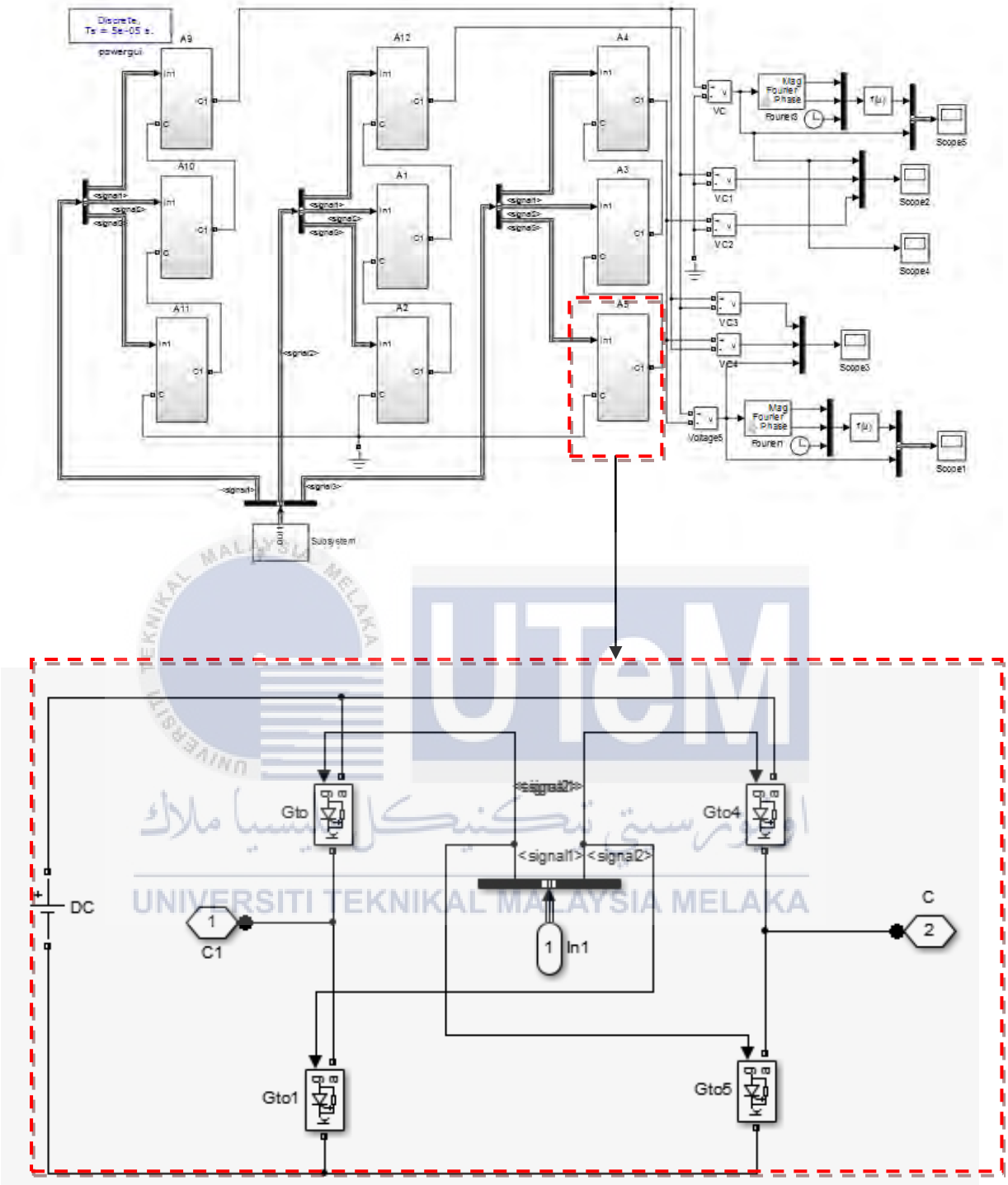

Figure 3.8: Schematic Diagram inside the cascaded H-Bridge multilevel inverter

Figure 3.8 show that component in each block with 100V direct current (DC) voltage source on the cascaded H-Bridge multilevel inverter. The Gate Turn Off (GTO) Thyristor in this circuit act as switching scheme from direct current (DC) to alternating current (AC) waveform.

3.4 Principle of the methods or techniques use in FYP 2

In this subtopic, the principle of the methods or techniques use in t is using seven-level cascaded H-Bridge multilevel inverter by using supercapacitor in Figure 3.10 as power supply that replace direct current source from previous work.

3.4.1 Modeling Supercapacitor

A supercapacitor can be modeled by using some standard circuit components as shown in Figure 2.11. This circuit design is used because a similar circuit is presented in the data sheet for the supercapacitor from EPCOS and because of recommendations from the project supervisor [10]. By adding more components until the circuit described in Figure 3.9 is achieved, the accuracy of the model is improved.

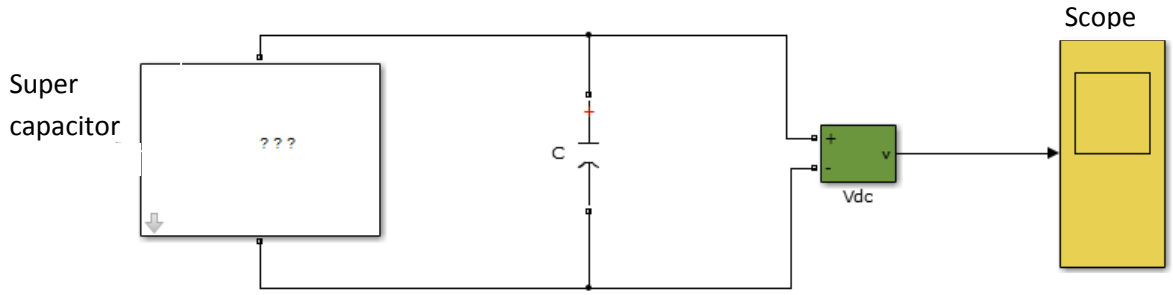

Figure 3.9: Modeling Supercapacitor by using MATLAB SIMULINK

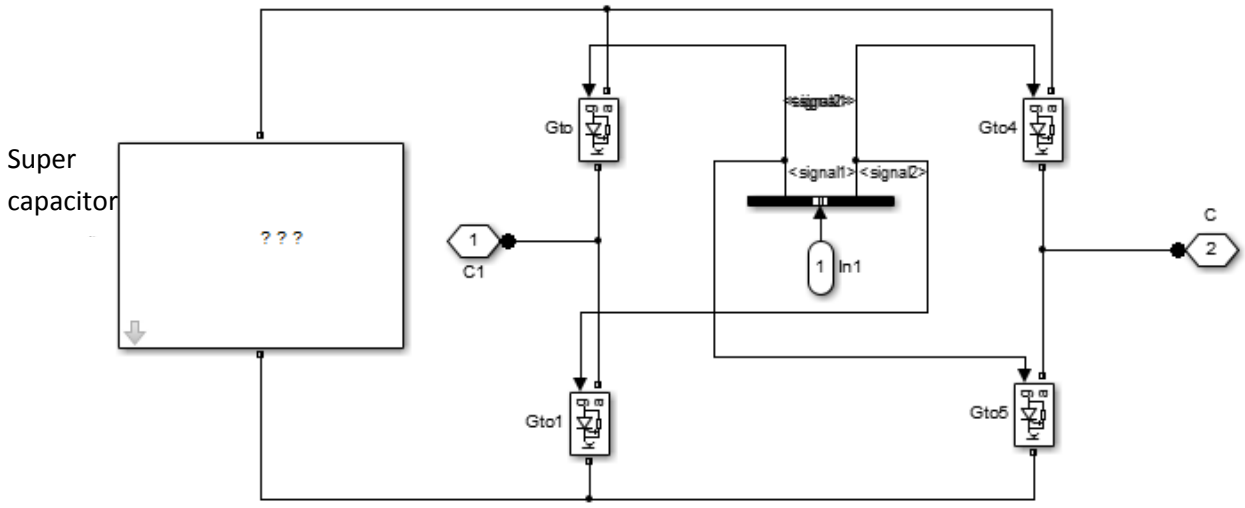

Figure 3.10: Schematic Diagram of Supercapacitor and switching by using MATLAB SIMULINK

Figure 3.10 show that component in each block with super apacitor as a power supply on the cascaded H-Bridge multilevel inverter. The Gate Turn Off (GTO) Thyristor in this circuit act as switching scheme from direct current (DC) to alternating current (AC) waveform.

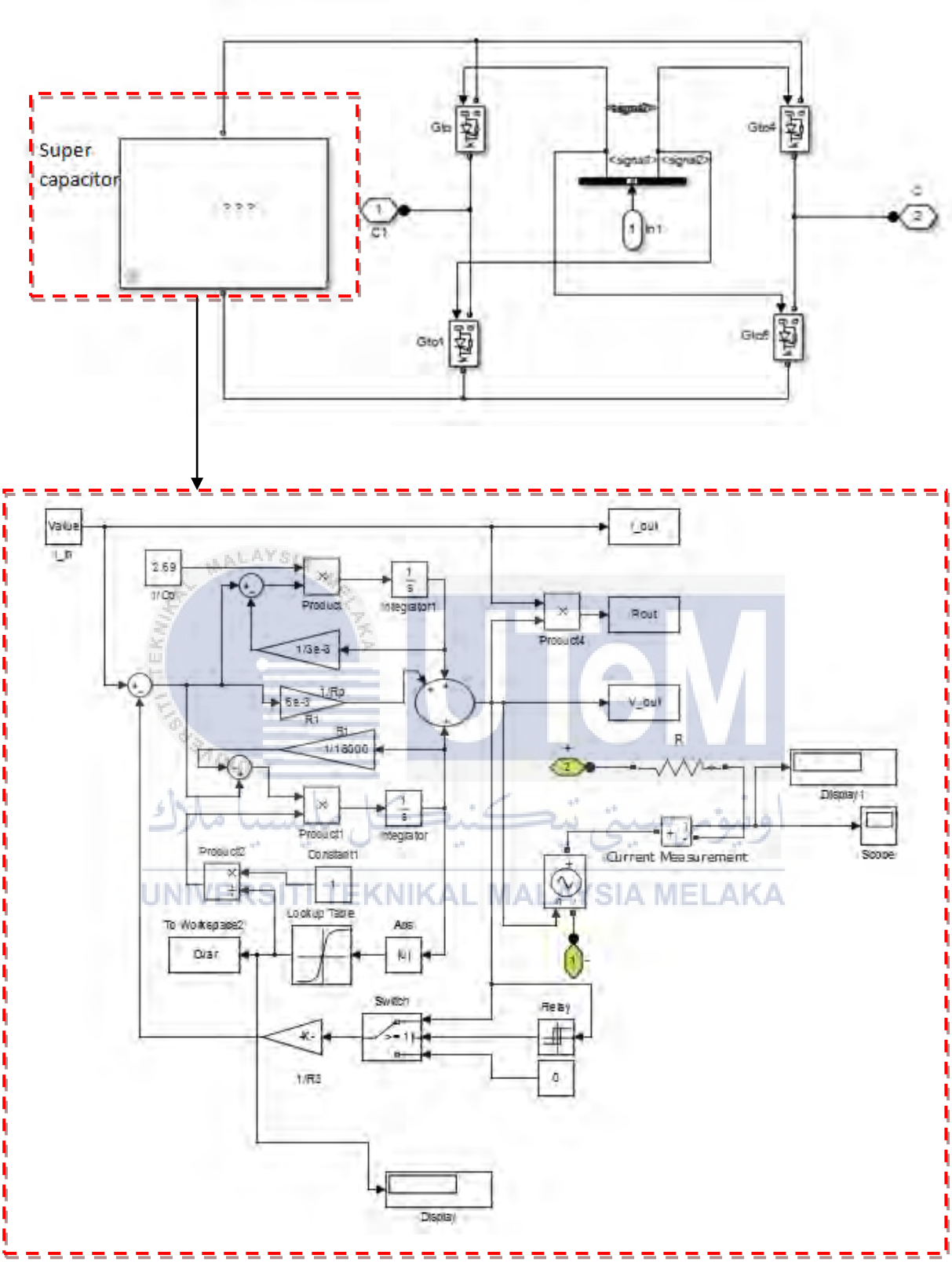

Figure 3.11: MATLAB SIMULINK model of supercapacitor

This block diagram that is used considered the basic model of the supercapacitor as shown in Figure 3.12. The controls blocks relay the switch that connects the resistance balancing *R3* to the circuit [15]. To calculate *R1, R3*, lookup table to be determined by using:

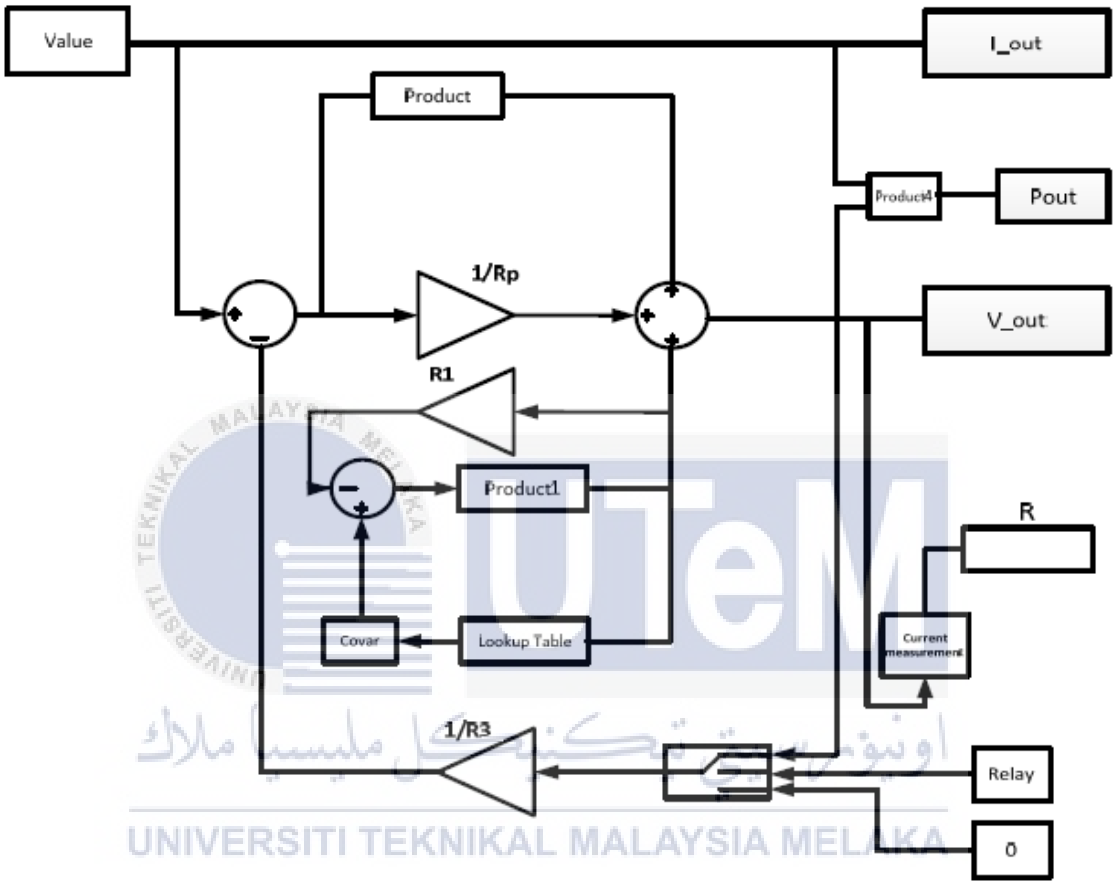

Figure 3.12: Block Diagram of supercapacitor

When high currents are used, other effects than the capacitance can affect the voltage level. These effects can cause the calculated capacitance value to be incorrect [16].

$$Q = I(t)\,dt \qquad (4)$$

Where; Q = stands of charge,

The charge in a capacitor can be calculated using the integral of the current during one charging cycle [17]. The capacitance value can then be calculated using:

$$C = \frac{\Delta Q}{\Delta u} \tag{5}$$

Where; Q and u = The differences in charge and voltage [17][18].

3.4.2 Modeling Sinusoidal Pulse Width Modulation (SPWM) Controller.

Control technology is the most popular method of pulse width modulation sine adapter's two traditional levels. The tem sinusoidal PWM reference is made to the production of the PWM output signal with a sine wave as a modulation signal [19]. The on and off instants of a PWM signal ill this case, can be determined by comparing the sinusoidal signal (wave modulation) with a triangular wave frequency (carrier wave), as shown in Figure 3.13 sinusoidal PWM technology is commonly used in industrial applications and abbreviated here as SPWM [20]. Frequency of the modulating wave determines the frequency of the output voltage. The enlargement of the height of the modulation index of the waveform and determines the composition turn control the RMS value of the output voltage [21].

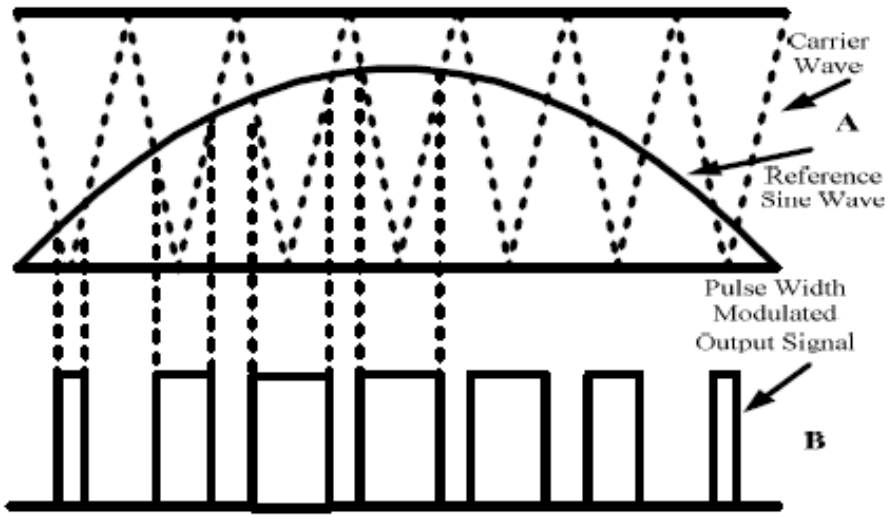

Figure 3.13: Sinusoidal Pulse Width Modulation [21]

The RMS value of the output voltage can be varied by changing the modulation index. The output voltage of the inverter contains harmonics. However, to be paid for the harmonics of the band around the carrier frequency and its complications [22].To perform sinusoidal PWM using analog circuit, use a series of bricks:

(1) High-frequency triangular wave generator.
(2) Sine wave generator.
(3) Comparator.
(4) Inverter circuits with dead-band generator to generate complimentary driving Signals with required dead band.

Sinusoidal Pulse Width Modulation (SPWM) controller is chosen because this controller is not complex from other controller such as space-vector (SV), step modulation, and selective-harmonic-elimination (SHE). Besides that, it is easy to get lower Total Harmonic Distortion (THD) in this seven-level cascaded H-Bridge multilevel inverter.

In the cascaded topology, this controller is low cost compare with the diode-clamped (DCMC) and flying-capacitor (FCMC), little heat whilst working, lower power consumption, and can utilized very high frequency.

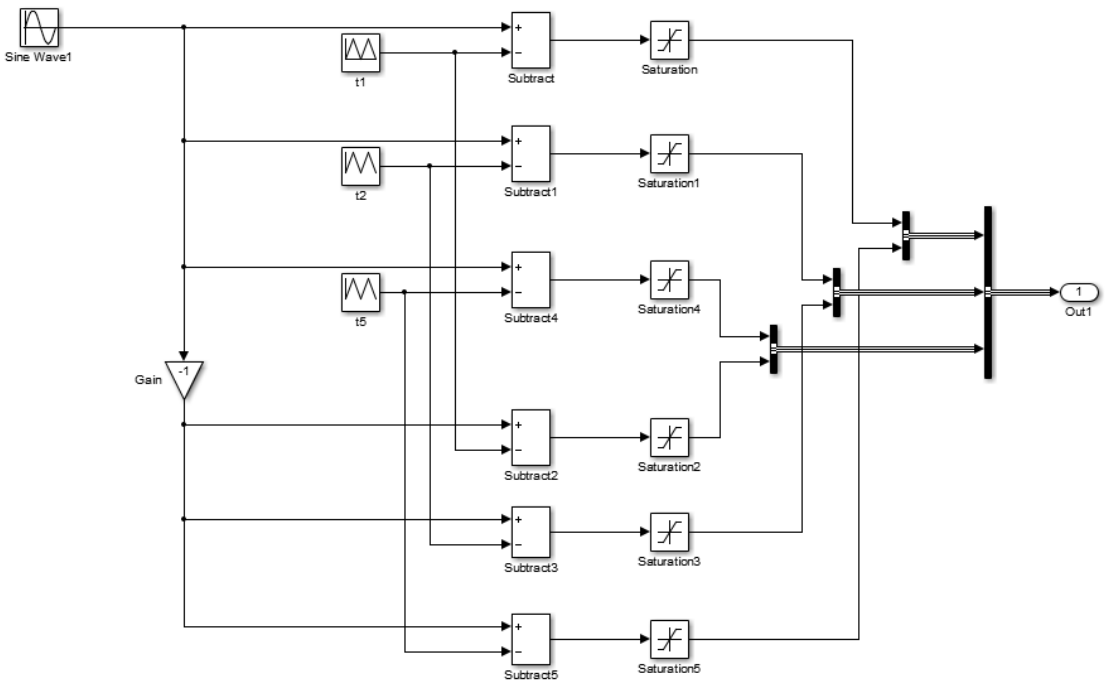

Figure 3.14: Sinusoidal Pulse Width Modulation (SPWM) Controller for seven-level cascaded H-Bridge multilevel inverter.

Figure 3.14 show that the Sinusoidal Pulse Width Modulation (SPWM) Controller connected to output 1. Output 1 is the input to inject the signal to the Gate Turn Off (GTO) Thyristor to make switching to get sinusoidal waveform.

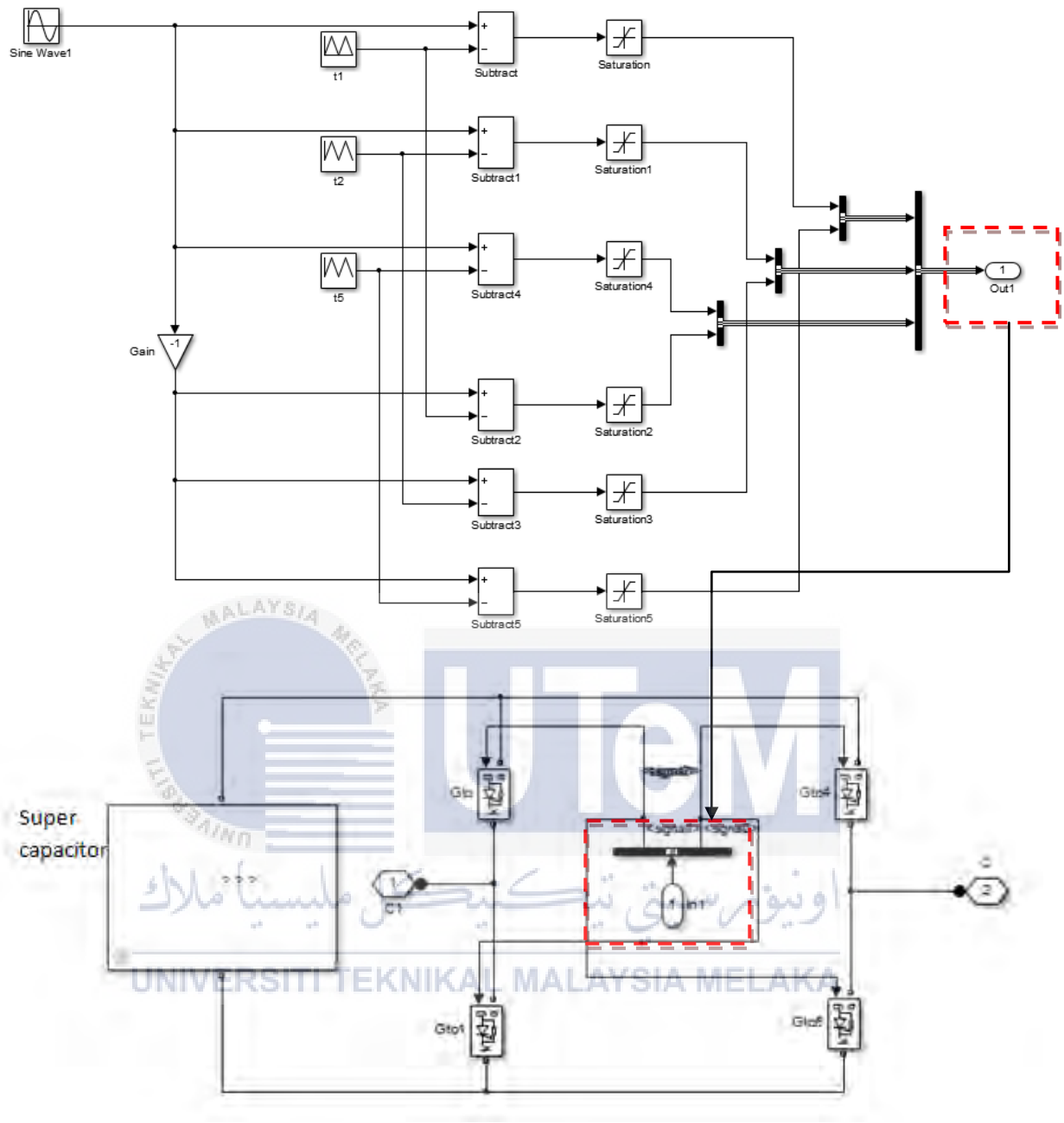

Figure 3.15: Output from SPWM controller

Figure 3.15 show that the output from Sinusoidal Pulse Width Modulation (SPWM) controller injects the signal to the four power transistor that is Gate Turn Off (GTO) Thyristor that act as a switching component to produce a sinusoidal waveform. The supercapacitor gives a voltage supply to the circuit for it to operation.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Project Achievement

This chapter will present the data and result gathered from discussed in preceding chapters. In this work of seven-level cascaded H-Bridge multilevel inverter based are using on sinusoidal pulse width modulation (SPWM) control inverter, a simulation module by MATLAB SIMULINK three phase multilevel inverters, Based on the simulation results, a seven level (odd level) SPWM inverter is presented to alleviate harmonic components of output voltage from DC supply and Super capacitor. Multilevel inverters are applied Gate Turn Off (GTO) Thyristor inverter that act as switching component to generate the sinusoidal waveform which is generating 50 Hz. Selected to carrier frequency 2500 Hz and modulation index equals to 0.5 until 1.0.

4.1.1 Changes makes at power supply

In this project, supercapacitor will replace DC supply as the power supply for the seven-level cascaded H-Bridge multilevel inverter and monitor it performance.

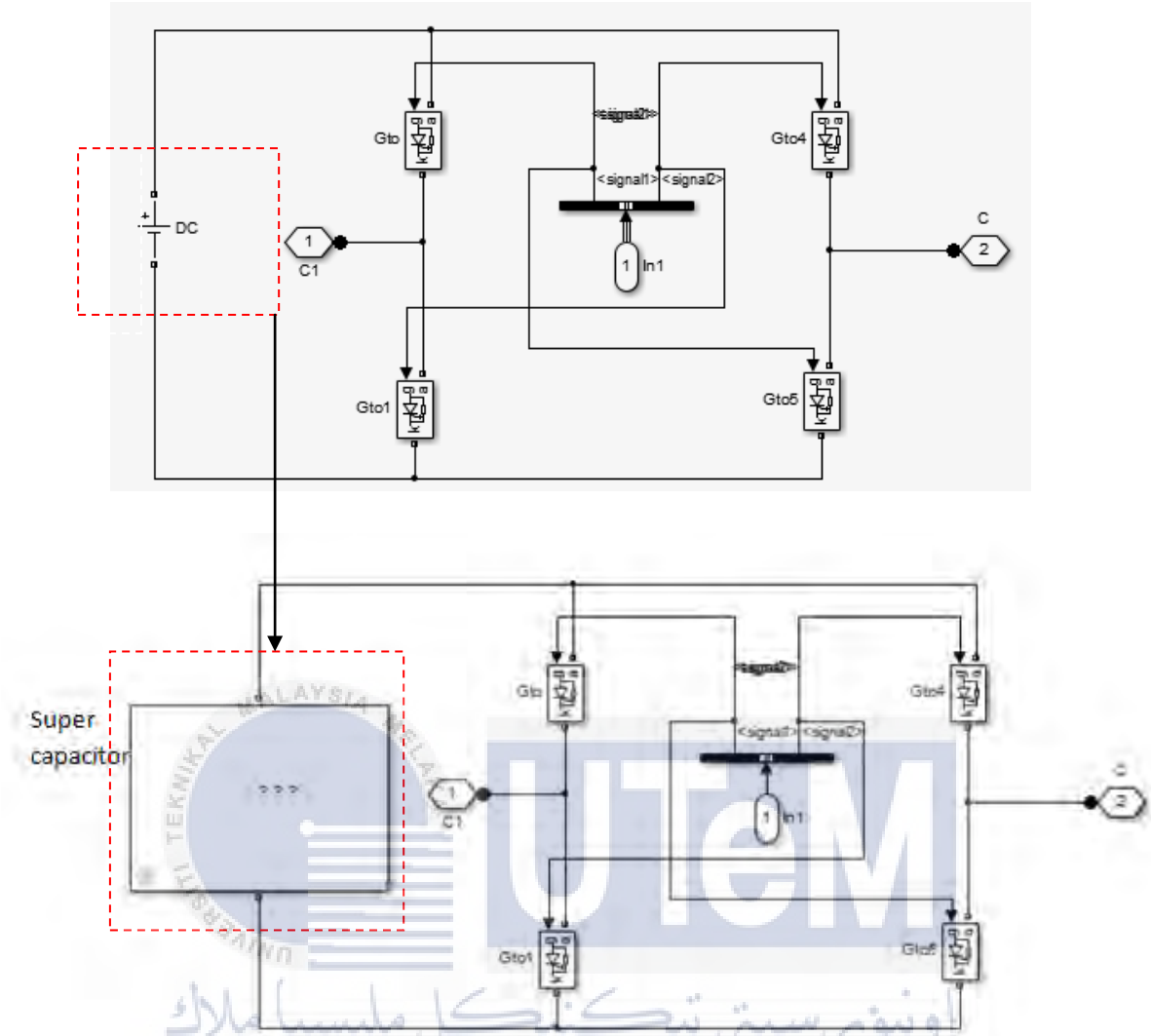

Figure 4.1: Schematic Diagram of power supply

Figure 4.1 shows that the Super capacitor that replaces DC supply as a power supply and switching by using MATLAB SIMULINK.

4.1.2 Performance of supercapacitor

Figure 4.2 show the charging of supercapacitor. The charging process starts from 0 second until 1 second and it show that the voltage stable at 2.6V.

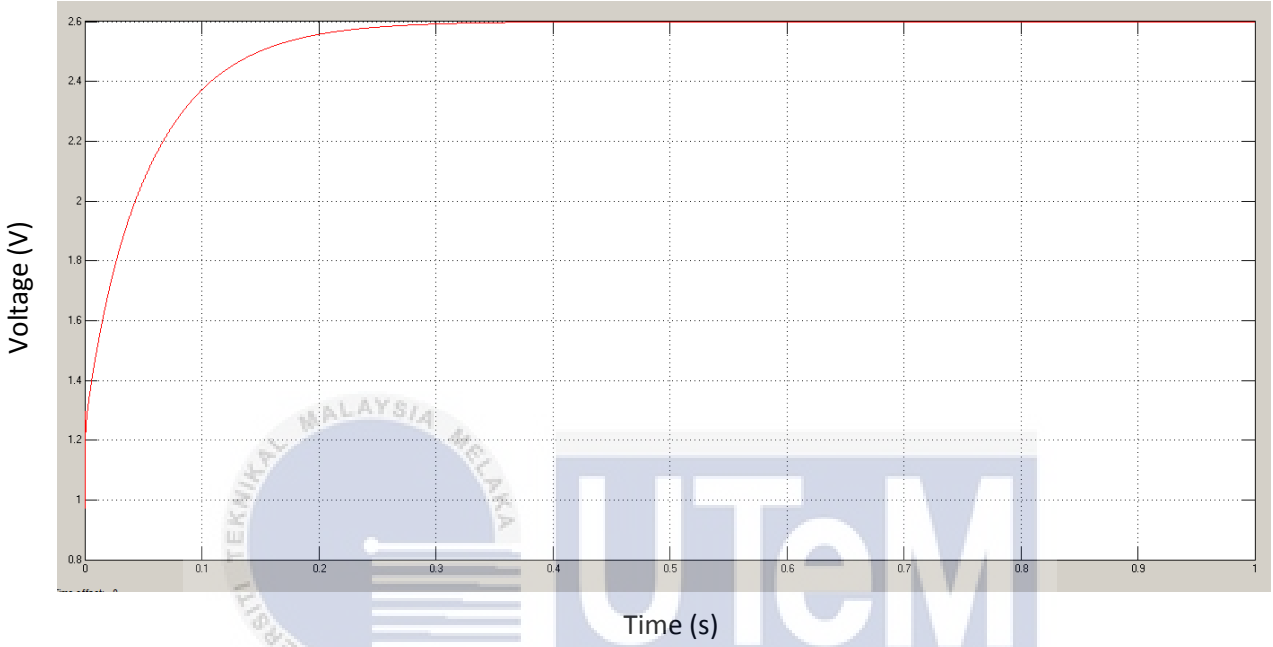

Figure 4.2: Supercapacitor DC voltage

Figure 4.3 show the discharging and charging of supercapacitor. The supercapacitor took 3 seconds to discharge from 2.0V to 0V and it charge back at 3 second after that.

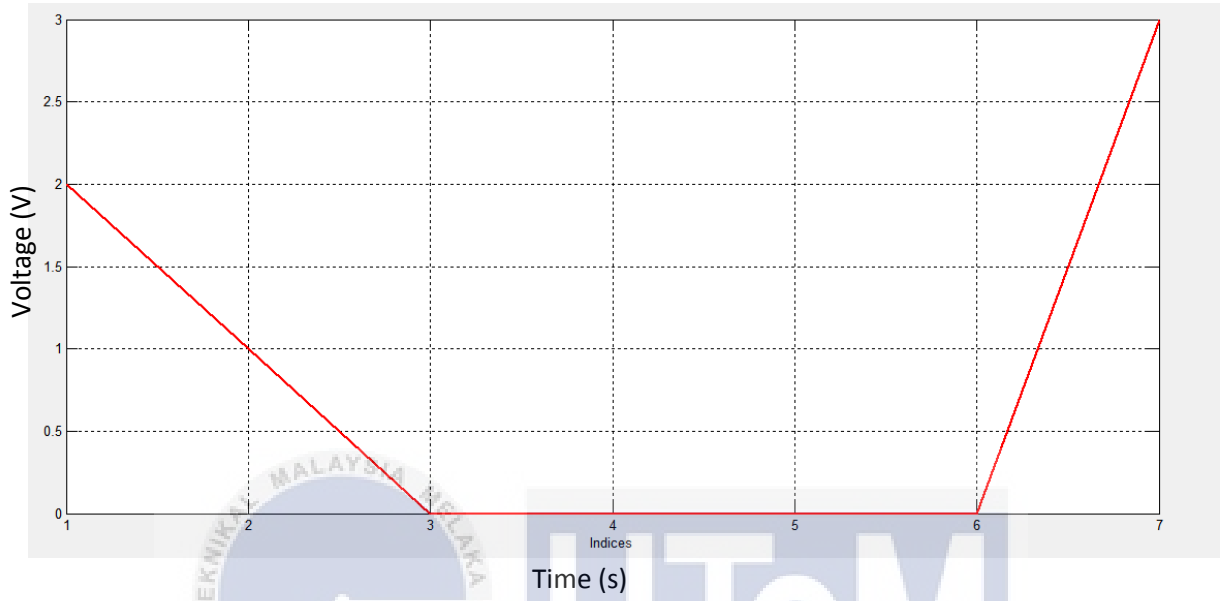

Figure 4.3: Supercapacitor graph when discharging and charging

Figure 4.4 show the charging and discharging of supercapacitor when attached at cascaded H-Bridge multilevel inverter. The duration takes to charge and discharge last for 0.4 seconds.

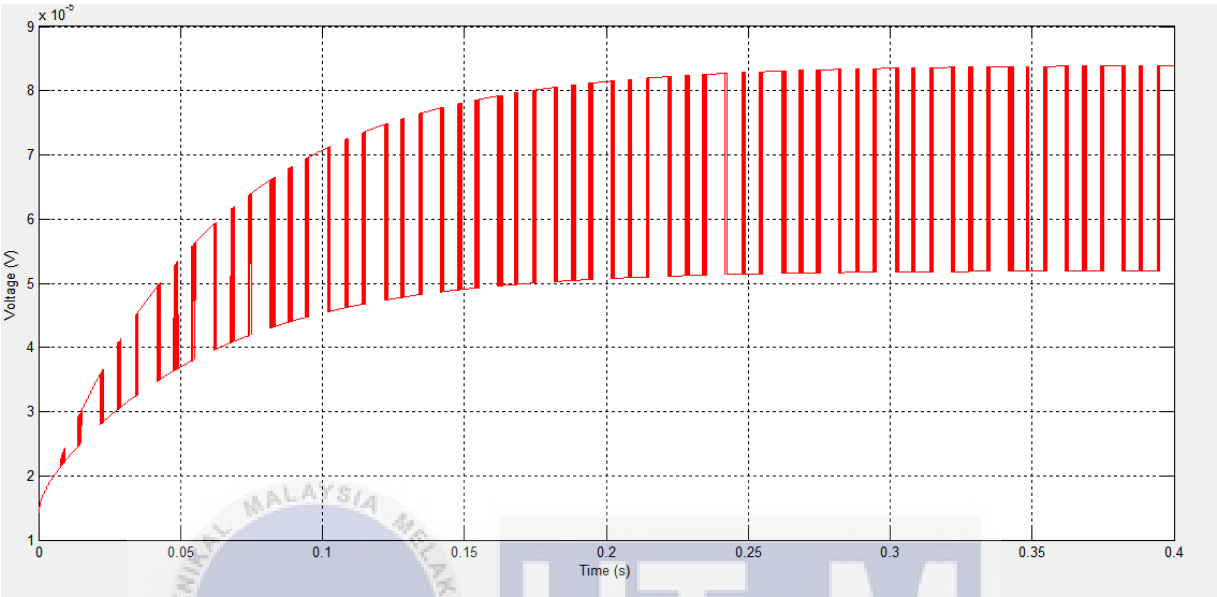

Figure 4.4: Supercapacitor graph charging and discharging when attached at cascaded H-Bridge multilevel inverter

4.1.3 Performance of DC supply applied to the seven-level cascaded H-Bridge multilevel inverter

Figure 4.5 show voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.5. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces five stage of harmonic in the graph at 400Vpp.

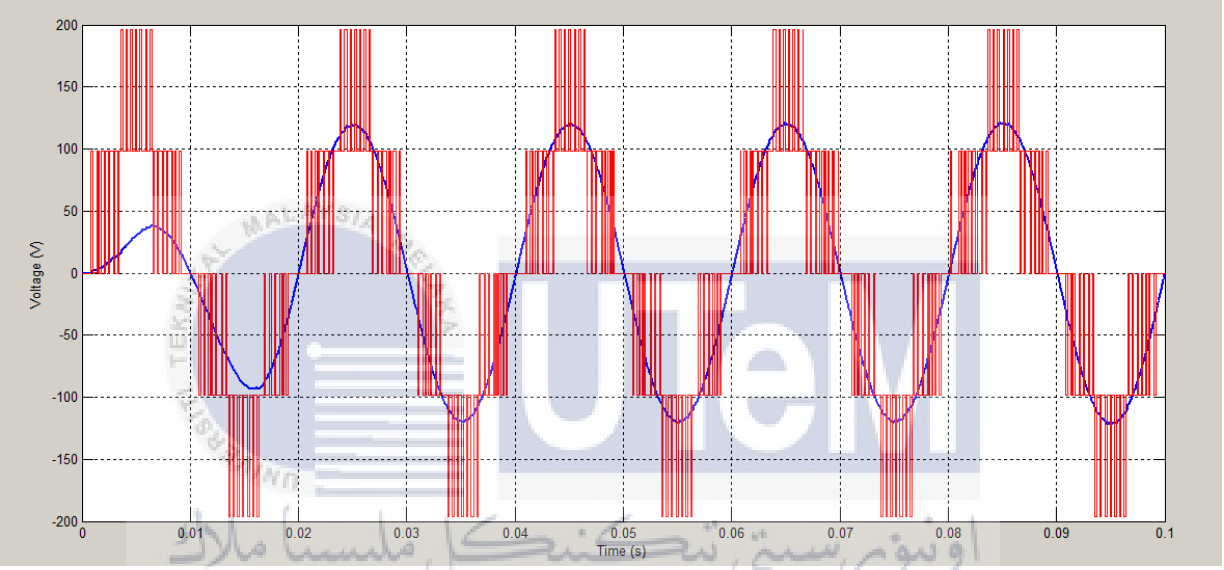

Figure 4.5: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.5 using DC supply

Figure 4.6 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.6. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces five stage of harmonic in the graph at 400Vpp.

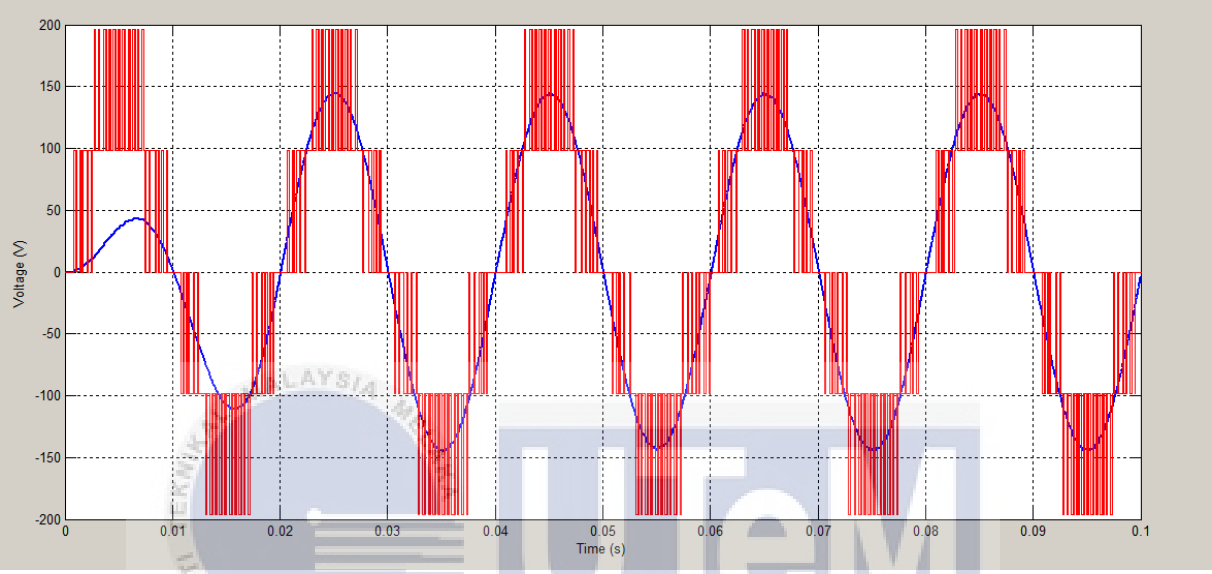

Figure 4.6: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.6 using DC supply

Figure 4.7 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.7. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces five stage of harmonic in the graph at 400Vpp.

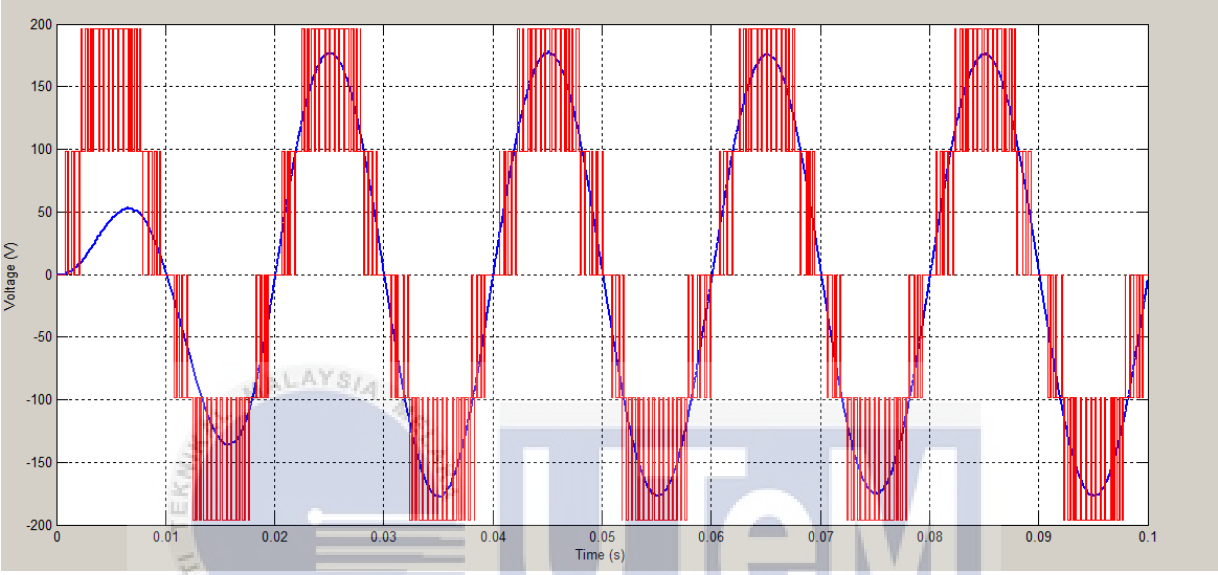

Figure 4.7: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.7 using DC supply

Figure 4.8 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.8. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces seven stage of harmonic in the graph at 600Vpp.

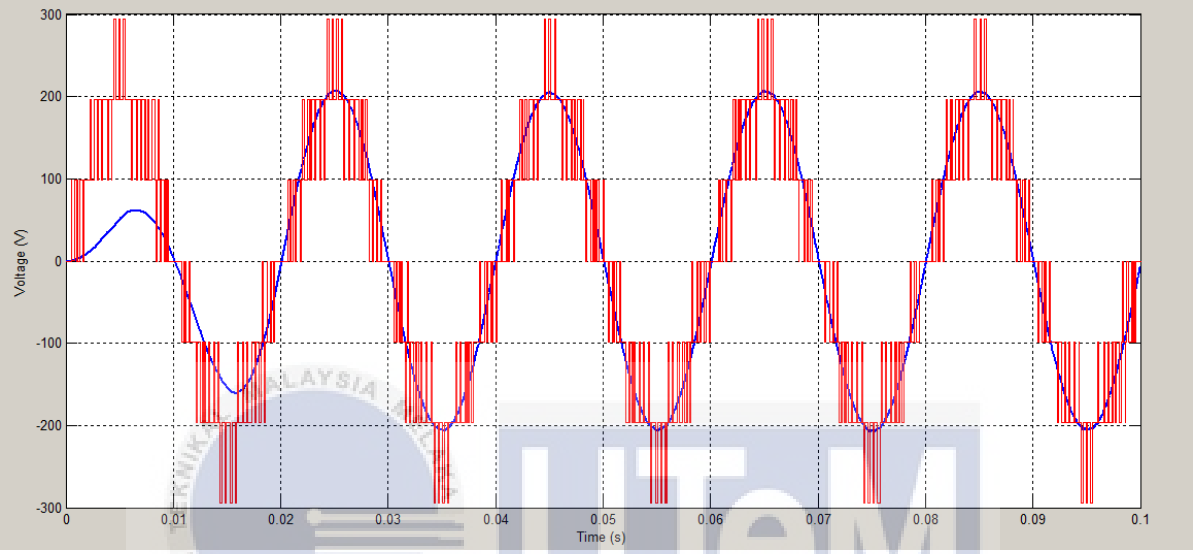

Figure 4.8: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.8 using DC supply

Figure 4.9 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using Dc supply and the modulation index that is set at 0.9. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces seven stage of harmonic in the graph at 600Vpp.

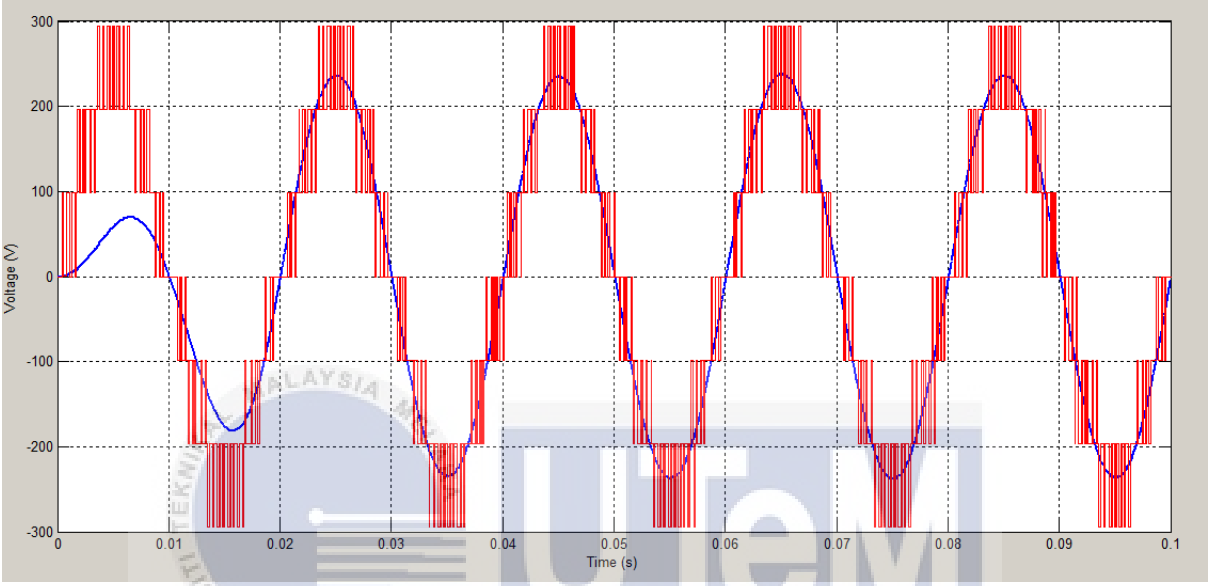

Figure 4.9: Voltage waveform voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.9 using DC supply

Figure 4.9 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter using DC supply and the modulation index that is set at 1.0. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds. It produces seven stage of harmonic in the graph at 600Vpp.

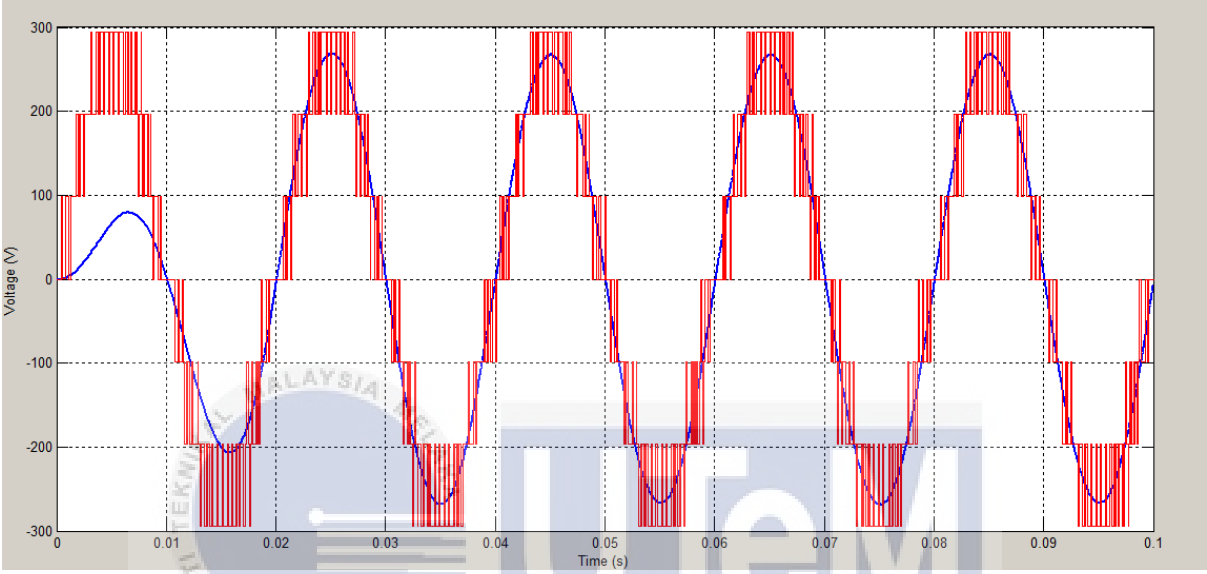

Figure 4.10: Voltage waveform voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 1.0 using DC supply

4.1.4 Performance of supercapacitor applied to the seven-level cascaded H-Bridge multilevel inverter

Figure 4.11 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.5. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second. It produces five stage of harmonic in the graph at 12.4Vpp.

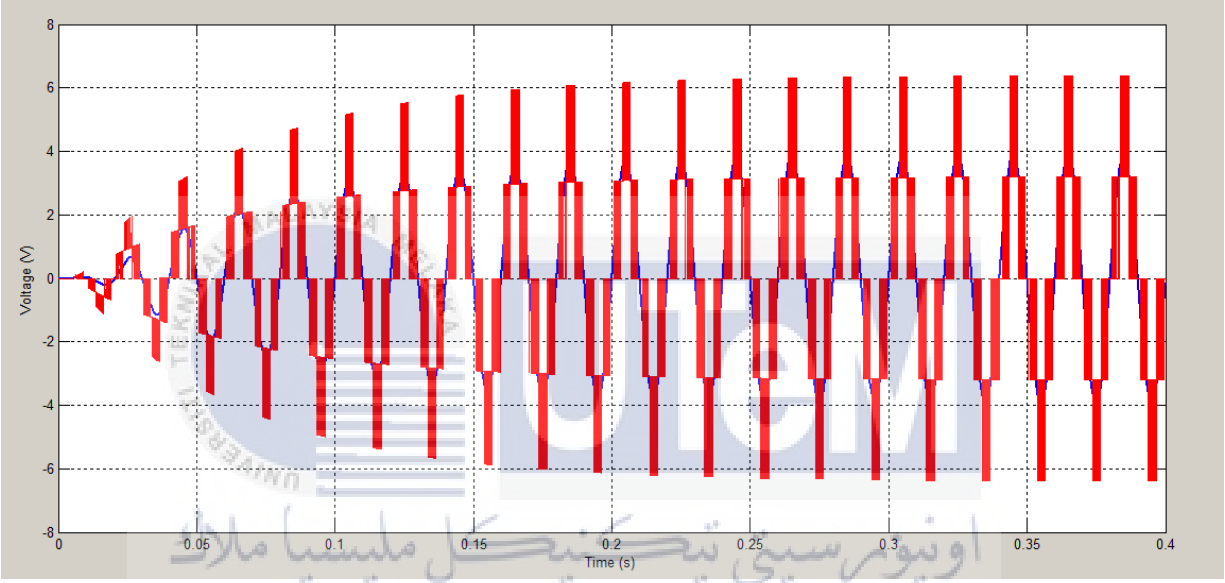

Figure 4.11: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.5 using supercapacitor

Figure 4.12 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.6. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second. It produces five stage of harmonic in the graph at 12.4Vpp.

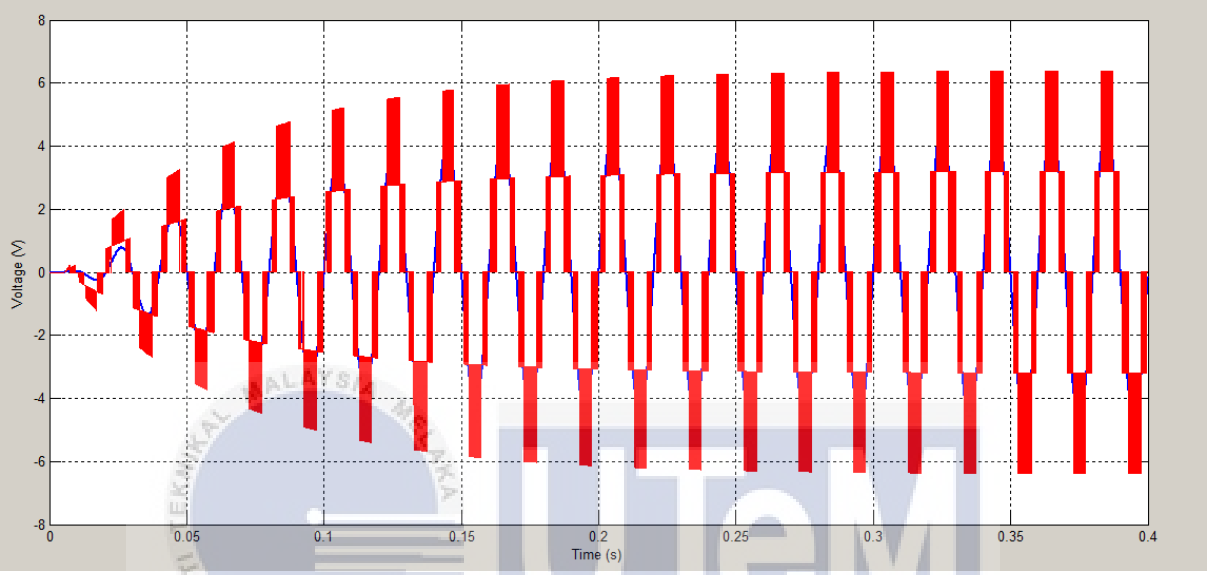

Figure 4.12: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.6 using supercapacitor

Figure 4.13 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.7. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second for super capacitor. It produces five stage of harmonic in the graph at 12.4Vpp.

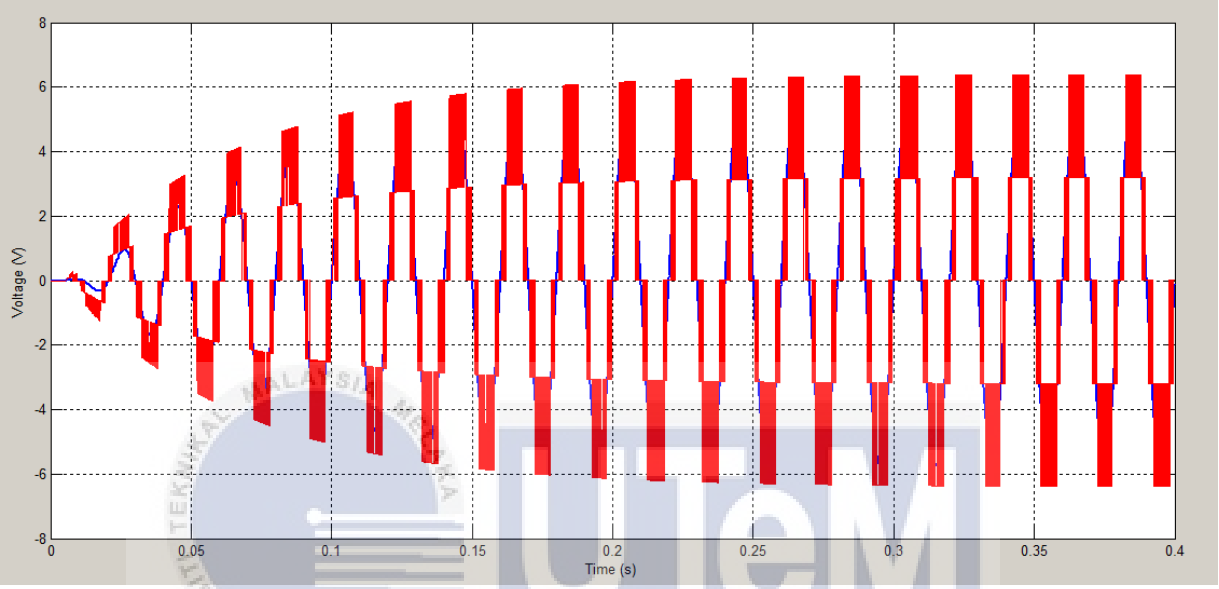

Figure 4.13: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.7 using supercapacitor

Figure 4.14 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.8. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second for super capacitor. It produces seven stage of harmonic in the graph at 18Vpp.

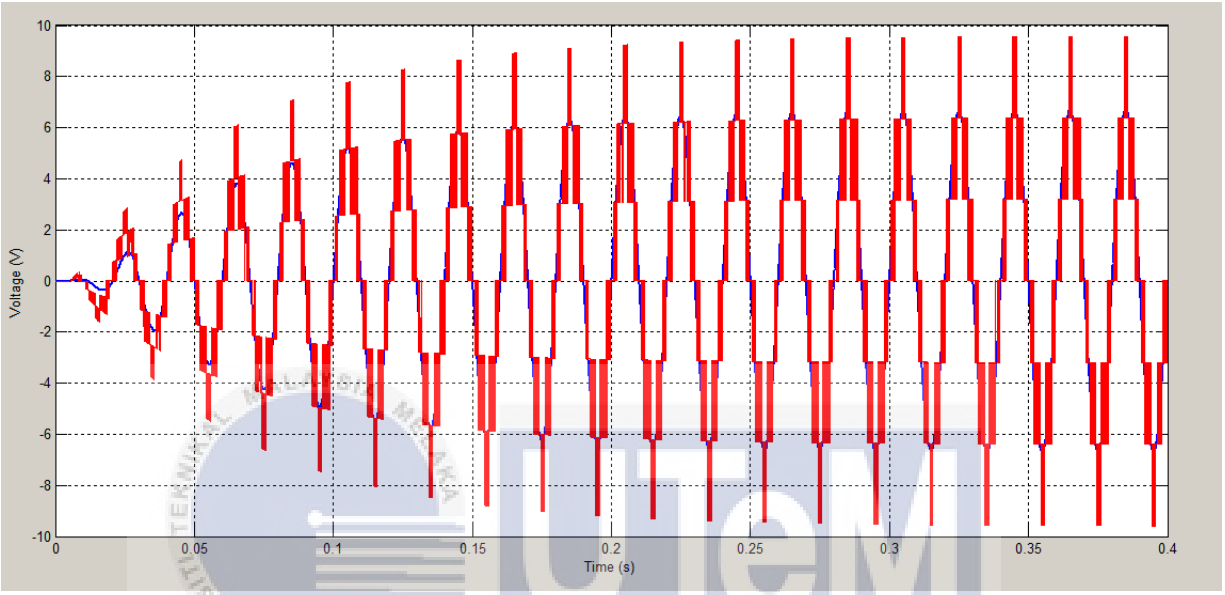

Figure 4.14: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.8 using supercapacitor

Figure 4.15 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.9. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second for super capacitor. It produces seven stage of harmonic in the graph at 18Vpp.

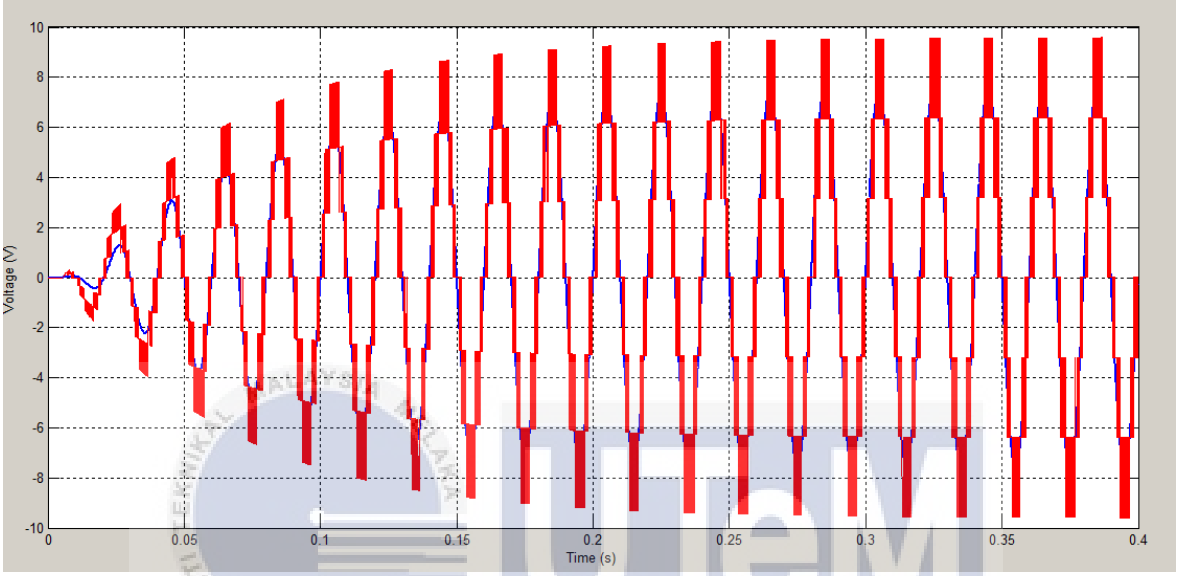

Figure 4.15: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 0.9 using supercapacitor

Figure 4.16 show the voltage waveform at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 1.0. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 second for super capacitor. It produces seven stage of harmonic in the graph at 18Vpp.

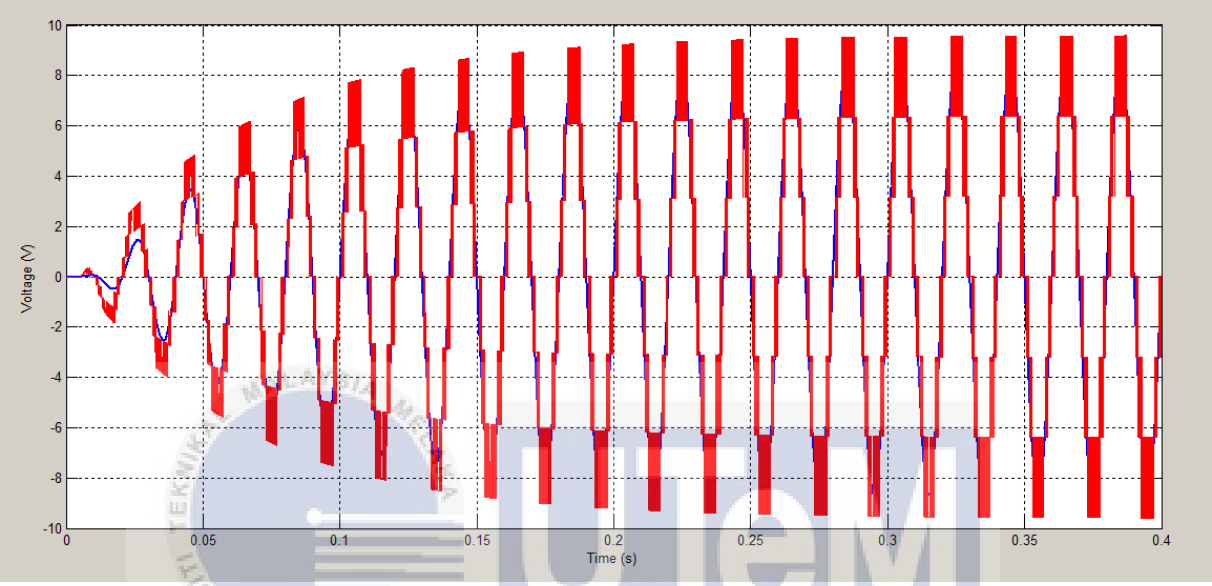

Figure 4.16: Voltage waveform at output seven-level cascaded H-Bridge multilevel inverter which MI= 1.0 using supercapacitor

4.1.5 Harmonic spectrum for Total Harmonic Distortion (THD) voltage based on DC supply.

Figure 4.17 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.5. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 51.72% with 120.2Vrms and 20 harmonic order.

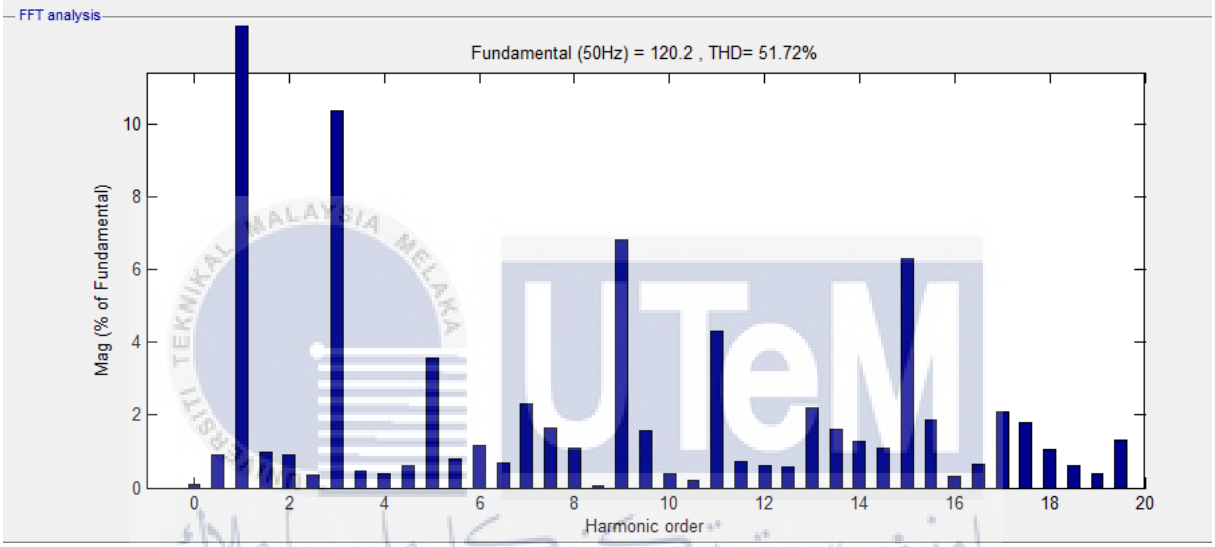

Figure 4.17: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.5 using DC Supply

Figure 4.18 show the harmonic at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.6. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 44.35% with 143.9Vrms and 20 harmonic order.

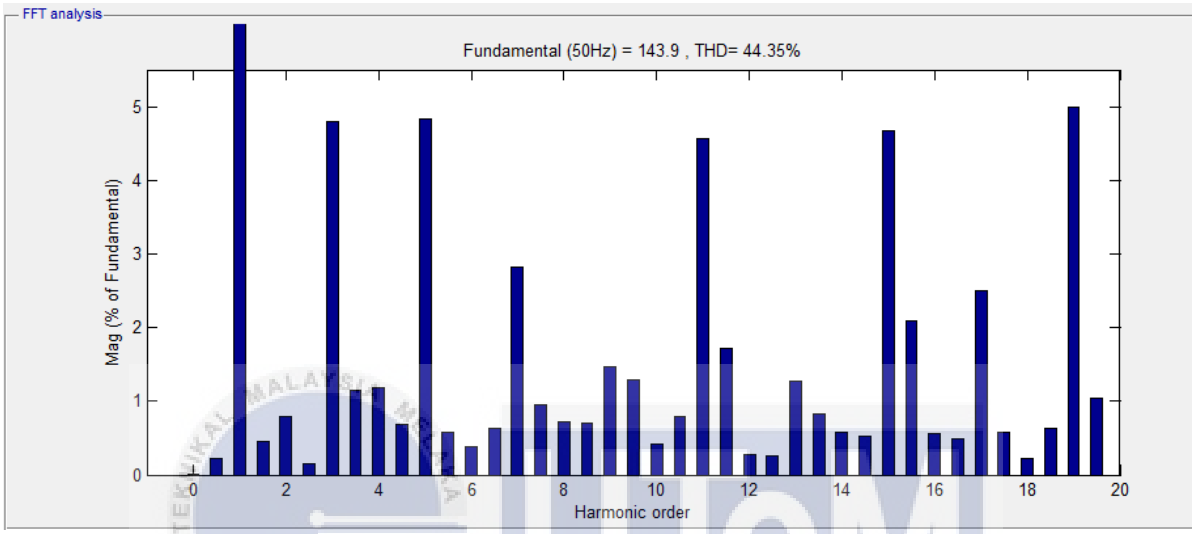

Figure 4.18: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.6 using DC Supply

Figure 4.19 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.7. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 35.19% with 175.6Vrms and 20 harmonic order.

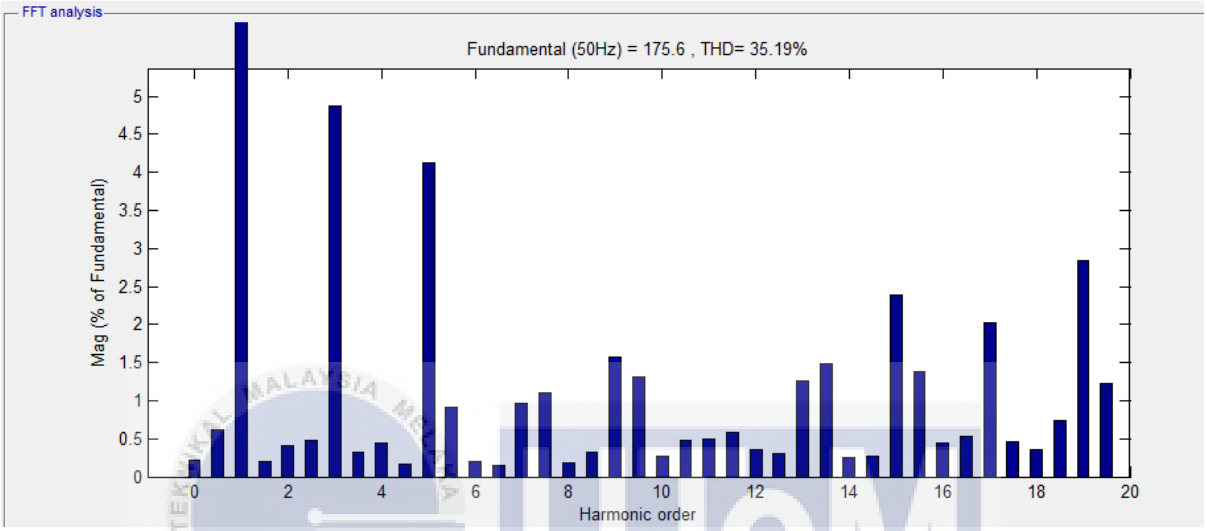

Figure 4.19: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.7 using DC Supply

Figure 4.20 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.8. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 31.67% with 206.1Vrms and 20 harmonic order.

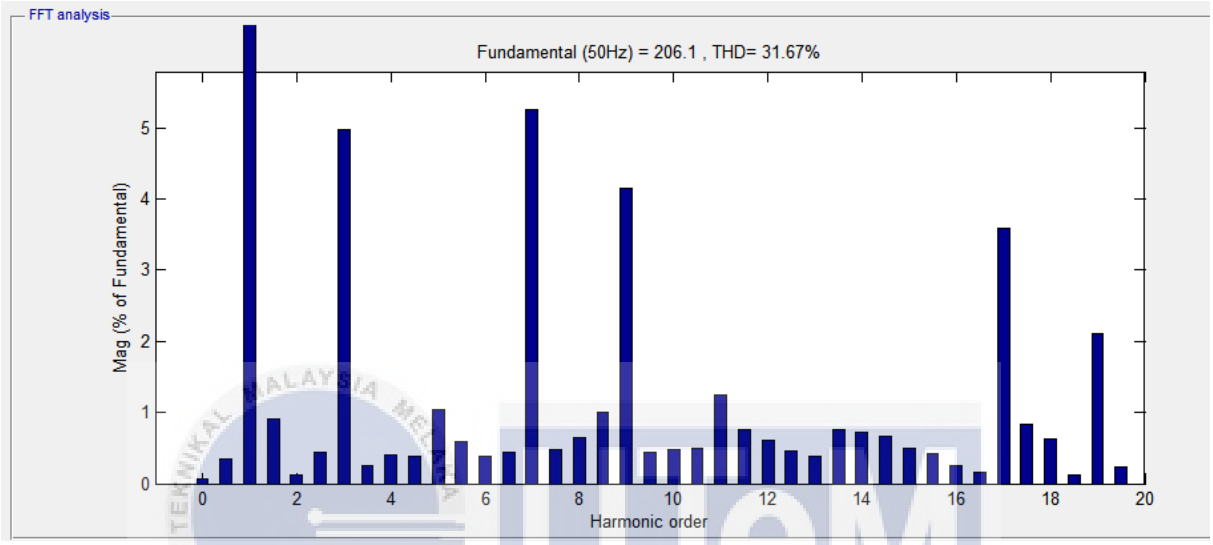

Figure 4.20: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.8 using DC Supply

Figure 4.21 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 0.9. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 27.74% with 237.1Vrms and 20 harmonic order.

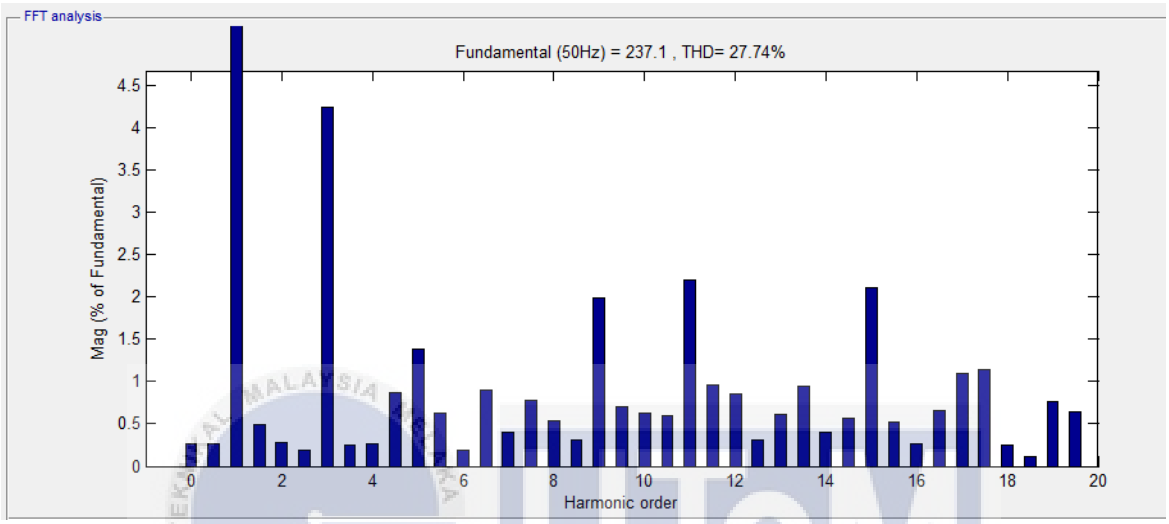

Figure 4.21: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.9 using DC Supply

Figure 4.22 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using DC supply and the modulation index that is set at 1.0. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.1 seconds and it produce the THD is 24.34% with 267.6Vrms and 20 harmonic order.

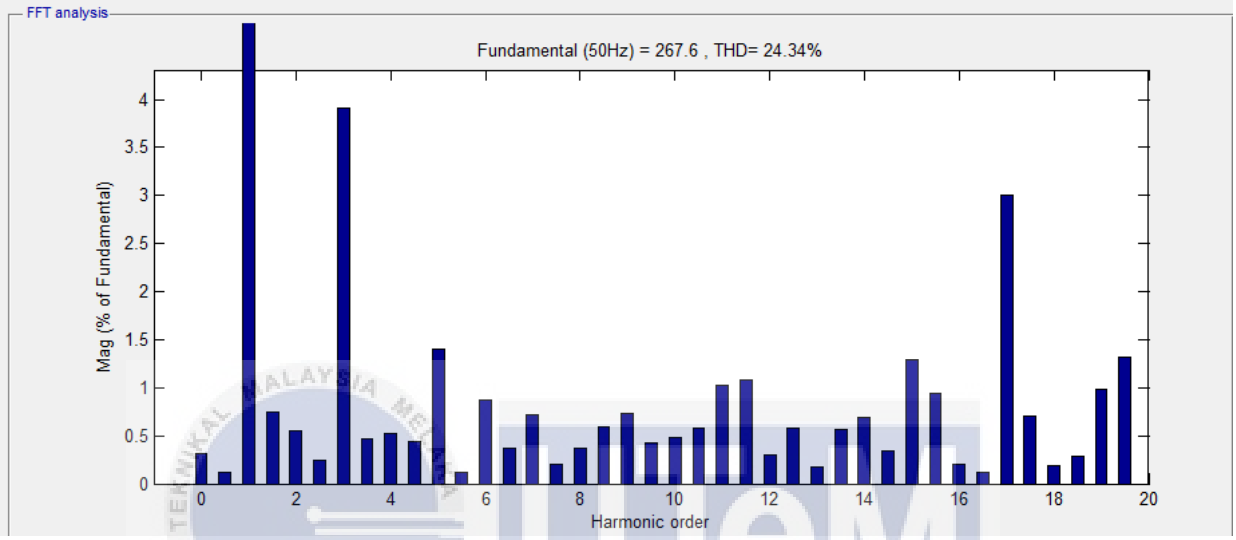

Figure 4.22: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 1.0 using DC Supply

4.1.6 Harmonic spectrum for Total Harmonic Distortion (THD) voltage based on supercapacitor

Figure 4.23 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.5. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 0.99% with 3.881Vrms and 20 harmonic order.

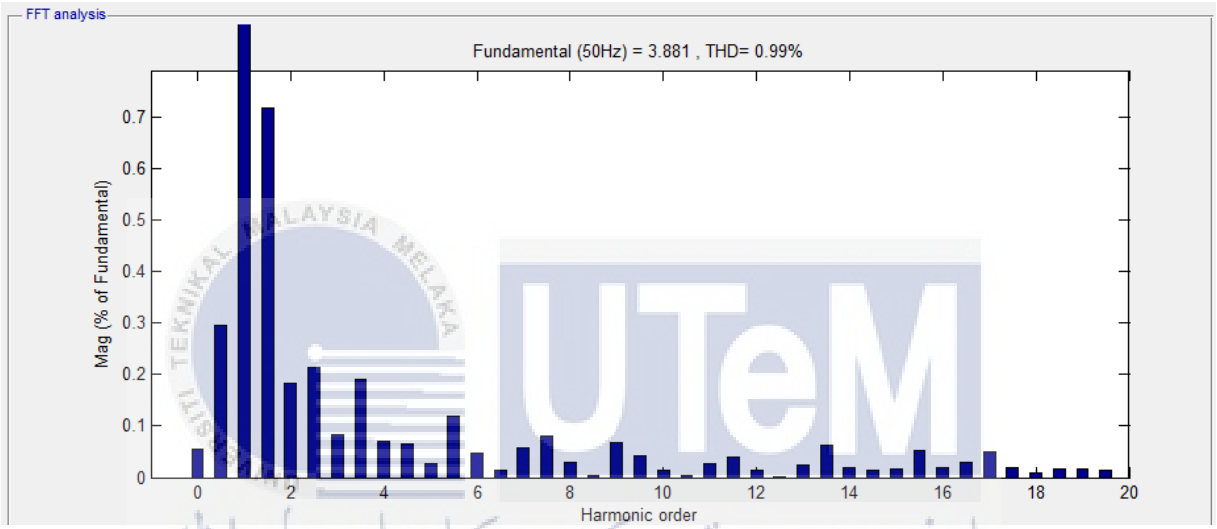

Figure 4.23: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.5 using supercapacitor

Figure 4.24 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.6. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 0.66% with 4.663Vrms and 20 harmonic order.

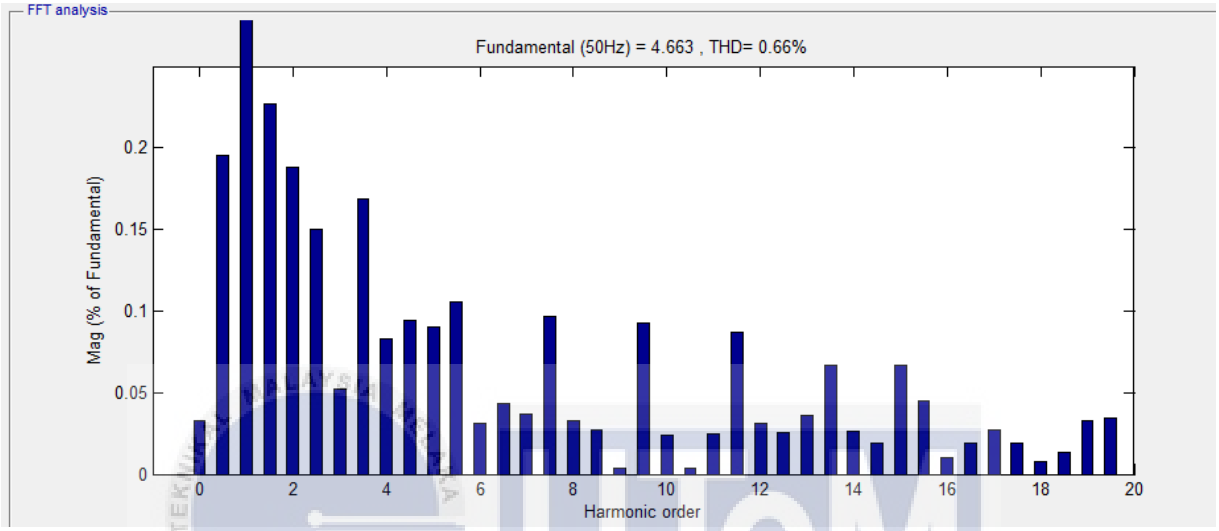

Figure 4.24: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.6 using supercapacitor

Figure 4.25 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.7. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 0.72% with 5.862Vrms and 20 harmonic order.

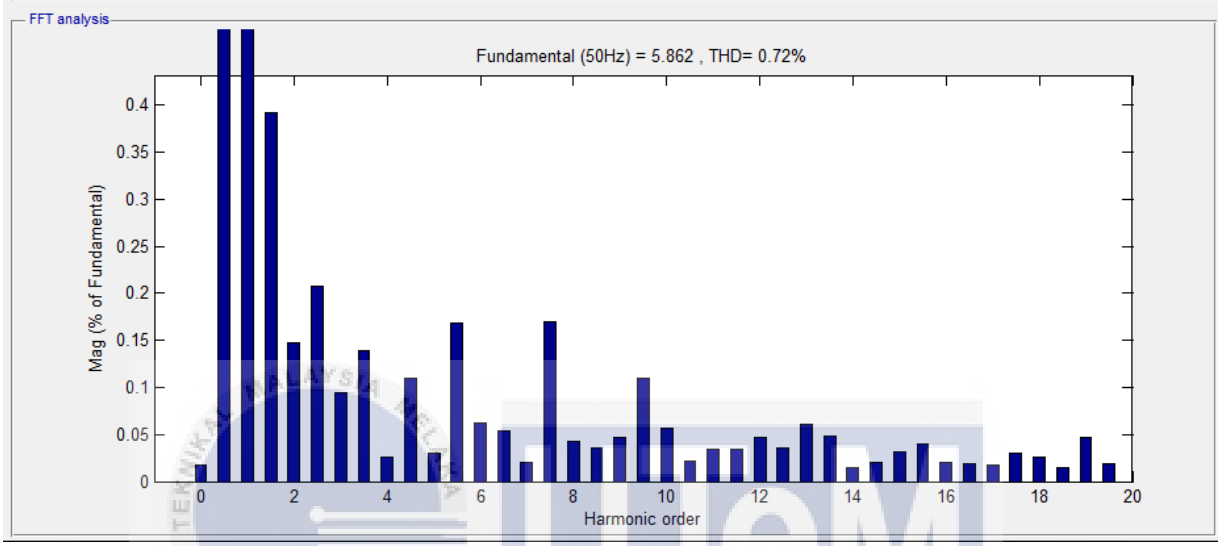

Figure 4.25: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.7 using supercapacitor

Figure 4.26 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.8. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 1.28% with 6.668Vrms and 20 harmonic order.

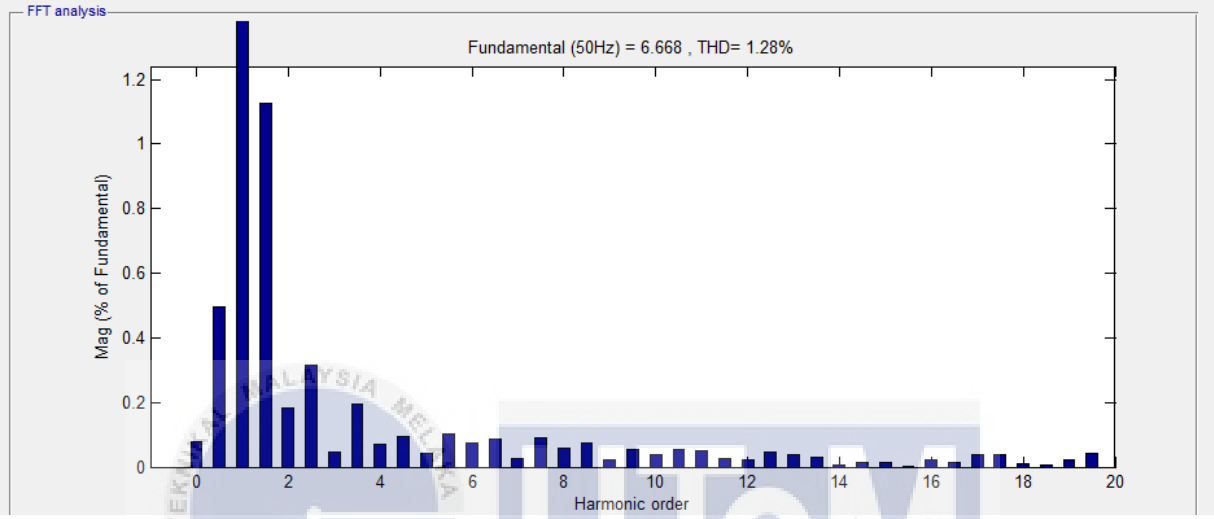

Figure 4.26: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.8 using supercapacitor

Figure 4.27 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 0.9. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 0.84% with 7.667Vrms and 20 harmonic order.

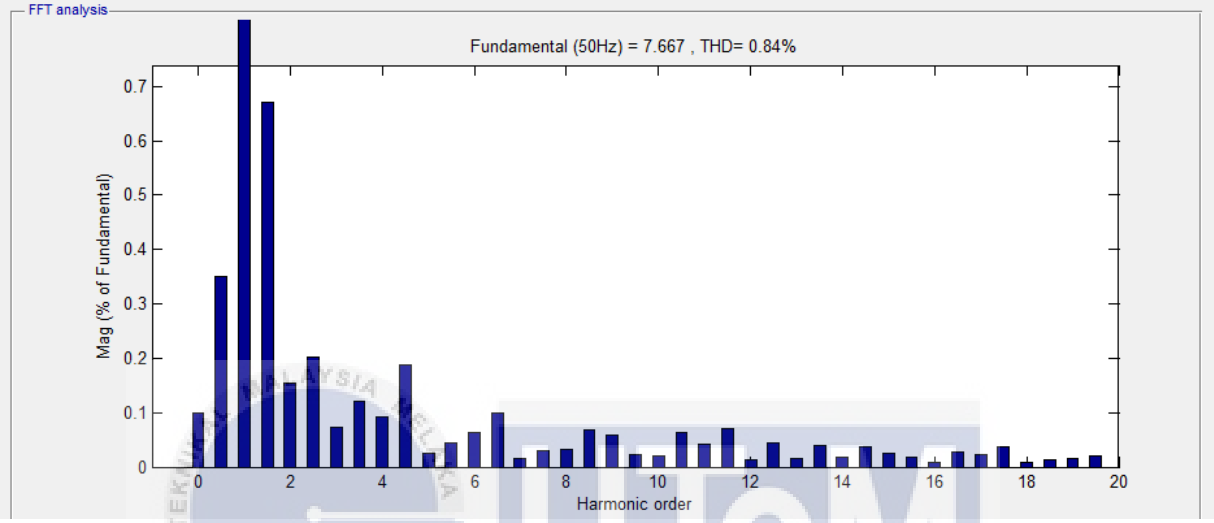

Figure 4.27: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 0.9 using supercapacitor

Figure 4.28 show the harmonic spectrum at output seven-level cascaded H-Bridge multilevel inverter by using supercapacitor and the modulation index that is set at 1.0. The frequency of this scope for this graph is set to 50Hz with carrier frequency which is set to 2500Hz and 0 firing angle. The time taken to selected signal is 0.4 seconds and it produce the THD is 0.92% with 8.66Vrms and 20 harmonic order.

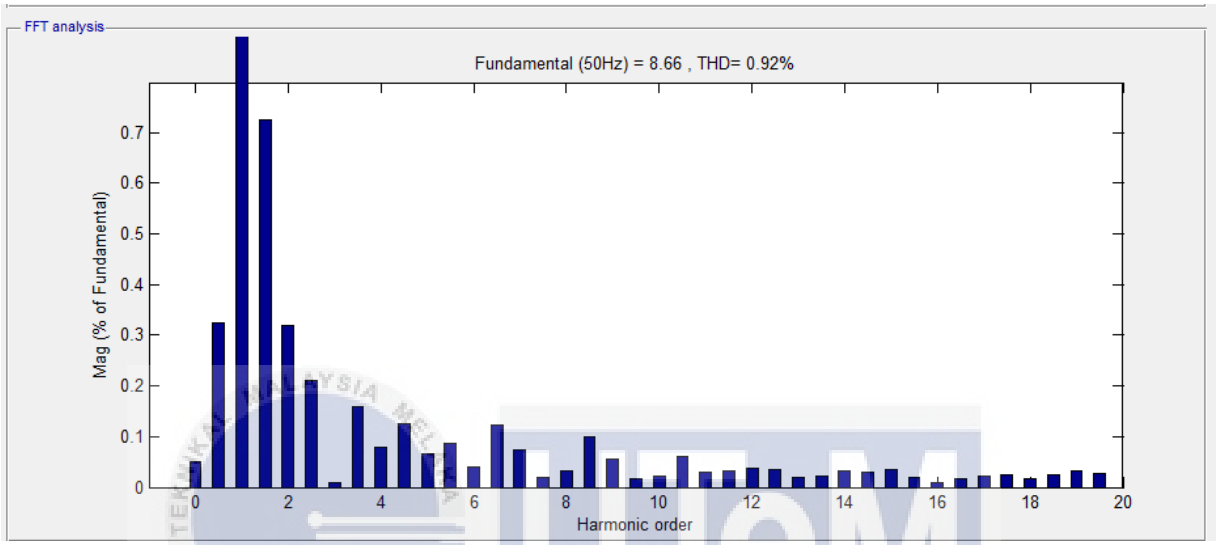

Figure 4.28: Harmonic spectrum for voltage at output seven-level cascaded H-Bridge multilevel inverter which MI = 1.0 using supercapacitor

4.1.7 Comparion between supercapacitor and DC supply based on Total Harmonic Distortion voltage (THDv)

Table 4.1: Comparion between supercapacitor and DC supply based on Total Harmonic Distortion voltage (THDv)

Modulation Index	THDv supercapacitor (%)	THDv DC supply (%)
0.5	0.99	51.72
0.6	0.66	44.35
0.7	0.72	35.19
0.8	1.28	31.67
0.9	0.84	27.74
1.0	0.92	24.34

Table 4.1 shows the comparion between supercapacitor and DC supply based on Total Harmonic Distortion voltage (THDv). The huge amount of total harmonic distortion (THD) voltage is reduce occur in this seven-level cascaded H-Bridge multilevel inverter by replacing the source from DC supply with supercapacitor by using MATLAB SIMULINK software.

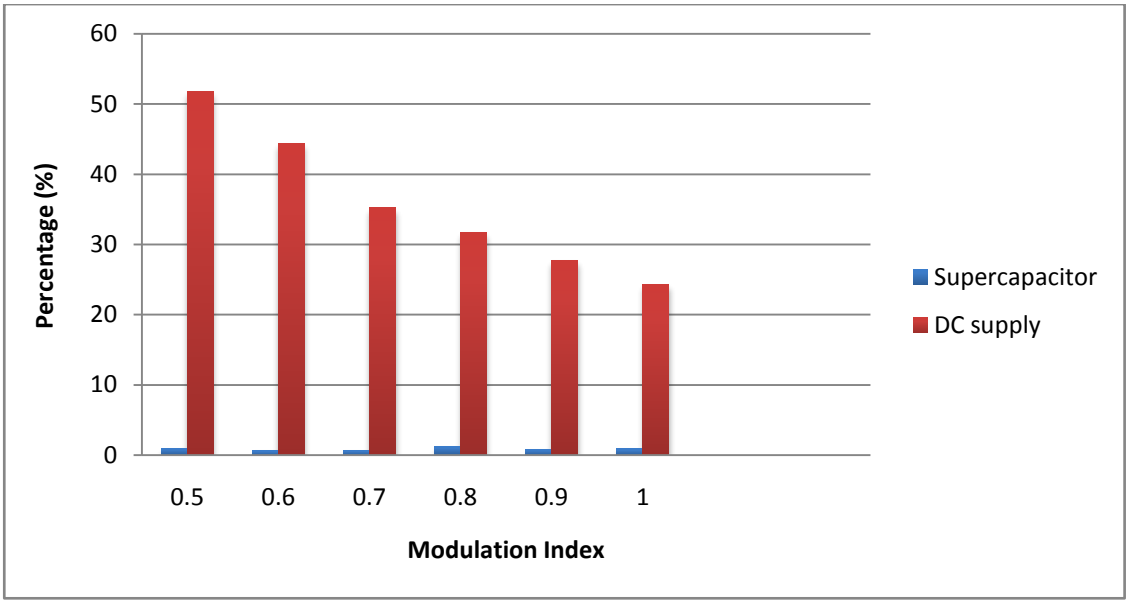

Figure 4.29: Bar Chart of comparison between DC supply and supercapacitor

Figure 4.29 shows the bar chart of comparison between DC supply and supercapacitor in percentage their performance. It shows that supercapacitor is more efficient in reduction of Total Harmonic Reduction (THD) than the DC supply.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The main objective for this project is to make a comparison the input source of cascaded H-Bridge multilevel inverter based on supercapacitor for harmonic reduction. The result that needs to be obtained is the harmonic distortion in waveform, harmonic distortion Fast Fourier Transform (FFT), and chart that show the percentage Total Harmonic Distortion (THD). Throughout pervious work that has been done, DC supply have been generated. In this project, the input source of cascaded H-Bridge multilevel inverter has changed from DC supply with supercapacitor. This project use Sinusoidal Pulse Width Modulation (SPWM) controller to control and inject the signal to the switching component. The results showed that the THD voltage of supercapacitor is reduced compared to the DC supply. It has given a clear picture that supercapacitor has more efficiency than other conventional storing system as DC supply. The supercapacitor designed which the result of the simulation has revealed that total harmonic distortion (THDv) voltage in supercapacitor storing system is lesser than DC supply.

5.2 Recommendation

Total harmonic distortion (THD) of three-phase sinusoidal pulse width modulation (SPWM) seven level cascaded H-Bridge inverter based on supercapacitor as storage is reduced. It can observed that the Voltage at THD for the super capacitor is considered low at 5% as specified by IEEE 519 standard on harmonic distortion level. The proposed model has investigated better harmonic distortion for voltage. In the next step, the prototype will be developed based on the inverter of cascaded H-Bridge with supercapacitor. This simulation will be validated through experiments in order to ensure the effectiveness of using supercapacitor as storage compared to other dc source.

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