AN OPTIMIZATION OF GATE LEAKAGE IN SCALED MOSFET ON THE EFFECT OF TEMPERATURE DURING THE METAL GATE ANNEALING PROCESS IN GATE-LAST TECHNOLOGY

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This report is submitted in partial fulfillment of requirements for the Bachelor Degree in Electronic Engineering (Industrial Electronic)

Faculty of Electronic Engineering and Computer Engineering

Universiti Teknikal Malaysia Melaka

JUNE 2017

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FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

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Tajuk Projek: AN OPTIMIZATION OF GATE LEAKAGE IN SCALED MOSFET ON THE EFFECT OF TEMPERATURE DURING THE METAL GATE ANNEALING PROCESS IN GATE-LAST TECHNOLOGY

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This thesis is dedicated to

My beloved mother and father, my siblings and my colleagues

who had been supporting me to complete this project.

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ACKNOWLEDGEMENT

"In the name of Allah, Most Gracious, Most Merciful,"

First and for most, praise to Allah S.W.T, because of His blessing that gave me to complete my Final Year Project and thesis in a given time without having any difficulties. The special thanks go to my helpful supervisor, Madam Niza Bt Idris for the valuable guidance and advice. She inspired me greatly to work in this project. Her willingness to motivate me contributed tremendously to my project for showing me some example that related to the topic of my project.

I also take this opportunity to express a deep sense of gratitude to Universiti Teknikal Malaysia Melaka for giving me a chance to undergo this Final Year Project as partial fulfillment for my Degree. Thanks again to Universiti Teknikal Malaysia Melaka for providing me with a good environment and facilities to complete this project

Finally, an honorable mention goes to my families and friends, especially Ameen Nurzikri Bin Munjani for their understandings, opinion, knowledge and supports in completing this project. Without help of the particular that mentioned above, I could face many difficulties while to finish this project.

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ABSTRACT

This research has been done to improve the performance of 22nm n-MOSFET by study the relationship between the effect of temperature during the metal gate annealing process toward an n-type MOSFET performance. The 22nm n-type MOSFET is designed by using Gate-Last Technology. Gate-last technology introduced the dummy gate to withstand the high temperature throughout the annealing process then replace the gate with the metal gate at the last process. The tools utilize is Technology Computer Aided Design (TCAD). In TCAD software, silvaco's deck build ATHENA and ATLAS were used to design the physical structure of bulk MOSFET hence obtaining its characteristics. The design structure will be going through a step by step fabrication process which parameter and value are stated in International Technology Roadmap for Semiconductor (ITRS). Then I-V characteristics of the device can be analyzed by using ATLAS to show the particular performance of current device created. The objective of this experiment is to design and compare the performance of 22nm n-MOSFET when the different value of temperature during the metal gate annealing process is applied. The results indicate that the difference in the value of temperature will affect the performance of the device. The optimized temperature of annealing process for this device is 750°C.

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ABSTRAK

Kajian ini telah dilakukan untuk meningkatkan prestasi 22nm n-MOSFET dengan mengkaji hubungan antara kesan suhu semasa proses penyepuhlindapan pintu logam terhadap prestasi n-jenis mosfet. 22nm n-jenis mosfet direka bentuk dengan menggunakan Teknologi Gate-Last. Teknologi Gate-lepas memperkenalkan pintu gantian untuk menahan suhu yang tinggi sepanjang proses penyepuhlindapan kemudian menggantikan pintu gerbang dengan pintu gerbang logam pada proses terakhir. Alat yang digunakan adalah Technology Computer Aided Design (TCAD). Dalam perisian TCAD, ATHENA modul digunakan untuk mereka bentuk struktur fizikal mosfet. Struktur reka bentuk melalui langkah demi langkah proses fabrikasi yang mengikut paiwaian parameter dan nilai yang telah dinyatakan dalam Pelan Hala Tuju Teknologi Antarabangsa Semiconductor (ITRS). Ciri-ciri I-V peranti boleh dianalisis dengan menggunakan ATLAS untuk menunjukkan prestasi peranti. Objektif kajian ini adalah untuk mereka bentuk dan membandingkan prestasi 22nm n-MOSFET apabila nilai suhu yang berbeza digunakan semasa proses penyepuhlindapan pintu logam. Keputusan menunjukkan bahawa nilai suhu yang berbeza akan menjejaskan prestasi peranti. Suhu yang optimum bagi proses penyepuhlindapan untuk peranti adalah 750 ° C.

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LIST OF ABBREVIATIONS

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
EDA	Electronic Design Automation
VWF	Virtual Wafer Fab
CMOS	Complementary Metal-Oxide-Semiconductor
NMOS	N-channel Metal-Oxide-Semiconductor
ITRS	International Technology Roadmap for Semiconductors
EOT	Equivalent Oxide Thickness
SiO_2	Silicon Dioxide
HK/MG	High-k Metal Gate
TCAD	Technology Computer Aided Design
Vds	Source-Drain Voltage
Vg	Gate Voltage
Vth	Threshold Voltage
°C	Degree Celsius
I	Current
V	Voltage

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CHAPTER 1

INTRODUCTION

1.1 Project Introduction

The phenomena of miniature size of MOSFET device have given the significant impact of semiconductor technology. The technology of scaling down the CMOS device can achieve a nanometre (nm) size which will give an advantage in production coast since there will be many CMOS devices can be fabricated on a single wafer. This scale down also suitable for the function and the performance of the digital device in term of storage and power rate of processing and so on [1]. According to Gordon Moore in his theory called Moore Law state that the number of transistor in the integrated circuit would be double for every two years. This will give an idea of there will be continuity in the scaling down the size of the transistor until reaching its maximum state. According to Iwai (2015), he predicts that the scaling down the size of the transistor only for several generations of Nano size before the Moore Law ended [2]. This Moore Law creates a competition in the industry to make the smaller and high performance of the electronic device [3]. This scaling down the size of transistor cause the several technical issues such as a percentage of gate leakage that will affect the performance of the device.

Regarding of that problem, this research will explore the effect of the annealing temperature toward the optimization of the gate leakage. In this research, the Gate-Last Technology will be used as the base of the N-type of MOSFET. Gate-Last Technology is a technique that introduced by Intel that implements it in 45nm technology. This

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technology uses a dummy gate to withstand the high temperature in annealing process and replace the metal gate at the last process [4].

There are four terminals consist in metal-oxide-silicon field effect transistor (MOSFET) namely source, gate, drain, and substrate (body) [5]. The body (substrate) of the MOSFET is commonly connected to the source terminal. The gate voltage controls the electron concentration in the n-channel MOSFET is preferred over p-channel MOSFET as the mobility of electrons is higher than the holes. Thus, only three terminals appear in electrical diagrams as illustrated in Figure 1.1.

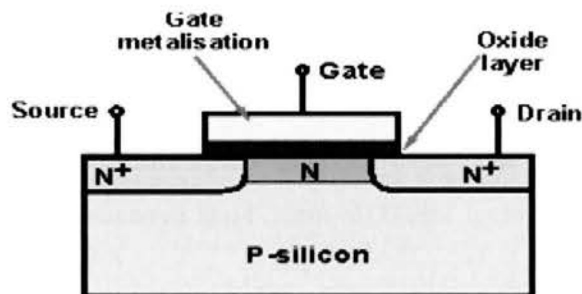

Figure 1.1 Basic n-Type MOSFET Structure

Source from radio electronic.com

The MOSFET is capable for voltage gain and signals power gain [4]. The current flows in MOSFET are controlled by gate voltage. Thus, it is known as a voltage controlled device [6].

The annealing process is applied a specified temperature to the terminal that will change its molecule structure. So, in this research, I will construct 22nm bulk MOSFET and investigate the effect of changing the temperature in an annealing process. We will see if there was a different of IV characteristic and gate leakage when we applied the different temperature of the annealing process. This process only involves the simulation that will conduct using TCAD Silvaco software that contains 2 part which is we will use ATHENA to construct the structure and ATLAS are used to plot the characteristic of the device that has been constructed.

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1.2 Problem Statements

The miniature size of MOSFET leads a lot of unwanted technological issues such as short channel effects (SCE). This effect can change the threshold voltage, clear pinch-off of the channel, increased output impedance and the most crucial is increased leakage current. All this change can slow down the performance of MOSFET. One of the cause factors that leads gate leakage to happen in MOSFET is temperature applied during an annealing process.

1.3 Objectives

The main objectives of this project are:

- To design the structure of Bulk 22nm MOSFET using Gate-Last Technology
- To examine the performance of Bulk 22nm MOSFET including IV characteristic and the leakage current.
- To investigate the effects of using different temperature for annealing applied during the formation of metalgate.

1.4 Scope of Project

The scopes of the project are as the following:

- Focus on designed and simulate the Bulk 22nm N-MOSFET using Gate-Last Technology.
- Focus on using six different temperatures (for temperature = 700°C, 750°C, 800°C, 850°C, 900°C, 950°C, 1000°C) for annealing applied during the formation of metalgate.
- Using Silvaco TCAD software as simulation tools, include Athena for design structure and Atlas for plotting the graph of the characteristics.

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1.5 Thesis Outline

The outline of this project is planned to ensure that the flow of this research study is presented properly. Besides that, this outline also can help the readers to fully understand the project research all about from the first chapter to the last chapter.

Chapter 1 includes the project introduction, problem statements, objectives, scope of this project and the thesis outline. Theory and literature review is discussed in chapter 2.

Chapter 2 discussed the MOSFET and the operation of the MOSFET. This chapter also states the research on the fabrication process of the N-Type MOSFET using gate-last technology. Besides, tools used in extension work is also outlined. This chapter will be the knowledge source to gain the understanding of the gate process theories.

The methodology and software implementation of this project is thoroughly discussed in chapter 3. The software to complete this research is SILVACO TCAD and it has two parts which are ATHENA and ATLAS.

Chapter 4 elaborate the results and discussions produced by the simulation. It consists of the findings and explanations of the data and problems occurs along this research is conducted. The result is presented in the form of the designed structure and graph comparison.

Lastly, in chapter 5 conclusion and recommendations are outlined. In this chapter, it concludes the overall project and makes a suggestion for the future work regarding this study.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Demand toward the modern electronic device that small and high performance is one of the motivation to semiconductor technology industry in their mission to create a Nanoscale MOSFET device that also gives a big impact toward research and development in scaling down transistor process. Follow the Moore Law, the industry has continuous to scaling down the transistor and have been set as the future of semiconductor field by International Technology Roadmap for Semiconductor. This scaling down transistor started earlier 1970, and this process shows a rapid grow until able to enter the nanometer region. But along with this achievement, there is some issue need to take care by researcher and semiconductor industry and still looking for the solution. One of the issue when scaling down the transistor is it's difficult to get the suitable threshold voltage(Vth) of the transistor and to control from having a leakage in the device [7].

The threshold voltage is the parameter that will decide whether that transistor can function as a switch or not which is the base of all the digital device [8]. From the research that has been done by Sugii et al. (2013), the performance of the device is influence by many factors such as short channel effect, change of threshold voltage, current leakage and so on [9]. This showed that not only one factor that controlled value of Vth when scaling down transistor is taking place. All of this contribute to the difficulty and challenge to get the suitable Vth. It happens because of current leakage along source and drain and also form a gate to drain, all of this will make transistor is always in ON state although there is no voltage provided at gate terminal [10].

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2.2 N-Type MOSFET Structure

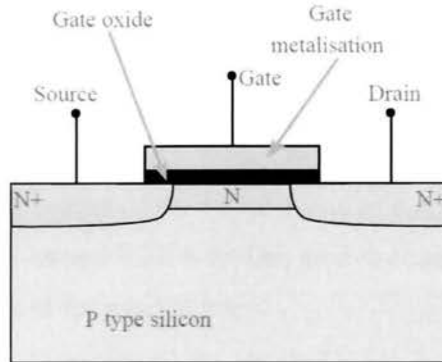

Figure 2.1 Basic n-Type MOSFET Structure

Source from www.electronics-notes.com

Figure 2.1 shows the basic n-Type MOSFET structure. The metal-oxide-silicon field effect transistor (MOSFET) consists of four terminals, namely the source, gate, drain, and substrate (body). It is, in its very simplest form, a simple extension of the MOS capacitor, in which the gate electrode and the semiconductor channel constitute the parallel capacitor plates and the isolating oxide layer is equivalent to the dielectric material [6]. Although the MOSFET has a four-terminal device with the source (S), the gate (G), the drain (D), and the body (B) terminals [5]. The body (substrate) of the MOSFET is commonly connected to the source terminal, making it three terminal devices like other field-effect transistors. Since these two terminals are normally connected to each other internally, it caused them to be short-circuited. Thus, only three terminals appear in electrical diagrams.

The drain and source terminals are connected to the heavily doped regions whereby the gate is connected on top of the oxide layer, and the body terminal or substrate is connected to the intrinsic semiconductor. The MOSFET is capable for voltage gain and signals power gain [11]. The inversion layer is formed between the source and drain terminal due to the flow of the carriers in it, the current flows in MOSFET are controlled by gate voltage. Thus, it is known as a voltage controlled device.

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2.3 Basic MOSFET Operation

There are three regions in which MOSFETs can operate:

- Cut-off region: In this region of the MOSFET is in a non-conducting state, i.e. turned OFF - channel current IDS = 0. The gate voltage VGS is less than the threshold voltage required for conduction.
- Linear region: In this linear region the channel is conducting and controlled by the gate voltage. For the MOSFET to be in this state the VGS must be greater than the threshold voltage and also the voltage across the channel, VDS must be higher than VGS.
- Saturation region: In this region, the MOSFET is turned hard on. The voltage drop for a MOSFET is typically lower than that of a bipolar transistor and as a result power MOSFETs are widely used for switching large currents.

2.4 N-channel MOSFET Fabrication Process

There is a variety of basic fabrication steps used in the manufacture of modern MOS ICs (Metal Oxide Semiconductor Integrated Circuits). The same process can be utilized for the design of NMOS or PMOS devices. The conventional gate material used could be either metal or poly-silicon whereby the most commonly used substrate is bulk silicon or silicon-on-sapphire (SOS). The following diagrams show the basic steps involve in n-MOSFET fabrication process [12].

Figure 2.2 Pure Silicon

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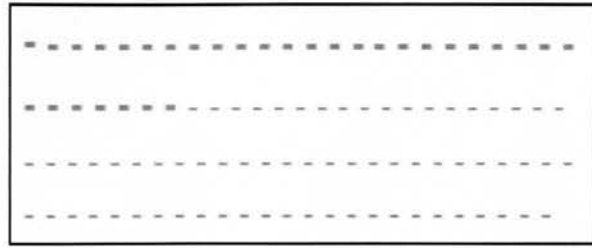

Figure 2.3 P-type impurity slightly doped.

Figure 2.2 and Figure 2.3 shows how the process is carried out on a thin wafer cut from a single crystal of silicon of high purity on which required p-impurities are introduced as a crystal is grown. Such wafer is typically 75 to 150 mm in diameter and 0.4 mm thick and doped with boron to impurity concentrations 1015/cm3 to 1016/cm3 [10], giving resistivity in the approximate range of 25-ohm cm to 2-ohm cm.

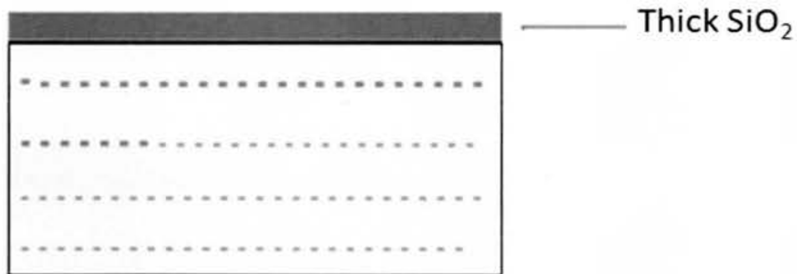

Figure 2.4 SiO2 Deposited over Si Surface

Figure 2.4 shows a layer of silicon dioxide (SiO2) is grown all over the surface of the wafer to protect the surface. The SiO2 used is typically 1 μm thick. It acts as a barrier to the dopant during the process and provides an insulating substrate onto which other layers may be deposited and patterned.

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