CHARACTERIZATION OF POLYSILICON VS METAL GATE ELECTRODES IN 19nm NMOS DEVICE

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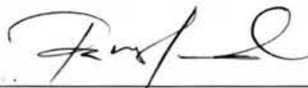

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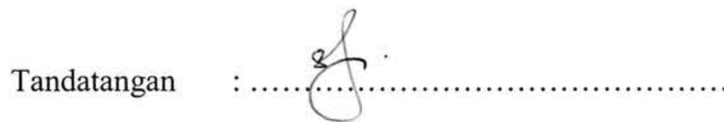

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DEDICATION

For my beloved husband, mother and my little lovely sons.

Thank You.

In memory, my late father.

Al - Fatihah

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ABSTRACT

Polysilicon has been used as a great gate dielectric since over years ago. The need to shrinking the size of MOSFET due to the new technology today need to replace the conventional Poly-Si/SiO_2 device. The main reason for replacing with new dielectric technology is because of the small scale NMOS devices using polysilicon gate lead to produce a high leakage current. To overcome this problem, metal gate with several different high *k* materials has been introduced in this project. This thesis presents the analysis of Polysilicon versus metal gate performance and compatibility of combination using several dielectric materials. The high *k* materials used in this simulation are Al_2O_3, HfO_2, TiO_2 and ZrO_2. The fabrication of the devices was done by using an ATHENA simulator module while the electrical characterization of the devices was analyzed by using an ATLAS simulator module. Both of this simulator module are from SILVACO TCAD Tools. Analysis of the results found that the best combination device in producing a great performance is Tungsten Silicide with Titanium Oxide ($WSiO_2/TiO_2$). The $WSiO_2/TiO_2$ device produced 587.69 μA/μm of drive current (I_{ON}) at 0.5345V of threshold voltage. The result of leakage current (I_{OFF}) for this device is at 1.9199 pA/μm which is the lowest I_{OFF} compared to the others. The parameter values meet the requirement predicted by the International Technology Roadmap Semiconductor (ITRS) 2013.

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ABSTRAK

Polisilikon telah digunakan sebagai pagar dielektrik yang baik sejak beberapa tahun yang lalu. Keperluan untuk mengecilkan saiz MOSFET adalah kerana teknologi baru hari ini perlu bagi menggantikan peranti Poly-Si/SiO_2 konvensional. Sebab utama untuk menggantikan dengan teknologi dielektrik baru adalah kerana peranti NMOS berskala kecil yang menggunakan polisilikon menghasilkan arus bocor tinggi. Untuk mengatasi masalah ini, pintu logam dengan beberapa bahan *k* tinggi yang berbeza telah diperkenalkan dalam projek ini. Tesis ini membentangkan analisis tentang polisilikon berbanding prestasi pintu logam dan keserasian gabungan menggunakan beberapa bahan dielektrik. Bahan *k* tinggi yang digunakan dalam simulasi ini adalah Al_2O_3, HfO_2, TiO_2 dan ZrO_2. Pembuatan peranti telah dilakukan dengan menggunakan modul simulator ATHENA manakala perincian peranti elektrik dianalisis dengan menggunakan modul simulator ATLAS. Kedua-dua modul simulator ini adalah daripada perisian SILVACO TCAD. Analisis keputusan medapati bahawa gabungan peranti terbaik dalam menghasilkan prestasi yang hebat adalah Tungsten Silicide dengan Titanium Oxide ($WSiO_2/TiO_2$). Peranti $WSiO_2/TiO_2$ telah menghasilkan 587.69 μA/μm arus pandu (I_{ON}) pada 0.5345V voltan ambang. Keputusan arus bocor (I_{OFF}) untuk peranti ini adalah sebanyak 1.9199 pA/μm yang merupakan (I_{OFF}) paling rendah dibandingkan dengan yang lain. Nilai-nilai parameter adalah memenuhi keperluan yang diramalkan oleh *International Technology Roadmap Semiconductor* (ITRS) 2013

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LIST OF ABBREVIATIONS AND SYMBOLS

MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N channel Metal Oxide Semiconductor
SiO_2	-	Silicon Oxide
HfO_2	-	Hafnium Oxide
TiO_2	-	Titanium Oxide
ZrO_2	-	Zirconium oxide
Al_2O_3	-	Aluminium Oxide
$WSiO_2$	-	Tungsten Silides
$TiSiO_2$	-	Titanium Silicides
High-*k*	-	High Permittivity
K	-	Permittivity
I_{ON}	-	Drive Current
I_{OFF}	-	Leakage Current
V_{TH}	-	Threshold Voltage
SS	-	Subthreshold Swing

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ITRS	-	International Technology Roadmap Semiconductor
DIBL	-	Drain Induced Barrier Lowering
CVD	-	Chemical Vapor Deposition
T_{OX}	-	Gate oxide thickness
BPSG	-	Boron Phosphor Silicate Glass
PMD	-	Pre Metal dielectric
IMD	-	Intel Metal Dielectric

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a four terminal device with source, drain, gate and substrate terminals. The MOSFET is commonly use as a transistor in digital and analogue circuits. The MOSFET works by varying the width of a channel along which charge carriers flow. The charges carriers contain electrons and holes flow from the source and exit through the drain. The voltage control the width of the channel on the gate. The gate commonly insulated with a thin layer of metal oxide.

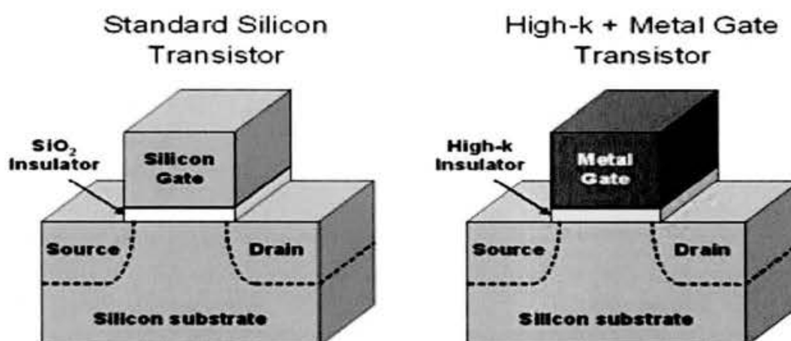

Figure 1.1: MOS transistor structure with dielectric gate [1]

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Generally, this project is focused to analyze the performance of polysilicon and metal gate electrodes. The polysilicon are combined with the silicon oxide (SiO_2) and four high-*k* materials which are hafnium oxide (HfO_2), titanium oxide (TiO_2), zirconium oxide (ZrO_2) and aluminium oxide (Al_2O_3). This high-*k* materials also integrated with the tungsten silides ($WSiO_2$) and titanium silicides ($TiSiO_2$) as the metal gate elecrodes. All these combination of structures are analyzed and presented in the following chapter.

1.2 Problem Statement

The traditional polysilicon has been used as an efficient gate since over many years ago. The need for increased speed of n-channel Metal Oxide Semiconductor (NMOS) has led to reducing the oxide thicknesss and reduce the size of NMOS. As the 19 nm NMOS is smaller in scales, it will lead a leakage current and degrade the performance if use the conventional polysilicon gate dielectric. Hence, the metal gate will be use to overcome this problem.

The advantages of metal gate electrode over polysilicon gates are much lower gate resistance and desirable work function setting [2]. The electrical characteristics of each structures need to be analyse to find the best combination in producing the great performance of NMOS. The compatibility of different high-*k* dielectric materials with a metal gate may differ due to their different dielectric constants [3].

1.3 Objectives

The objectives of this project are stated below :

(i) To design the 19 nm NMOS device by using ATHENA modules simulator

(ii) To analyze the electrical characteristic value utilizing by ATLAS modules simulator

(iii) To compare the characteristic of the polysilicon gate and metal gate

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1.4 Scope of Project

The scope of this project is consists of two step of simulations. The simulations are performed with a device simulator SILVACO TCAD tools. The simulations of devices fabrication are designed using ATHENA module. The simulations are used for the physical structure of the scaled NMOS. The simulation of electrical characteristics is being performed by using ATLAS module.

The performance of polysilicon with silicon oxide (SiO_2) will be compared with titanium silicides ($TiSiO_2$) and tungsten silides ($WSiO_2$) as a high-*k* dielectric. The high-*k* materials used are titanium oxide (TiO_2), hafnium oxide (HfO_2), zirconium oxide (ZrO_2) and aluminium oxide (Al_2O_3). The completed devices were characterized by using ATLAS module.

The parameters were targeted to comparing are the threshold voltage, gate leakage current, drive current (I_{ON}), leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio and subthreshold swing. All these electrical characteristic value must be refer to the requirement predicted by International Technology Roadmap Semiconductor (ITRS) 2013 [4]. Table 1.1 shows the requirement values of device characteristic by ITRS 2013.

Table 1.1 : International Technology Roadmap Semiconductor (ITRS) 2013 [4]

Device characteristic	ITRS 2013
Threshold voltage (V_{TH})	0.533 V±12.7%
Drive current (I_{ON})	≥456 μA/μm
Off-leakage current (I_{OFF})	≤20 pA/μm
Subthreshold voltage (SS)	70~100(mV/decade)

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1.5 Project Outline

This thesis consist of five chapters. Chapter one provides an introduction of this project which are includes the project introduction, problem statement, objectives of this project and scope of project.

Chapter two contains the literature review in several of jurnals. In this chapter review about introduction of MOSFET, basic structure of MOSFET and circuit symbol of MOSFET. The explaination about enhancement type N channel of MOSFET, the polysilicon versus metal gate, short channel effect, leakage current and threshold voltage.

Chapter three discuss about the methodology of this project. This chapter explains the flow of this project and explainations on the designing of the 19 nm NMOS device using deckbuild and fabrication process using ATHENA.

Chapter four shows the results that will obtain from the simulation using ATLAS module. The data and results are then analyzed and compared to obtained the best materials between polysilicon gate versus metal gate. This chapter highlights the comparisons of the results.

For the last, chapter five will be the finalize all the chapters. In this chapter, it contains conclusion and suggestions. In order to determine the achievements of this project, all the chapters must meet the objectives stated previously.

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