ANALYZE OF PROCESS PARAMETER IN 19nm WSi_2/TiO_2 N-CHANNEL MOSFET USING STATISTICAL MODELLING

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Dedicated to my beloved family especially my parents, supervisor, lecturers and all my friends who helping me whether directly or indirectly.

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ABSTRACT

This project investigates the impact of process parameter on threshold voltage (V_{TH}), drive current (I_{ON}) and leakage current (I_{OFF}) for 19nm WSi_2/TiO_2 NMOS device. using statistical modelling. The statistical methods that were used are 2k-factorial design and Taguchi method. The four process parameter, namely oxide growth temperature, V_{TH} implant energy, pocket halo implant dose and compensate halo implant will be investigated and adjusted to improve the results. The simulated of the device was performed by using ATHENA module. While the electrical characterization of the device was implemented by using ATLAS module. These two modules will be combined with 2k-factorial and Taguchi Method to aid design and optimize the process parameters. The most effective process parameter with respect to threshold voltage, drive current and leakage current were chosen depend on the percentage of the factor effect on S/N ratio that indicate the relative power of factor to reduce variation. In this research, optimum condition for elcetrical characteristics have been compared using two methods to choose the best method for optimization process. The most dominant or significant factors for S/N Ratio are pocket halo implant dose and compensate implant dose. Meanwhile, the S/N Ratio values of V_{TH}, I_{ON} and I_{OFF} after the optimization approaches for array L_9 is 41.30dB, 55.70dB and -14.17dBrespectively. In L_9 experiments, V_{TH}, I_{ON} and I_{OFF} values for NMOS device after optimizations approaches are 0.530V, 622.667μA and 2.776pA respectively. The results obtained are closer to ITRS 2013 prediction. As conclusions, Taguchi Method was observed to be the most suitable method to be implemented in statistical modeling of 19nm WSi_2/TiO_2 NMOS device.

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ABSTRAK

Projek ini menyiasat kesan proses parameter di voltan ambang (V_{TH}), *drive current* (I_{ON}) dan arus kebocoran (I_{OFF}) untuk peranti 19nm WSi_2 / TiO2 NMOS. menggunakan pemodelan statistik. Kaedah statistik yang digunakan adalah reka bentuk 2k-faktorial dan kaedah Taguchi. Empat proses parameter, iaitu suhu oksida pertumbuhan, implan tenaga V_{TH}, poket halo implan dos dan mengimbangi halo implan akan disiasat dan diselaraskan untuk meningkatkan keputusan. Simulasi peranti telah dilakukan dengan menggunakan modul ATHENA. Manakala pencirian elektrik peranti telah dilaksanakan dengan menggunakan modul ATLAS. Kedua-dua modul akan digabungkan dengan 2k-faktorial dan Taguchi Kaedah untuk membantu reka bentuk dan mengoptimumkan parameter proses. Proses parameter paling berkesan berkenaan dengan voltan ambang, memandu semasa dan arus bocor dipilih bergantung kepada peratusan kesan faktor kepada nisbah S / N yang menunjukkan kuasa relatif faktor untuk mengurangkan variasi. Dalam kajian ini, keadaan optimum untuk ciri-ciri elcetrical telah dibandingkan dengan menggunakan dua kaedah untuk memilih kaedah yang terbaik untuk proses pengoptimuman. Faktor yang paling dominan atau penting untuk S / N Ratio adalah poket halo doktor dos dan mengimbangi dos implan. Sementara itu, S / N nilai Nisbah V_{TH}, I_{ON} dan I_{OFF} selepas pengoptimuman menghampiri untuk pelbagai L_9 adalah 41.30dB, 55.70dB dan -14.17dB respectively. Dalam eksperimen L9, V_{TH}, I_{ON} dan I_{OFF} nilai untuk peranti NMOS selepas pengoptimuman pendekatan yang 0.530V, masing-masing 622.667μA dan 2.776pA. Keputusan yang diperolehi adalah lebih dekat dengan ITRS 2013 ramalan. Sebagai kesimpulan, Taguchi Menghubungi diperhatikan sebagai kaedah yang paling sesuai untuk dilaksanakan dalam pemodelan statistik 19nm WSi2 peranti / TiO2 NMOS.

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LIST OF ABBREVIATION

MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
WSi_2	-	Tungsten Silicide
TiO_2	-	Titanium Oxide
SCE	-	Short Channel Effect
OA	-	Orthogonal Array
V_{TH}	-	Threshold Voltage
I_{ON}	-	Drive Current
I_{OFF}	-	Leakage Current
EOT	-	Equivalent Oxide Thickness

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CHAPTER 1

INTRODUCTION

1.1 Background

In this new technology, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology now become famous in microelectronic industry for almost fifth decade. Because of that, the size of the MOSFET transistor has been decrease continuously through process of scaling validating based on Moore's Law [1]. Scaling down used to ensure the robust performance of transistor because of the user need for minor, quick, and affordable in price. Anyhow, there is some problem to further technology scaling which is short channel cause by expanding the process of fabrication of wafer. This lead to the introducing of high-K material such as Titanium Oxide (TiO_2) [1]. Too many years the uses of Silicon oxide (SiO2) being gate dielectric material. Nowadays, replacing SiO_2 with high-k material as one of the new research initiatives to overcome those problems. Metal gate such as Tungsten Silicide (WSi_2) are used for get rid of Poly-Si depletion which make leakage current are too high [2].

In this project, statistical method is used in order to analyzed the process parameter that impact most on the electrical characteristic especially threshold voltage (V_{TH}). This is because threshold voltage is used to make sure whether the device working well or not. This consumed to better performance of IC. The most popular technique that used as statistical modelling called Taguchi method. This is because Taguchi method has ability to give the closer value to predicted value. Other than that,

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Taguchi method also can verify the process parameter that give big impact on output response such as V_{TH}, I_{ON} and I_{OFF}. The benefit of using Taguchi method than other method is Taguchi method only require small number of experiment but can studied the entire process [3].

1.2 Objective in this research

The objective in this research:

(i) To optimize the process parameter variation and electrical characterization of 19nm WSi_2/TiO_2 using 2k-factorial and Taguchi method.

(ii) To analyze the significant input process parameters which will be impact most on the output responses of WSi_2/TiO_2 MOSFET.

(iii) To obtain the optimum solutions for nano scale MOSFETs device to verify the predicted optimal design.

1.3 Problem Statement

The problem occurs because the further scaling of SiO2 is below 2nm gate layer thickness which can result in a large increase of the leakage current and short channel effect. In order to overcome this problem, many researchers are focusing on the metal gate with high –k materials that have the ability to be integrated in MOSFET flow [3]. Other than that, statistical modelling is one of the method to improve the performance of the ICs [2]. Optimization was the one of the solution to solve the problem related with performance of device without expanding the cost [2]

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1.4 Scope of Project

First and foremost, based on the journal, previous research and reference books will be reviewed in more detail. The literature reviews of this project regarding of objective this project will be covered. This research mainly focused on the optimization of input process parameter variation and performance of electrical characteristics in WSi_2/TiO_2 MOSFET device. This device will be optimized through out of this project using 2-k factorial and Taguchi Method. Virtual fabrication design of WSi_2/TiO_2 MOSFET device will be carried out by using Silvaco ATHENA. The electrical characterization of device is going to be carried out by employing ATLAS. Other than that, there is also important to know more about characteristic of MOSFET in order to get the better value threshold voltage level (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) in International Technology Roadmap Semiconductor (ITRS) 2013 for Low Power (LP) technology requirements of year 2015 prediction [5].

1.5 Organization of Report

This thesis contains five chapter starting from introduction to the research, literature review that related with this research, result analysis and discussion based on the result and lastly the conclusion from the result that have done with the desired future work.

In chapter 1, starting from introduction of this research with explanation little bit about the project and objective to conduct this experiment. After that, followed by chapter 2 which is will discuss about past researcher work that related to this project. The literature review in this research will be focused on statistical modelling since it is the main objective of this project.

In this chapter 3, the project methodology will be discussed in this chapter. All the flowchart and flow of the whole process that related to the statistical modelling. Flow of the process to do optimization using Taguchi method and 2k-factorial will be analyzed in this chapter.

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In chapter 4, the whole result of the modelling process starting from Taguchi method until 2k-factorial design will be analyzed in this chapter. The comparison will be finalized after complete the two process of optimization. Lastly, in chapter 5, the conclusion and future work will be finalized in this chapter.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is a device that has been widely used in the industry. These devices are, such as the digital circuit, microprocessor and memory circuit industry. MOSFET is used as a switch to amplify the electronic signal. The integrated circuit (IC) comprises million numbers of MOSFET devices due to their small size characteristic, and this feature is another advantage of this device to the electronic industry in the world [1]. Since the 1970s the MOSFET has been the prevailing device in microprocessors, memory circuits and logic applications of many kinds. The fabrication process for MOSFET has become very mature over the 25 to 30 year lifetime of this device [3].

A MOSFET is based on the modulation of charge concentration caused by a MOS capacitance. The structure of a MOSFET is shown in Figure 2.1. The MOSFET has two terminals, called source and drain, which are connected to highly doped regions which are separated by a region called the channel. With an insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve) [4]. This region is not so highly doped. The third electrode in the MOSFET, called the gate, is located above the body and insulated from all of the other regions by an oxide (usually an oxide of Si) [6].

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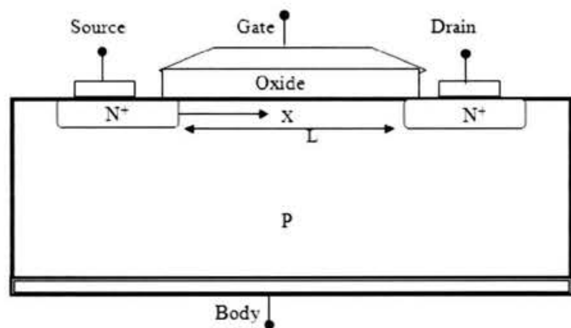

Figure 2.1: Structure of a MOSFET

The source is so named because it is the origin of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel. The MOSFET can be of n-channel or p-channel depending on the doping material in the source and drain of the MOSFET [6].

2.3 Operation Modes in MOSFET

In the case of n-channel MOSFET, when there is no voltage applied to the gate there is no channel formation between source and drain and hence there is no current flow between them. However, when a positive gate-source voltage is applied, it creates a channel at the surface of the p- region which is negatively charged, under the oxide. When a negative voltage is applied between gate and source, the channel disappears and no current can flow between the source and the drain. The operation of a MOSFET can be divided into three different regions, depending upon the voltages at the terminals. The three regions of operation are cutoff, linear and saturation region [6].

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