SUPERVISOR ENDORSEMENT

"I hereby declare that I have read through this report entitle "Generalized Selective Harmonic Elimination Technique for Cascaded H-Bridge Multilevel Inverter" and found that it has comply the partial fulfillment for awarding the degree of Bachelor of Electrical Engineering (Power Electronics & Drive)".

Signature : .....

Supervisor's Name : Puan. Wahidah binti Abdul Halim

Date : ……..

GENERALIZED SELECTIVE HARMONIC ELIMINATION TECHNIQUE FOR CASCADED H-BRIDGE MULTILEVEL INVERTER

KOMATHI D/O APPLASAMY

A report submitted in partial fulfillment of the requirements for the degree of

Bachelor in Electrical Engineering (Power Electronics & Drive)

Faculty of Electrical Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

JUNE 2015

DECLARATION

I declare that this report entitle "Generalized Selective Harmonic Elimination Technique for Cascaded H-Bridge Multilevel Inverter" is the result of my own research except as cited in the references. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : .....

Name : Komathi d/o Applasamy

Date : …….

DEDICATION

To my beloved mother and father

ACKNOWLEDGEMENT

First of all, I would like to thank almighty God for the strength and blessings. I would also like to express my deepest gratitude to my supervisor, Puan.Wahidah binti Abdul Halim and Dr.Auzani bin Jidin for guiding me throughout my final year project development. Knowledge and extra input given by them has highly motivated me to successfully complete this project. The information, suggestions and ideas given by them played huge role in developing a fully functional project.

I would also like to thank my parents for their moral support. Their support gives me the strength to endure this final year project and successfully complete it. Finally, I am also grateful and would like to thank my friends who had helped me directly or indirectly and their help had given me a lot of ideas on troubleshooting the problems that rises during the development of the project.

ABSTRACT

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Multilevel inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the staircase voltage waveform (from several dc sources) which has reduced harmonic content. This report presents an implementation of selective harmonic elimination (SHE) modulation for a single-phase 7-level cascaded H-bridge multilevel inverter. The optimum switching angle of the SHE equations is taken from the reference [45] where Newton-Raphson method is used in solving the transcendental equation describing the fundamental and harmonic components. The proposed SHE scheme is performed through simulation using MATLAB/SIMULINK. This simulation results are then verified through experimental using H-bridge modules, gate drivers and Altera Field Programmable Gate Array (FPGA) controller. The proposed SHE is efficient in eliminating the 3^{rd} and 5^{th} order harmonics and produces a higher quality with a better harmonic profile and sinusoidal shape of the stepped output waveform.

ABSTRAK

Peranti elektronik kuasa yang menukarkan kuasa AT kepada AG pada voltan dan kekerapan tahap yang dikehendaki dikenali sebagai penyongsang. Penyongsang bertingkat muncul sebagai baka baru pilihan penukar kuasa tinggi. Mereka biasanya mensintesis bentuk gelombang voltan tangga (dari beberapa sumber dc) yang telah mengurangkan kandungan harmonik. Laporan ini membentangkan satu pelaksanaan terpilih penghapusan harmonik (SHE) modulasi untuk sistem satu fasa 7 peringkat penyongsang jejambat-H bertingkat. Sudut pensuisan optimum persamaan SHE diambil daripada rujukan [45] di mana kaedah Newton Raphson digunakan dalam menyelesaikan persamaan transenden menerangkan komponen asas dan harmonik. Skim SHE yang dicadangkan dilakukan melalui simulasi menggunakan MATLAB/SIMULINK. Keputusan simulasi kemudiannya disahkan melalui eksperimen menggunakan jejambat-H, pemacu get dan Altera tatasusunan get boleh aturcara medan (FPGA) pengawal. Cadangan SHE adalah berkesan dalam menghapuskan harmonik bagi 3 dan 5 dan menghasilkan kualiti yang lebih tinggi dengan profil harmonik yang lebih baik dan bentuk sinus output gelombang melangkah.

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Research Motivation

In recent years, the research on multilevel inverters have drawn enormous interest and have been studied for high power and medium voltage energy control. There are three commercial topologies of multilevel inverters namely, neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitors (FC). However, the cascaded H-bridge (CHB) has attracted special attention as it gives continuous supply to load even if there is fault in any module and thus it is very reliable [1]. In addition, it reduces the number of components used when compared with NPC or FC, thus the cost of the inverter is less than that of two types.

Generally, modulation techniques of multilevel inverter can be categorized into high-frequency switching and low-frequency switching methods. The multilevel sinusoidal pulse-width modulation (PWM) and space-vector modulation (SVM) techniques are considered high-switching frequency schemes, whereas selective harmonic elimination (SHE) technique falls under low-switching frequency group.

Selective harmonic elimination (SHE) is non-carrier based PWM technique. It is computed offline, where the switching angles are properly selected to eliminate the most significant low order harmonics among different level inverters [2]. Various algorithms have been developed to calculate the switching angles such as the Newton-Raphson (NR) method, genetic algorithms (GA) and the particle swarm optimization (PSO).

This study would mainly concentrate on 7-level cascaded H-bridge (CHB) inverter topology as shown in Figure 1.1. The switching control modulation that proposed in this study is selective harmonic elimination (SHE) technique. Thus, the significant of the study is to prove the SHE technique ability to eliminate the harmonics to any level of output.

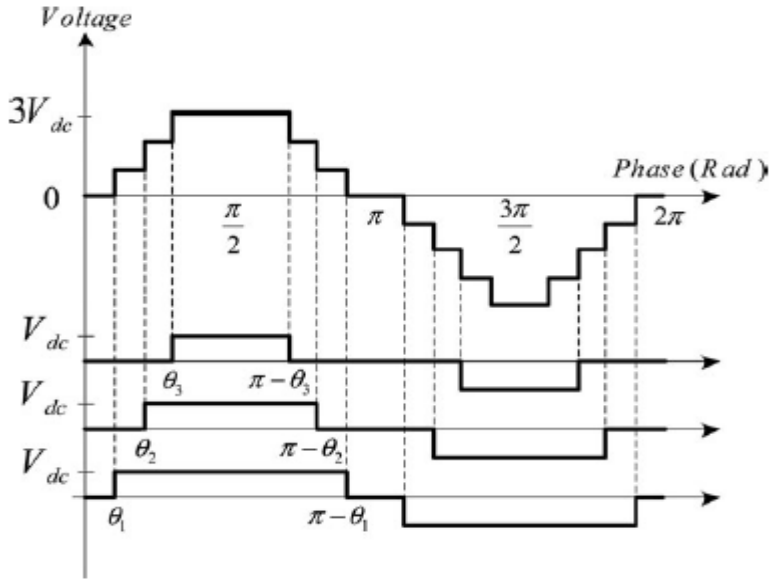

Figure 1.1: The output voltage waveform of 7-level inverter.

1.2 Problem Statement

Inverters are circuits that convert DC to AC. Applications of multilevel inverters are adjustable speed drive, grid-connected photovoltaic system and many more. In other words, multilevel inverter becomes an alternative for high-power medium-voltage energy control. However, the biggest concern of multilevel inverter is the harmonic distortion problem. Generally, the supplied voltage by a power system in any facility is not a pure sine wave. Instead, it usually possesses some amount of distortion, which has a fundamental frequency and harmonics at that frequency as shown in Figure 1.2. These harmonics have high chances to corrupt the data and cause inconsistent equipment performance [3]. Thus, harmonic elimination in multilevel inverters are considered very important task. Suitable control algorithms and modulation technique should be applied to eliminate the harmonic components.

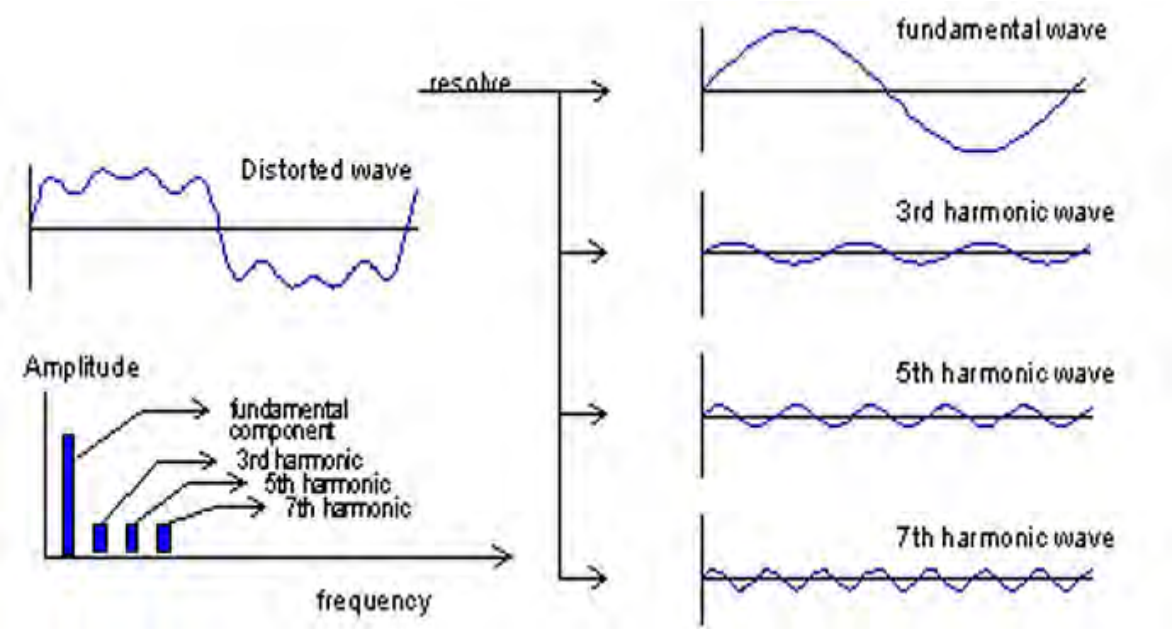

Figure 1.2: Sample of harmonically distorted output waveform [47].

1.3 Project Objective

This study embarks on the following objectives:

i. To generalized selective harmonic elimination (SHE) modulation technique for a single-phase cascaded H-Bridge multilevel inverter with the ability to eliminate low-order harmonics.

ii. To design the SHE control scheme using Altera Field Programmable Gate Array (FPGA) controller.

iii. To develop a single-phase 7-level cascaded H-bridge multilevel inverter prototype in order to implement the SHE technique.

iv. To analyse and verify the SHE method through simulation and experiment.

1.4 Project Scope

This project is mainly concerned to develop multilevel inverter with three H-bridge modules in series using selective harmonic elimination (SHE) technique. The proposed SHE will be able to eliminate 3^{rd} and 5^{th} order harmonics. The optimum switching angle of the SHE equations is taken from the reference [45] where Newton-Raphson method is used in solving the transcendental equation describing the fundamental and harmonic components.

1.5 Report Outline

In first chapter, it gives an overview with commence on introduction of the project, problem statement, objectives, and scopes. In chapter 2, studies on the various topologies available are presented. Chapter 3 presents the methodology of the project that covers the techniques and detailed description of the main components used in hardware implementation. Simulation of the H-bridge cascaded inverter is done up to 7-level and the results are verified and analysed by hardware implementation as shown in chapter 4. Lastly, chapter 5 covers the conclusion of the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter presents the topologies of multilevel inverter such as diode clamped, flying capacitor and cascaded H-bridge. In addition, suitable control switching modulation for these inverter topologies also reviewed in this chapter. It includes sinusoidal pulse-width modulation (SPWM), space vector pulse-width modulation (SVPWM) and selective harmonic elimination (SHE) techniques. Finally, the application of the multilevel inverter technologies are discussed.

2.2 Types of Multilevel Inverters

Generally, multilevel inverter produce sinusoidal output voltage from several levels of DC voltages. The synthesized output waveform has more steps as the number of level increases, which provides a staircase wave that approaches a desired waveform. In addition, as the number of voltage levels increases, the harmonic distortion of the output wave decreases, approaching zero. There are three types of multilevel inverters:

i. Diode Clamped Multilevel Inverter
ii. Flying Capacitor Multilevel Inverter
iii. Cascaded Multilevel Inverter

2.2.1 Diode Clamped Multilevel Inverter

The diode-clamped inverter is the most commonly used multilevel topology for distributed generation such as wind turbine and photovoltaic. The diode clamped inverter uses diode as the clamping device to clamp the DC bus voltage to produce steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress [2]. The major advantages of the inverter are when the number of level is high enough, the harmonic content is low enough to avoid needing to filters. In addition, its efficiency is high because all devices are switched to the fundamental frequency and also simplified control method. However, the main problem with this inverter is the difficulty to control the DC-link capacitor unbalance. The DC input sources must divide equally between the series DC capacitors as the imbalance voltage between series DC capacitors will increase distortion of the output waveforms.

A three-level diode-clamped inverter is shown in Figure 2.1(a) [2] [15]. In this circuit, the DC-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors *n* can be defined as the neutral point. For DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through clamping diodes [29]. There are three switching states for output voltage, V_{an} as illustrated in Table 2.1.

Table 2.1: Switching states of three-level diode clamped inverter.

Output voltage	S_1	S_2	S_1'	S_2'
½ V_{dc}	On	On	Off	Off
0	Off	On	On	Off
-½ V_{dc}	Off	Off	On	On

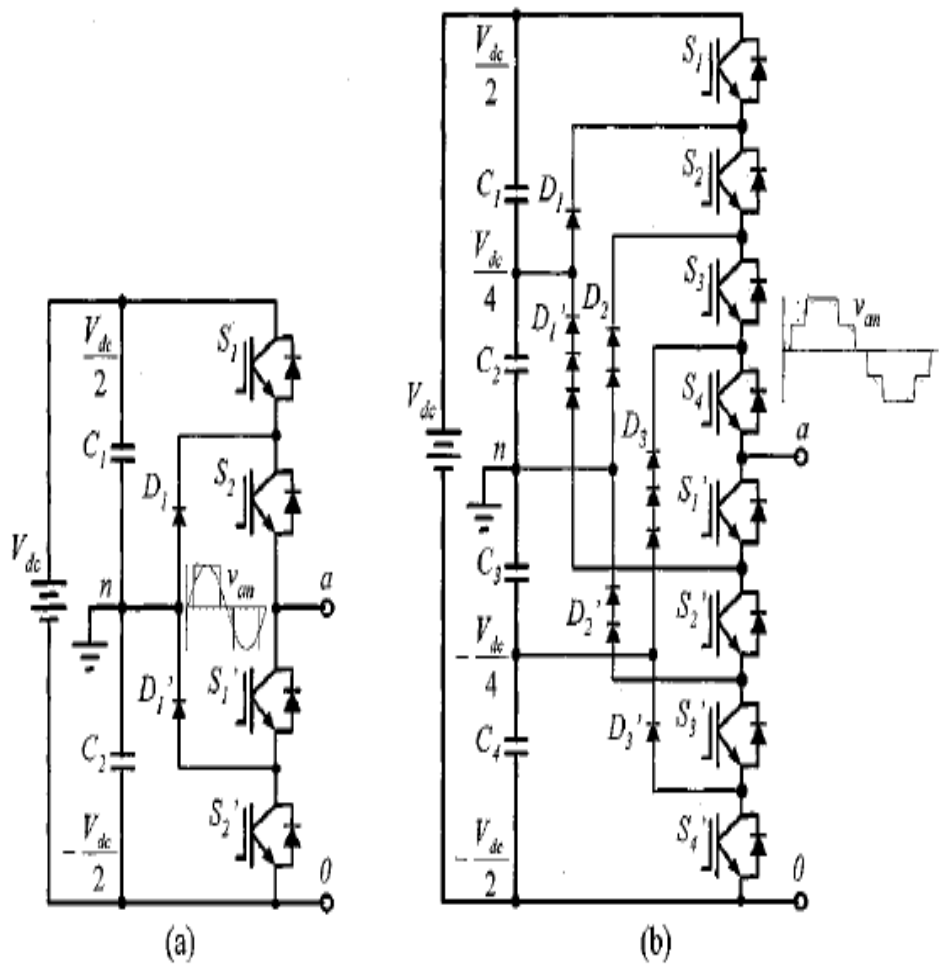

Figure 2.1: Diode-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level [2].

Figure 2.1(b) shows a five-level diode-clamped converter in which the DC bus consists of four capacitors, C_1, C_2, C_3 and C_4. For DC-bus voltage V_{dc}, the voltage across each capacitor is V_{dc} /4, and each device voltage stress will be limited to one capacitor voltage level V_{dc} /4 through clamping diodes [30]. There are five switch combinations to synthesize five level voltages across *a* and *n* as illustrated in Table 2.2.

Table 2.2: Switching states of five-level diode clamped inverter.

S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	Output voltage
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

When the number of output levels is sufficiently high, the inverter system required a huge number of clamping devices due to the series connection of clamping diodes and capacitors. These not only increase the cost of the system, but also controlling the inverter output and capacitor voltage balance becomes more complex when the number of levels is higher than five. Thus, diode clamped inverters are usually limited to three.

2.2.2 Flying Capacitor Multilevel Inverter

The flying capacitor (FC) multilevel inverter has been introduced in 1992 by Meynard. The FC topology is in some way similar to the NPC, with the main difference being that the clamping diodes are replaced by flying capacitors [35], as can be seen in Figure 2.2.

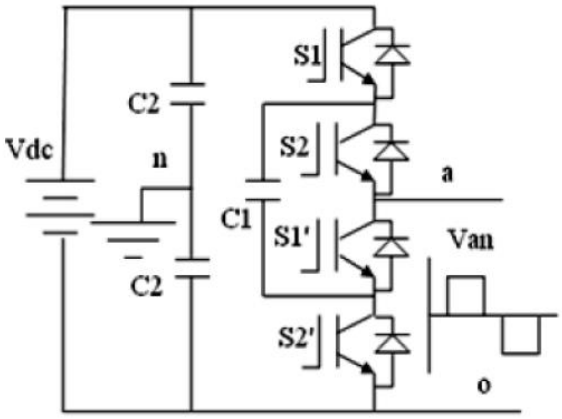

Figure 2.2: Single phase of three-level FC multilevel inverter [2].

Hence, capacitors in this topology can be classified into two parts that are DC-link capacitors and auxiliary capacitors. The number of DC-link capacitor needed in *n*-level FC multilevel inverter can be determined using the formula (*n*-1). Whereas, the number of auxiliary capacitors, N_c required can be calculated as shown in Equation (2.1).

$$N_C = (n-1)(n-1)/2 \tag{2.1}$$

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Figure 2.3 as the example, the voltage of the five-level phase-leg a output with respect to the neutral point n, V_{an}, can be synthesized by the following switch combinations [15] [26].

1) For voltage, $V_{an} = V_{dc}/2$, turn on all upper switches S_1-S_4.
2) For voltage level $V_{an} = V_{dc}/4$, there are three combination:
   a) S_1, S_2, S_3, S_1' ($V_{an} = V_{dc}/2$ of upper C_4's – $V_{dc}/4$ of C_1);
   b) S_2, S_3, S_4, S_4' (V_{an} =3 $V_{dc}/4$ of C_3's – $V_{dc}/2$ of lower C_4's);
   c) S_1, S_3, S_4, S_3' (V_{an} = $V_{dc}/2$ of upper C_4's -3$V_{dc}/4$ of C_3's + $V_{dc}/2$ of C_2's)
3) For voltage $V_{an} = 0$, there are six combination:
   a) S_1, S_2, S_1', S_2' ($V_{an} = V_{dc}/2 - V_{dc}/2$)
   b) S_3, S_4, S_3', S_4' ($V_{an} = V_{dc}/2 - V_{dc}/2$)
   c) S_1, S_3, S_1', S_3' ($V_{an} = V_{dc}/2 - 3V_{dc}/4 + V_{dc}/2 - V_{dc}/4$)
   d) S_1, S_4, S_2', S_3' ($V_{an} = V_{dc}/2 - V_{dc}/3 + V_{dc}/4$)

e) S_2, S_4, S_2', S_4' (V_{an} =3V_{dc} /4- V_{dc} /2+ V_{dc} /4- V_{dc} /2)

f) S_2, S_3, S_1', S_4' (V_{an} =3V_{dc} /4- V_{dc} /4- V_{dc} /4- V_{dc} /2)

4) For voltage V_{an} = - V_{dc} /4, there are three combination:

a) S_1, S_1', S_2', S_3' (V_{an} = V_{dc} /2- 3V_{dc} /4)

b) S_4, S_2', S_3', S_4' (V_{an} = V_{dc} /4- V_{dc} /2)

c) S_3, S_1', S_3', S_4' (V_{an} = V_{dc} /2- V_{dc} /4 - V_{dc} 2)

5) For voltage V_{an} = - V_{dc} /2, Turn on all lower switches S_1'-S_4'.

The optional switching states for voltage levels of V_{dc}/4, 0, -V_{dc}/4 shows switch combination redundancy for balancing different voltage level. This advantage allows the user to select charging and discharging orders of capacitors by constituting proper switching algorithms. The most important advantages of FC multilevel inverter are avoid the need of filter and control the active and reactive power flow. Although these advantages, the increment of level will restrain the accurate charging and discharging control of capacitors. The cost of inverter will increase and device will be more enlarged due to increased number of capacitors [30].

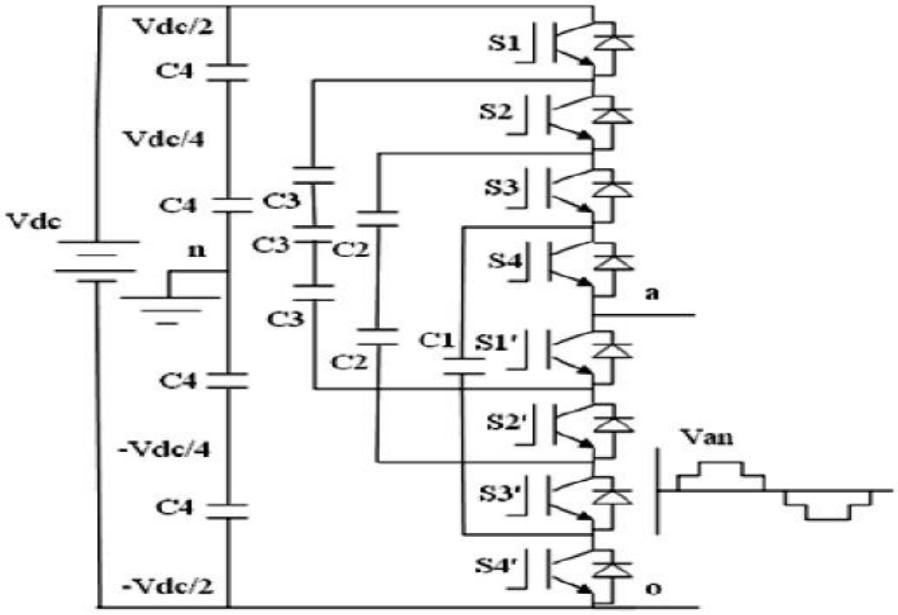

Figure 2.3: Single-phase of five-level FC multilevel inverter [2].

2.2.3 Cascaded H-Bridge Multilevel Inverter

A cascaded multilevel inverter consist of H-bridges inverter units which are connected in series. Mainly, multilevel inverter synthesize a desired output voltage waveform from separate DC sources. The cascaded H-bridge inverter does not need any voltage clamping diodes or voltage balancing capacitors. For real power conversion from AC to DC, the cascaded inverter need separate DC source, where the structure of separate DC source is well suited for various renewable energy sources such as fuel cell [2] [5]. Main advantages of cascaded H-bridge inverter when compared with diode clamped and flying capacitors inverter includes only uses less number of component to achieve the same output voltage level. In addition, optimized circuit layout and packaging are possible because each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors. However, it needs separate DC source for real power conversion somewhat limits its applications [15] [30].

In this topology, each cell has separate DC link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one DC voltage source. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd [23].

Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency. Consider the 7- level inverter as shown in Figure 2.4; it requires 12 IGBT switches and three DC sources. By closing the appropriate switches, each H-bridge inverter can produce three different voltages: $+V_{dc}$, 0 and $-V_{dc}$ as can be seen in Figure 2.5.