UNIVERSITI TEKNIKAL MALAYSIA MELAKA

STRENGTH ANALYSIS OF IC PACKAGE THROUGH THE IMPACT OF DYNAMIC LOAD

This report submitted in accordance with requirement of the Universiti Teknikal Malaysia Melaka (UTeM) for the Bachelor Degree of Manufacturing Engineering (Manufacturing Design) (Hons.)

by

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DECLARATION

I hereby, declared this report entitled "Strength Analysis of Integrated Circuit Package through the Impact of Dynamic Load" is the result of my own research except as cited in references.

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Date : 08TH JUNE 2016

APPROVAL

This report is summited to Faculty of manufacturing Engineering of UTeM as a partial fulfillment of the requirements for the degree of Bachelor of Manufacturing Engineering (Manufacturing Design) (Hons.). The member of the supervisory committee is as follow:

……

(En. Khairul Fadzli Bin Samat)

ABSTRAK

Laporan ini mengkaji kekuatan pakej Integrated Circuit (IC) melalui kesan beban dinamik. Semasa pengeluaran pakej IC, terdapat beberapa kesan yang menjejaskan komponen pakej IC. Kesan dinamik terhadap pin pogo semasa perhimpunan itu boleh menyebabkan retak atau kemek di mana-mana komponen dalam pakej IC. Oleh itu, adalah penting untuk mengkaji agihan tegasan pada pakej IC yang disebabkan oleh kesan dinamik pin pogo itu. Projek ini mengunakan rekabentuk model yang mempunyai ukuran yang khusus. Simulasi unsur terhingga bagi kajian dinamik pada model itu telah dilakukan. Analisis unsur terhingga telah menganalisis menggunakan perisian ANSYS. Keputusan ditumpukan pada penilaian tekanan pada diepad dan chip komponen. Analisis kegagalan dengan menggunakan analisis unsur terhingga adalah berhubung dengan beberapa syarat dan ciri-ciri beberapa kesan pin pogo dalam keadaan dinamik telah diringkaskan. Bagi menyokong keputusan itu, pengesahan diuji dengan ujian fizikal dengan membandingkan ujian analisis dengan ujian fizikal. Analisis pengesahan dalam keadaan tertentu seperti yang sama dengan ujian fizikal telah diperolehi dan itu adalah hasil menujukkan keputusan hampir sama, itu adalah mewakili mengubahan plastik di kawasan kemek.

ABSTRACT

This report investigates the strength of Integrate Circuit (IC) package through impact of dynamic load. During the production of IC package, there are several effects that affected the IC package component. The dynamic impact of the pogo pin during the assembly can cause the crack or dented in any components of IC package. Therefore, it is importance to investigate the stress distribution on the IC package due to the dynamic impact of the pogo pin. This project constituted the design of model based on a specific package dimensions. The finite element simulation of dynamic study on the model had been performed. The finite element analysis had been analyzed using ANSYS software. The results focus on the stress evaluation of the diepad and die component. The failure analysis by using finite element analysis was performed in several conditions and their impact in dynamic condition had been summarized. To support the result, the developed model and boundary conditions had been justified by comparing the analysis test with the physical test. The result from the validation analysis in a specific condition shows good agreement with the dented area of physical test. The finite element simulation result found that there is the indication of plastic deformation on the diepad and represents as a dented area in physical test.

DEDICATION

To my beloved mother and father and brother

KAIRON BEE BINTI MOHAMMAD HUSSAIN
AZIZAN BIN ISMAIL
MUHAMMAD KHAIRUL AZLIZAN BIN AZIZAN

Supervisor

KHAIRUL FADZLI BIN SAMAT

and teammate.

ACKNOWLEDGEMENT

First at all, I would like to express my greatest gratitude to Allah S.W.T., for His will, this project has finished completely. Thousands of thanks to my supervisor, En Khairul Fadzli Bin Samat for his kind and patience, his valuable advices, concern, guidance, time and support throughout the process to completing my degree project.

I would also like to express my sincere gratitude to my parents and family, who had continuously giving out their support financially and emotionally for me to complete my project. Also a lots of thanks to my dearest friends and lectures for all the knowledge, helps and guidance to complete this project.

Last but not least, I have the greatest hope that my degree project, 'Strength Analysis of Integrated Circuit Package through the Impact of Dynamic Load' will give its benefit in Semiconductor Company in the future.

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LIST OF ABBREVIATIONS, SYMBOLS AND NOMENCLATURE

Al	-	Aluminium
Au	-	Gold
DIP	-	Dual In-line Package
DSO	-	Dual Small Outline
EFO	-	Electric flameoff
FBGA	-	Fine-pitch ball grid array
FEA	-	Finite Element Analysis
IC	-	Integrated circuit
PCB	-	Printing circuit board
RPM	-	Rotation per minute
Si	-	Silicon
TCE	-	Temperature coefficient of expansion
>	-	More than
~	-	Nearest
σ	-	Stress
ϵ	-	Strain
τ	-	Torque

CHAPTER 1
INTRODUCTION

In this chapter, it contains a brief explanation about the background of this project which is, "Strength Analysis of Integrated Circuit Package through the Impact of Dynamic Load". This chapter are consists the background of project, problem statement, objective and scope.

1.1 Background

In electronic worlds, integrated circuit (IC) package is a protective package that function to easy the hold and assembly onto printed circuit boards, also defend the devices from crack or damage. In IC package consist of die that function for direct connections to a substrate without an intermediate header or carrier. Three general categories of IC package which are Dual In-line Packages (DIP), Quad Flat Packs and Grid Arrays. All the packages have a body style that scales with pin count, for examples DIP with the two rows of lead on two sides of the package, Quad Flat Packs with leads on all four sides (Figure 1.1) and Grid Arrays that have pins arranged in a grid *(www.electroons.com).*

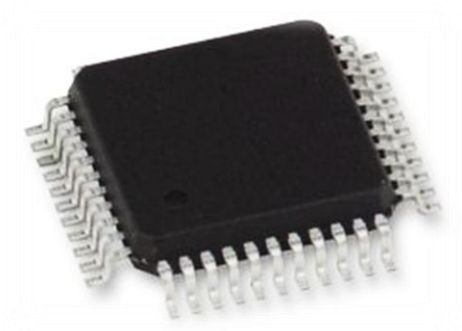

Figure 1.1: Quad Flat Packs once of IC Package Example (www.electroons.com)

Since the IC packages are manufactured by several materials, it will have the certain failure theories. In other hand, the major material use for die/chip is silicon. Silicon is brittle material that has a lower of yielding because of crystal structure. In crystal structure behavior, it will not allow in plastic deformation compare to layer structure. This characteristic will cause the cleavage inside the die when occur by impact of load. Therefore, the properties of die been investigated by experimental or simulation due to different dimension built with advance of technology (Cornelis Klein, 1985).

Pogo pin is used to connect the electrical between IC lead and load board. There are several problems using pogo pin which are indentation marks, blur marks, tilting spring and high cost. It also cause a reliability problems when dealing-pitch packages. The contact of pogo pin and IC package will have the foreign particle that will affect the surface of IC package. There are also several effects that produced by pogo pins which are the force been applied during production and the impact of velocity on the IC package. Therefore, at the end of production the test need to conduct to check the IC package condition. In manufacturing of semiconductor, there were many process that may effects at the end of production. Therefore, the test on IC package had been applied to make sure all requirement connection and performance are fulfilled (M.Idzdihar Idris, 2015).

The physical test shows the visual failure that currently occurs in electronic device. The common tests that have been used in IC package device are point-load test, three-point bending and four-point bending test. These three tests were purpose to investigate the reliability of chip (M.Y. Tsai, 2008).

Free drop test is the method that used to investigate drop test respond and for sight and electrical failures after the drop test. Data from experiment can get the impact of stress wave propagation and distribution to an IC packages (Scott Irving, 2004).

Nowadays, there are many efforts to study a dynamic load using IC packages. Most of them utilize Finite Element Analysis (FEA) by designing it using ANSYS software and can produce better parameter. Using the simulation can faster and

affordably find the state that provides sufficient survivability under different states of condition. This method is used to detect failure stress on the die due to several limitations which are the cost, finding distribution of stress and close assumption to the real impact (Jiang Yuqi, 2005).

1.2 Problem Statement

There are some problem arise during the testing process of IC package as shown in Figure 1.2. Therefore, have a several factors that might be contribute toward to the problem of IC package such as foreign particles, assembly speed, split of pogo pin. The illustration of the factor that effect the IC package are shown in Figure 1.3.

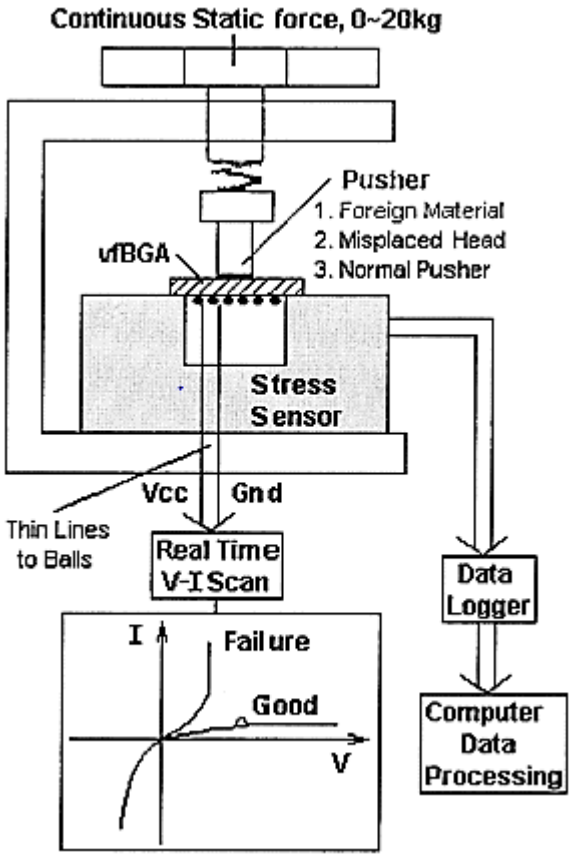

Figure 1.2: Experiment Equipment (Fang Yu, 2002)

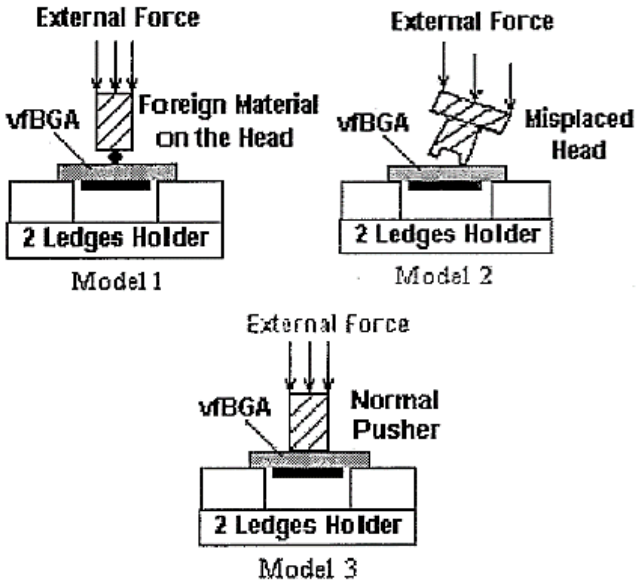

Figure 1.3: Factor that Effect the IC Package (Fang Yu, 2002)

The focus problem of the study was the pogo pin impact on the IC package during test. The high velocity of the pogo pin travel during the test can cause the crack on the IC package because of dynamic impact on the IC package. This is because during test, the IC package in rigid condition and the pogo pin will attach with the velocity that been fix by production. The travel of pogo pin to the IC package area will produce the large inertia force and will cause the impact on IC package. Besides that, the impact of pogo pin during test will cause dented on surface of IC package at once can cause cracked in die. Can IC package sustain with that velocity? Therefore, it is important to investigate the strength analysis of IC package through the impact of dynamic load. In other hands, this analysis also can investigate the stress distribution on the IC package due to the dynamic impact of the pogo pin. This because it can analyze the strength through information of deformation plastic and elasticity of IC package.

1.3 Objective

The aim of this project is to analyze the strength analysis of IC package through the impact of dynamic load. This can be carried out through these objectives:

1. To study the internal stress generated in 3D model of IC package due to dynamic impact of pogo pin.
2. To find out the possibility of die crack in IC package by dynamic impact of pogo pin.
3. To extend the strength analysis of die and diepad on the several conditions.

1.4 Scope

This project constitute the design of model based on package dimension easy to use for analysis. The design of model is conducted using SolidWork software. Before conducting the simulation, the material properties of every component need to be considered. This is because every component have different material. For example die/chip component is made from silicon while mould of IC package is made from EMC-CEL 9220 HF10 V83. Therefore, they will have a different impact while simulation because of it properties. The boundary conditions to apply on IC have to consider the parameters for area, velocity and constrain. The area is to explain the effective contact area of pogo pin and IC package, the velocity act as the speed of the pogo pin move during assembly/test and constrain as a supporting area. The dynamic test will be the main analysis for finite element simulation using ANSYS software. The defects from the process analysis will be analyzed and simulate for the optimum result and minimize the crack on IC package. The result been compared with the existing physical test.

1.5 Project Schedule

Table 1.1 shows the project schedule for PSM 1 that has to achieve according to the plan. There are several identifications and researches have been done for this project. For PSM 1, the model of project has been constructed and the boundary condition of finite element simulation also has been considered. The preliminary result has been analyzed using ANSYS software. Poster presentation for this project and the writing of report from Introduction to Methodology was done according to project schedule.

Table 1.1: Project Schedule for PSM 1

Activities/ Time Scale*		**1***	**2***	**3***	**4***	**5***	**6***	**7***
Problem Identification								
Literature Review								
Development of Model & Boundary Condition of Finite Element(FE) Simulation								
Finite Element Simulation using ANSYS (Preliminary Result)								
Result & Poster Preparation								
Report Writing								

***1 unit = 2 weeks**

Table 1.2 shows the project schedule for PSM 2 that also has to achieve according to the plan. The study of dynamic on several conditions has been done using ANSYS software. The analysis and further evaluation on result have been done according to schedule. Finally report writing be edit and done before due date of submission.

Table 1.2: Project Schedule for PSM 2

Activities/ Time Scale*	**1***	**2***	**3***	**4***	**5***	**6***	**7***
Finite Element Simulation (Dynamic Study on Several Condition)							
Analysis on Result of The Dynamic Study							
Further Evaluation on the Result							
Report Writing							

***1 unit = 2 weeks**

CHAPTER 2
LITERATURE REVIEW

2.1 Overview of IC Package

IC package is a protective package use to cover the inside semiconductor material from damage and crack. Another functions of IC package are to facilitate the packaging and handling of IC chip, to dissipate heat generate by IC package and protect the IC package characteristic. It usually place in circuit boards to the external electronic or electric device. Inside the IC package, there was die that need to been protecting. It the higher in power because of eutectic bonded into the package and made using silicon. It directly glued using adhesive (Diego & Development, 2001).

2.1.1 Type of IC Package

There are three categories of IC package which are Dual In-line Package (DIP), Chip Carriers and Grid Arrays (Figure 2.1). The categories has been classify based on it body style with pin count. If DIP packages with two rows of leads on two side of the package, while Chip Carries are square with leads on all four sides and Grid Arrays those that have their pins in grid arranged (Diego & Development, 2001).

Figure 2.1: Type of IC Package (Diego & Development, 2001)

2.1.2 Component in IC package

There are six component in the IC package which are mould, diepad, die, die attach, wireframe and lead.

2.1.2.1 Mould

Mould function to protect IC package mechanically and environmentally from outside destroyer. Mostly the material been use are plastic because anti corrosion, safety from electrical charge, and low cost. The process of making mould are describe in Figure 2.2, by putting the silicon chip with integrated circuit on a mold and load an epoxy compound a pot. Then after the top and bottom mold been closed with a few tens of clamping tonnage, the compound was pushed by unit transfer and the compound melting flowed into molding area by mold temperature 180°C show clearly in Figure 2.2.After that, slowly the compound came into the molding area because not to bend the wires and not voids. The bottom and top molds keep closing until the compound has been cured. The final stage of molding, the top and bottom mold been opened, taken out molded products, the surfaces of mold automatically cleaned and the molding process completed.

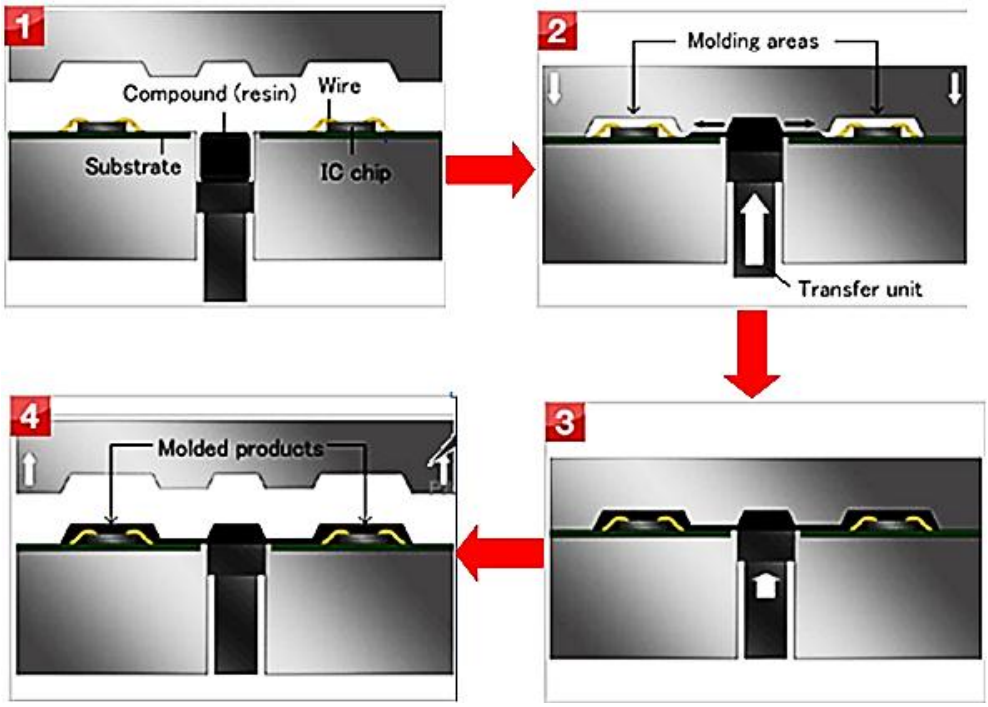

Figure 2.2: Step of Making Mould of IC Package (www.daiichi-seiko.com)

Material that been used were ceramic and plastic packages. It been selected based on their application and operating environment. If ceramic, it has high reliability while plastic most popular because of low cost. IC package classified based on shape, material, and mounting methods (Diego & Development, 2001).

2.1.2.2 Diepad

A resin function to cover the semiconductor chip and semiconductor chip mounted on diepad. Diepad can support chip while a stress applied to the semiconductor device. From the research, it's described that the diepad is formed to be smaller than a semiconductor chip so that can avoid the peeling between the resins and diepad. Diepad also support chip from expanded by stress applied during a wire bonding process. Semiconductor chip mounted on diepad which called part of a leadframe and it set on heat stage. After this stage the leadframe connected to semiconductor chip through wire during wire bonding process. So diepad will support expands by thermal expansion in the wire bonding process. If diepad moves from initial position, the chip or wire will be exposed from the surface of the molding resin.