ELECTRICAL CHARACTERISTICS OF HIGH-K DIELECTRICS FOR THE 19NM GATE LENGTH NMOS DEVICE

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For my beloved father, Mohd Sabki Ibrahim, my beloved mother Norhayati Mohd Lod and my beloved siblings

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ABSTRACT

Aggressive scaling of n-channel metal oxide semiconductor (NMOS) device will increase the transistor density and performance. However, continual gate oxide scaling will require high-k gate dielectric, since the leakage current (I_{OFF}) is increasing with reducing physical thickness of gate oxide (SiO_2). In this project, the effect of high-k dielectrics for electrical characteristic in 19nm NMOS device were investigated. The two electrical characteristics that were considered are threshold voltage (V_{TH}) and I_{OFF}. The device was virtual fabricated by using the ATHENA simulation module while the electrical characteristic response was stimulated using ATLAS module. The performance of Titanium Oxide (TiO_2) and Hafnium Oxide (HfO_2) as high-k dielectric materials with different metal gates such as Tungsten Silicides (WSix) and Titanium Silicides (TiSix) have been made. As conclusion, the TiO_2 has been recognized to be the most suitable high-k dielectric material for metal gate, WSix. This is because TiO_2/WSix device has the lowest leakage current (1.92pA/μm) and the highest drive current (578.8μA/μm) if compare with other devices include SiO_2/Poly device. The result obtained are well within International Technology Roadmap Semiconductor (ITRS) prediction for the year 2015. Moreover, the TiO_2/WSix device has an excellent power consumption due to its higher I_{ON}/I_{OFF} ratio.

ABSTRAK

Pengecilan agresif peranti n-saluran logam oksida semikonduktor saluran -n(NMOS) akan meningkatkan ketumpatan transistor dan prestasi.Walaubagaimanapun, pengecilan beterusan get oksida akan memerlukan *high-k* get dielektrik, kerana arus bocor (I_{OFF}) semakin meningkat dengan mengurangkan ketebalan fizikal get oksida (SiO2). Dalam projek ini, kesan dielektrik *high k* untuk ciri elektrik bagi peranti NMOS 19nm telah disiasat. Kedua-dua ciri-ciri elektrik yang dipertimbangkan adalah ambang voltan (V_{TH}) dan I_{OFF}. Peranti telah difabrikasi secara maya menggunakan modul simulasi ATHENA manakala sambutan ciri elektrik dirangsang menggunakan modul ATLAS. Prestasi *Titanium Oxide* (TiO_2) dan *Hafnium Oxide* (HfO_2) sebagai bahan *high-k* dengan get logam yang berbeza seperti *Tungsten Silicides* (WSi_x) dan *Titanium Silicides* ($TiSi_x$) telah dibuat. Sebagai kesimpulan, TiO_2 telah diiktiraf untuk sebagai bahan high-k paling sesuai untuk get logam, WSi_x. Ini adalah kerana peranti TiO_2/WSi_x mempunyai arus bocor paling rendah (1.92pA/μm) dan arus salir yang tinggi (578.8μA/μm) jika dibandingkan dengan peranti lain termasuk peranti SiO_2/Poli. Hasil lingkungan *International Technology Roadmap Semiconductor* (ITRS)2013 ramalan bagi tahun 2015. Selain itu, peranti TiO_2/WSi_x mempunyai penggunaan kuasa yang sangat baik kerana nisbah I_{ON} / I_{OFF} yang lebih tinggi

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LIST OF SHORT FORM

SHORTFORM	FULL WORDS
BF2	Boron Difluoride
BPSG	Boron Phosphor Silicate Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
D	Drain
DIBL	Drain Induced lowering Barrier
G	Gate
GIDL	Gate Induced Drain Leakage
IC	Integrated Circuit
I_D	Drain Current
IMD	Intel Metal Dielectric
ITRS	International Technology Roadmap for Semiconductor
LPCVD	Low Pressure Chemical Vapour Deposition
NMOS	N Channel MOSFET
PMD	Premetal Dielectric
S	Source
SCE	Short Channel Effect
TCAD	Technology Computer Aided Design
v_D	Drain Voltage
v_{DS}	Drain to Source Voltage
v_G	Gate Voltage
v_{GS}	Gate To Source Voltage
v_S	Source Voltage

v_{sub}	Sub Threshold Voltage
v_{th}	Threshold Voltage

CHAPTER 1

INTRODUCTION

1.1 Background

With new technologies, many industries to rely on a manufacturing of smaller, faster, cheaper and good quality of the MOSFET. With increasing global competition, modern industries have to adapt their production process to be more efficient and competitive. In order to more advanced technologies have to employ to scale down the MOSFET into nanoscale [1]. Silicon oxide (SiO_2) has been used as the gate dielectric material over the years. Nowadays, high-k dielectric is widely accepted as a better approach for the gate dielectric of the MOSFET.

In this project, the fundamental understanding of the physical and the electrical characteristics of the 19nm gate length NMOS device containing high dielectric constant will be investigated. For this project, the performance of high-k dielectric Titanium Oxide (TiO_2) will be compared with SiO_2 as gate dielectric. Besides, design nanoscale of NMOS transistor device using ATLAS module in generating the current-voltage (I-V) Characteristic, structure and the value of threshold voltage. Meanwhile, the NMOS transistor will be stimulated by using fabrication tools ATHENA module SILVACO software. In order to know how it is a good affected on the electrical characteristics of 19nm gate length NMOS device.

1.2 Objectives of this project

The objectives of this project are:

i) To design the 19nm gate length NMOS device by using SILVACO TCAD Tools.

ii) To analyze the effect of high-k dielectrics for electrical characteristic of 19nm NMOS devices.

iii) To compare the performance of Titanium Oxide (TiO_2) and Hafnium Oxide (HfO_2) as high-k dielectric with Silicon Oxide (SiO_2) dielectric with different metal gate which are Titanium Silicides ($TiSi_x$) and Tungsten Silides (WSi_x)

1.3 Problem Statement

In trend of global competition, modern industries have to adjust their production process to be more efficient and competitive. Regarding that, more advanced technologies have to employ to scale down the MOSFET into nanometer. A few decades ago, SiO_2 known as widely used as the gate dielectric material and it requires the film thickness to be as thin. However, the further scaling of SiO_2 is below 2nm gate layer thickness which can result in a large increase of the leakage current and short channel effect. In order to overcome this problem, many researchers are focusing on the metal gate with high –k materials that have the ability to be integrated in MOSFET flow. Among the high-K materials are compatible with silicon and also materials have too low or high dielectrics constant may not be an adequate choice for alternative gate dielectric [1]. Therefore, replacing the SiO_2 with a high-K materials allows increased gate capacitance [2].

1.4 Scope of Project

First and foremost, based on the journal, previous research and reference books will be reviewed in more detail. The literature review of this project regarding of objective this project will be covered. The physical and electrical characteristics of

19nm gate length NMOS device will be learned through out of this project. During this project, TiO_2 and HfO_2 will be used as the material gate dielectric with gate oxide thickness is scaled to get the same Equivalent Oxide Thickness (EOT) for physical models of 19nm NMOS. Besides, process design of the NMOS device also will be learned. Then, the virtual design and fabrication of the device will be performed by using Athena module. Meanwhile, electrical characteristic performance will be stimulated by using an Atlas module of SILVACO software.

1.5 Report Structure

This thesis is a combination of five chapters that contain the introduction, literature review, methodology, result and discussion and the last chapter is the conclusion and recommendation of the project.

Chapter 1 is an introduction to the project. In this chapter, we will explain the background and objectives of the project. The concept behind the project and an overall overview of the project also will be discussed within this chapter. Chapter 2 discuss about the literature review of the effect of high-k dielectric value based upon previous research done.

Chapter 3 will explain about the project methodologies of the project. This chapter will show the steps and flow for problem solving in such a specific method used to design and develop the NMOS MOSFET structure, also the other factor and characteristic need to be focused on.

Chapters 4 describe the expected result from this project and justify its performance to make sure it meets the objectives of the research. Finally, Chapter 5 concludes the whole research and proposes the future progress of the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

MOSFET stands for Metal-Oxide Semiconductor Field-Effect-Transistor. MOS (Metal-Oxide-Semiconductor) shows the basic physical device materials. The metal is used for contact electrodes and interconnections, the oxide is present for barriers. For developing the characteristics the isolation and semiconductor substrate with a specified doping profile provides the necessary physics. A MOSFET is referred at as a unipolar device because the nature of its design it. Specifically, the majority carriers in the channel region can be of only one type (electrons or holes). The MOSFET with electrons as the majority carriers in the channel is entitled a n-channel MOSFET or NMOS. Similarly, the MOSFET with holes as the majority carriers in the channel is a p-channel MOSFET or PMOS [3].

Since the 1970s the MOSFET has been the prevailing device in microprocessors, memory circuits and logic applications of many kinds. The fabrication process for MOSFET has become very mature over the 25 to 30 year lifetime of this device [3]. These mature fabrication processes leads to less errors and variances in circuit construction and gives rise to a higher yield of good devices. Size cost reduction has followed the MOSFET through its history. In the initial stages of

the MOSFETs development at 10-micron gate length was a standard design goal [3]. This length would prove to decrease significantly as time past with engineers striving to increase speed and component count per unit area. The gate length (the natural measure of the device technology) has been reduced by a factor 2 about every 5 years [3]. Since 2001, when bulk MOSFET was fabricated with the technology node of 130 nm by Intel as Under this technology, the device was produced using gate length and oxide thickness of 60 nm and 1.5 nm respectively.

2.2 Basic Mosfet Structure

The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semi conductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes. The gate of a junction field effect transistor (JFET) must be biased in such a way as to reverse-bias the pn-junction. With an insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve). This makes the MOSFET device valuable as electronic switches because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices [4].

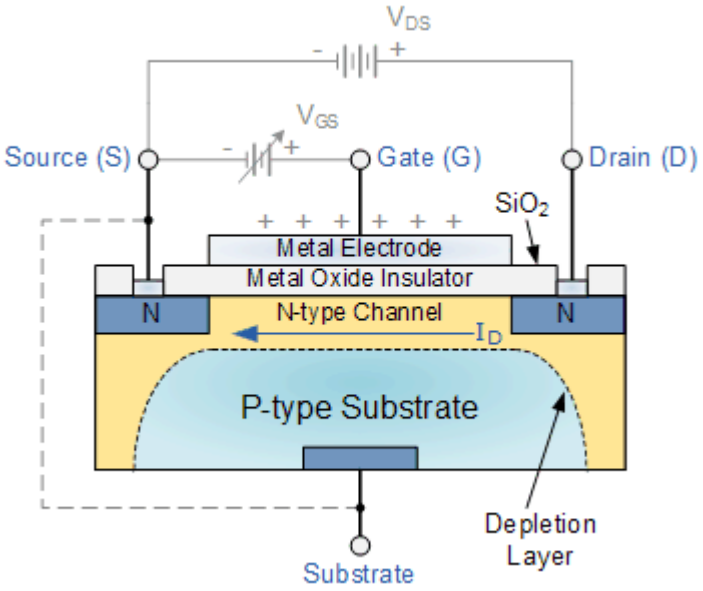

Figure 2.1: MOSFET Structure

2.3 Types of MOSFET

Both the p-channel and the n-channel MOSFETs are available in two basic forms, which are the Enhancement type and the Depletion type. Figure 2.2 shows the channel and symbol of n-channel MOSFET and p-channel MOSFET [4].

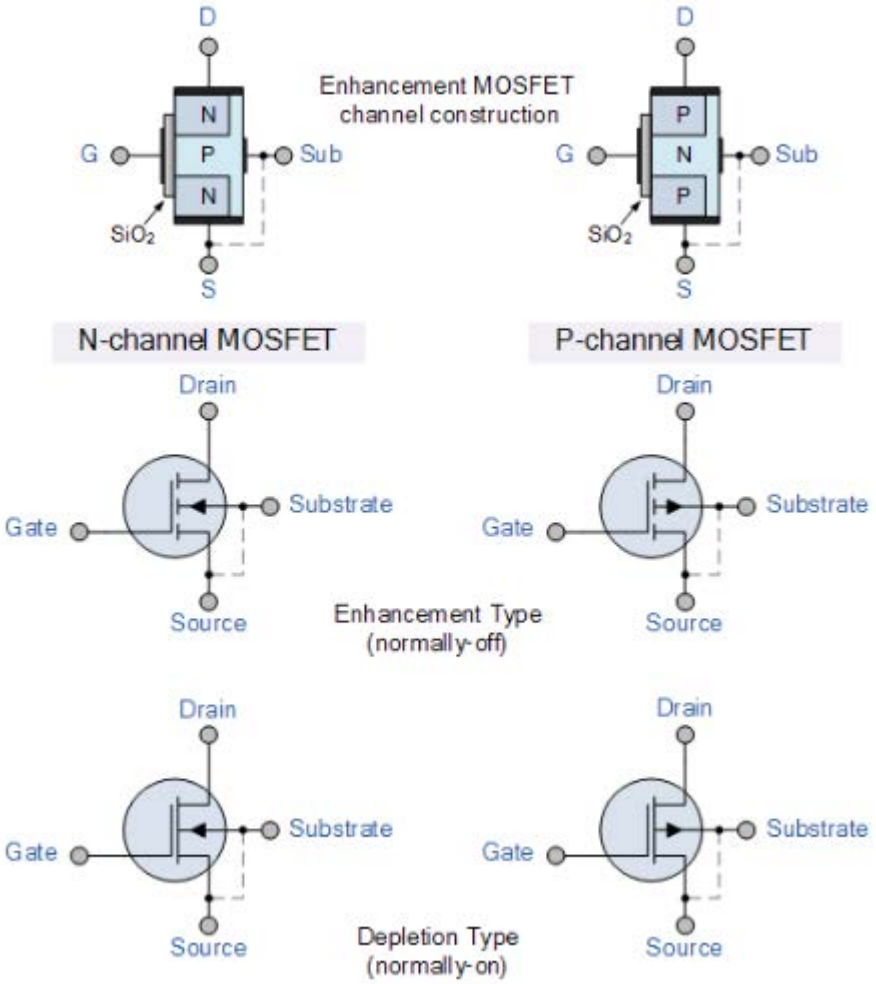

Figure 2.2: Channel and Symbols of n-channel MOSFET and p-channel MOSFET

2.3.1 Depletion-mode MOSFET

The Depletion-mode MOSFET, which is less common than the enhancement mode types is normally switched "ON" (conducting) without the application of a gate bias voltage. That is the channel conducts when V_{GS}=0V makes it a 'normally-closed' device. The circuit symbol shown in Figure 2.2 for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel. For the n-channel

depletion MOS transistor, a negative gate-source voltage ($-V_{GS}$) will deplete (hence its name) the conductive channel of its free electrons switching the transistor 'OFF'. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage ($+V_{GS}$) will deplete the channel of its free holes turning it 'OFF'. In other words, for a n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. Meanwhile a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a 'normally-closed' switch. The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain (D) and Source (S) with zero Gate (G) bias. Figure 2.3 shows graph of drain current (I_D) versus drain voltage (V_{DS}) for n-channel MOSFET device [4].

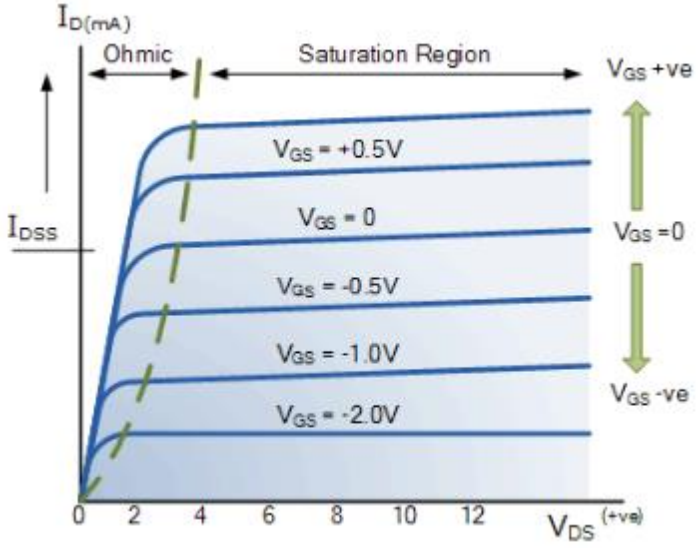

Figure 2.3: I_D-V_{DS} graph n-channel MOSFET