ANALYSIS OF 20NM SOI NMOS DEVICE WITH DIFFERENT GATE SPACER DIELECTRIC

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This Report Is Submitted In Partial Fulfillment of the Requirements for the Award of Bachelor of Electronic Engineering (Computer Engineering) With Honors

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka

June 2016

UNIVERSTI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN
PROJEK SARJANA MUDA II

Tajuk Projek : ANALYSIS OF 20NM SOI NMOS DEVICE WITH DIFFERENT GATE SPACER DIELECTRIC

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Special dedication to my loving parents, Mr. Mohd Daud bin Ajmain and Mrs. Ruslimah binti Markasan, my lovely supervisor, Dr. Fauziyah Salehuddin and thanks to my dearest friends.

ACKNOWLEDGEMENT

After an intensive period of two semesters, today is the day: writing this note of thanks is the finishing touch on my thesis. It has been a period of intense learning for me, not only in the technical arena, but also on a personal level. Writing this thesis has had a big impact on me. I am grateful to my true self for not giving up for this challenge is real. I would like to reflect on the people who have supported and helped me so much throughout this period.

I would first like to express my gratitude to the greatest ALLAH S.W.T for the mercy, blessing and strength given to me to complete this thesis writing and final year project within the time range given. With HIS consent, I was be able to complete this thesis and the project.

My special thanks go to my dedicated supervisor and co-supervisor Dr. Fauziyah binti Salehuddin, Dr. Anis Suhaila binti Mohd Zain, who always provides good supervision, encouragement , valuable guidance and moral support to complete this project and thesis.

My deepest appreciations also go to my beloved parents for their support and endless encouragement throughout my studies. They have been a wonderful source of support, inspiration, finance and encouragement throughout my education , and they deserve much credit for where I am today.

Next, I thanked to all the persons that involved directly and indirectly in this project with full of willingness in contributing their efforts, time, energy and idea in helping me completes this thesis.

ABSTRACT

As scaling down MOSFET devices degrade device performance in term of leakage current and short channel effects. To overcome the problem a Silicon-on-Insulator (SOI) NMOS device has been introduced. Several investigations will be done to reduce the SCE in 20nm SOI NMOS device. This project execution is based on simulation and program development of the device. Simulation of this device fabrication is being performed by using ATHENA module while the simulation of electrical characteristics is being implemented by using ATLAS module from Semiconductor TCAD tools. Semiconductor TCAD tools are computer programs which allows for the creation, fabrication, and simulation of semiconductor devices. This work is also facilitating for the improvement of performance of 20nm SOI MOSFET using high-k gate spacer dielectric. Throughout this project, it has been proved that High-k spacer provides higher transconductance than conventional SiO_2 spacer. It also provides higher voltage gain, so SOI MOSFET devices with high-k spacer can be use for amplification purpose. Also I_{ON}/I_{OFF} is higher in case of high-k spacer. High-k spacer improve short channel effects by improving subthreshold slope than conventional SiO_2 spacer. So, high-k gate spacer is better option for coming SOI MOSFET devices.

ABSTRAK

Pengecilan peranti MOSFET menjejaskan prestasi peranti dari segi efek saluran pendek dan kebocoran arus. Bagi mengatasi masalah itu peranti (SOI) NMOS Silicon-on-Insulator telah diperkenalkan. Beberapa penyiasatan akan dilakukan untuk mengurangkan SCE dalam 20nm peranti SOI NMOS. Pelaksanaan projek ini adalah berdasarkan kepada simulasi dan program pembangunan peranti. Simulasi fabrikasi peranti ini dilakukan dengan menggunakan modul ATHENA manakala simulasi ciri-ciri elektrik dilaksanakan dengan menggunakan modul ATLAS dari alat TCAD Semiconductor. Semiconductor TCAD adalah program komputer yang membolehkan penciptaan, fabrikasi, dan simulasi peranti semikonduktor. Kerja ini juga memudahkan untuk memperbaiki prestasi 20nm SOI MOSFET menggunakan High-k pintu spacer dielektrik. Sepanjang projek ini, telah terbukti bahawa High-k spacer mempunyai transkonduksi lebih tinggi daripada konvensional SiO_2 spacer. Ia juga menyediakan gandaan voltan yang lebih tinggi kepada peranti MOSFET SOI dengan High-k spacer untuk tujuan pembesaran. juga I_{ON} / I_{OFF} adalah lebih tinggi dalam kes High-k spacer. High-k spacer meningkatkan kesan saluran pendek dengan menambahbaikkan voltan ambang daripada konvensional SiO_2 spacer. Jadi, High-k pintu spacer adalah pilihan yang lebih baik untuk datang peranti SOI MOSFET.

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LIST OF ABBREVIATION

MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
IC	-	Integrated Circuit
SCE	-	Short Channel Effect
SOI	-	Silicon On Insulator
TCAD	-	Technology Computer Aided Design
CMOS	-	Complementary Metal-Oxide Semiconductor
VTH	-	Threshold Voltage
DIBL	-	Drain Induced Barrier Lowering
BOX	-	Buried Oxide
STI	-	Shallow Trench Isolation
CVD	-	Chemical Vapor Deposition
Al_2O_3	-	Aluminium Oxide
HfO_2	-	Hafnium Oxide
TiO_2	-	Titanium Oxide
ZrO_2	-	Zirconium Oxide
Si_3N_4	-	Silicate Nitride
I_{ON}	-	Drive Current
I_{OFF}	-	Leakage Current
g_m	-	Transconductance
I_D	-	Drain Current
V_G	-	Gate Voltage
k	-	Permittivity
ALD	-	Atomic Layer Deposition
ITRS	-	International Technology Roadmap for Semiconductors

CHAPTER 1

INTRODUCTION

1.1 Background

In this era of technology, the widespread use of chip has been trigger the device functionality, which makes it a major component in the modern computers and electronic devices such as mobile phones, digital watches and calculators. MOSFET which is stand as Metal Oxide Field Effect Transistor, has the major advantage that it uses low power for accomplishing its purpose and the little dissipation of power loss. Every transistor placed in a transistor need to be as small as possible in order to fit in the limited size of chip. As the time passed, the chip become smaller and according to that, a downscaling process needs to be done on MOSFET. The purpose of this process is to load more transistor on its smaller chip area. In the mean time, this will cut cost of the process of fabrication. This is because, the cost needed is related to the cost per integrated circuit (IC) and the number of chips per wafer. As the number of chips increase, the size of IC and the cost of fabrication decrease. The technology is expected to continue its historical advancing rate with Moore's law for a couple of decades although there are many constraints ahead. The exponential increase of number of transistors on an integrated circuit over time was first predicted by Moore's Law (as shown in Figure 1.1). With this trend, the silicon gate oxide will be scaled down to its physical limit to keep the proper functioning of the transistors in the sub-10 nm technology node.

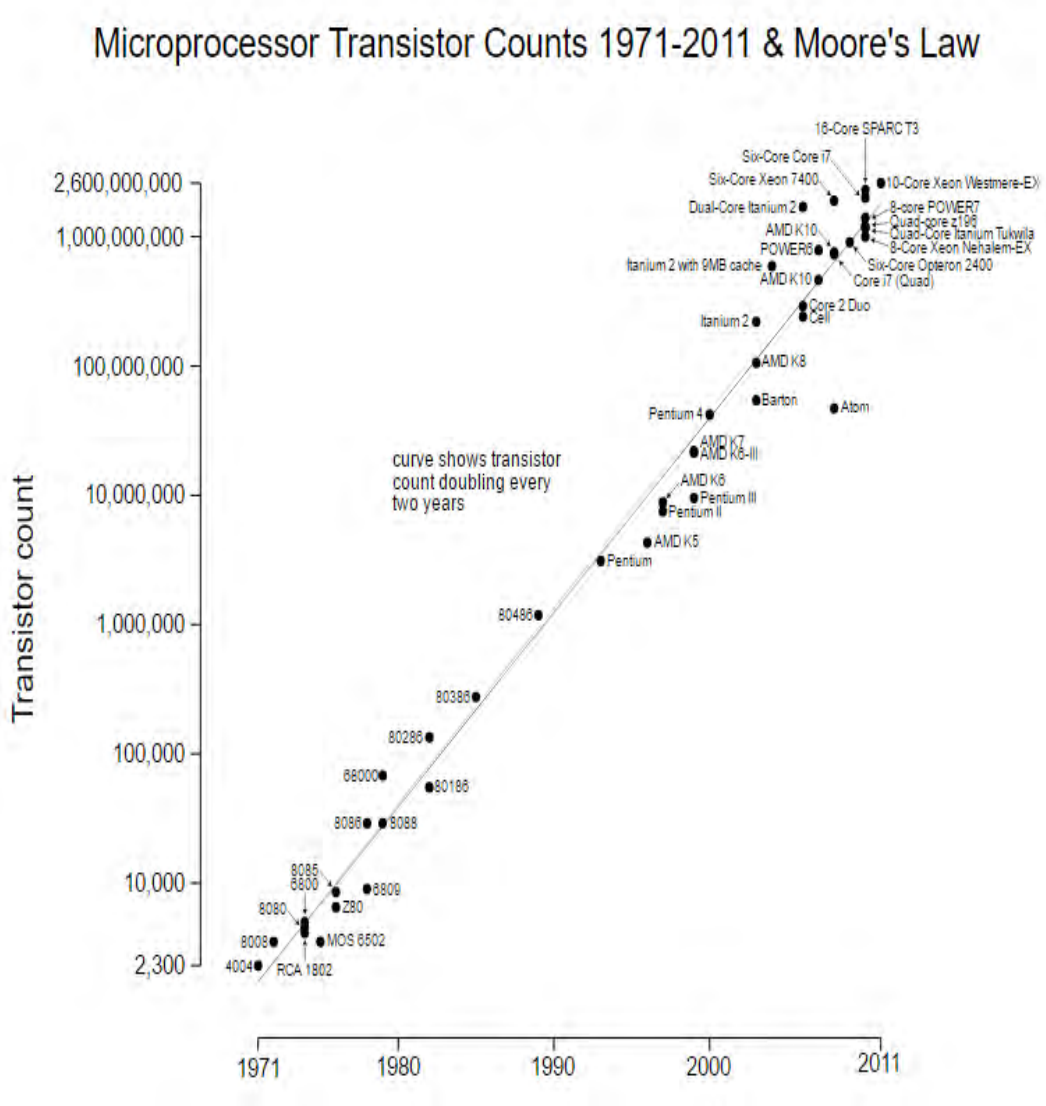

Figure 1.1: Enhanced performance Trend as predicted by Moore's Law [19].

To continue the downward scaling, high-k dielectric materials are currently in consideration for gate dielectric in MOSFET devices which play a major role in affecting threshold voltage (VT). As the name suggest, these material have high dielectric constant (high-k) which improves the oxide capacitance, has low gate leakage current thus providing better stability to the device. Besides, due to the degrading device performance in term of the Short Channel Effects (SCE) and leakage current, the Silicon On Insulator (SOI) has been introduced to overcome the problem. In addition, several investigation has been done to reduce the SCE in 20nm SOI NMOS device.

Dielectric materials with high dielectric constants are used as gate dielectric in MOSFETs. The dielectric materials examined in this study in detail are hafnium oxide and titanium oxide. High-k dielectric material gives high value of oxide capacitance (Cox) which may influence the threshold voltage (VT) and working of the device. The dielectric constants of these materials totally depend upon the way they are deposited over the silicon substrate. The dielectric layers with higher electrical permittivity are used for thicker films to reduce the leakage current and improve upon the reliability of the gate dielectric layer with electrical thickness equal to ultrathin SiO2 layer.

There are some of High-k dielectric material properties and challenges. High-k dielectric materials are chosen with properties such as high permittivity, high barrier height, reduce the leakage current, lower the power consumption, lower direct tunneling effect, stable over silicon substrates, compatible with the gate metal, and have compatibility with process.

The challenges of high-k dielectric material are mobility degradation, fixed charges, hot carrier effects due to reduced energy barrier for electrons and holes, diffusion of oxygen and dopant on to the silicon substrate, charge trapping and threshold voltage (VT) shifts.

This project execution is based on simulation and program development of the device. Simulation of this device fabrication is being performed by using ATHENA module while the simulation of electrical characteristics is being implemented by using ATLAS module from Semiconductor TCAD tools. Semiconductor TCAD tools are computer programs which allows for the creation, fabrication, and simulation of semiconductor devices.

1.2 Objectives of study

The main goal of this research is to design 20nm SOI NMOS. Specifically, the objectives are:

i. To analyze the characteristic of 20nm SOI NMOS device in term of leakage current and short channel effects using Silvaco ATLAS module.
ii. To analyze the performance of 20nm SOI NMOS device with different gate spacer dielectric.

1.3 Problem Statement

The silicon industry has been scaling down silicon dioxide (SiO2) aggressively for the past 15 years for low power, high performance CMOS transistor applications [1]. This is also degrading the device performance in term of leakage current and Short Channel Effects (SCE) [2]. A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (*x*dD, *x*dS) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise. [3].

1.4 Scope of Project

The scope of this project is to design and develop the process to down scale the n-channel MOSFET device. The software used are ATHENA and ATLAS in SILVACO TCAD TOOLS whereby tools to be used to create simulations of the devices being worked on. ATHENA is for fabrication process while the ATLAS is for electrical characteristics. All the literature review about gate spacer dielectric High-k materials and Silicon In Insulator (SOI) devices are covered. High-k dielectric is widely used for nano-scale device performance improvement, due to its reduced off state leakage and enhanced electrostatic control over the channel [4]. It has been found that, due to the presence of high-k dielectric, the major short channel device controls subthreshold slope

and off state leakage is reduced as compared to conventional SOI MOSFET having low-k(SiO2) gate and spacer dielectric [4].

1.5 Report Structure

This thesis is a combination of five chapters that contain the introduction, literature review, methodology, result and discussion and the last chapter is conclusion and recommendation of the project.

Chapter 1 is an introduction to the project. In this chapter, the background and objectives of the project will be explained. The concept behind the project and overall overview of the project also will be discussed within this chapter. Chapter 2 is about the literature review of the effect of High-K Materials gate spacer dielectric on VTH and SOI impact on the SCE and leakage current based upon previous research done.

Chapter 2 contain literature review on past study about SOI, High-k materials and any relevant information related to SOI, High-k materials in terms of leakage current and SCE researches around the world.

Chapter 3 will explain about the project methodologies of the project. This chapter will show the steps and flow for problem solving in such a specific method used to design and develop the MOSFET structure, also the other factor and characteristic need to be focused on.

Chapter 4 is about the progress result throughout the semesters and its discussion of findings. Discuss the particular result obtain and do the mini conclusion of the result.

Chapter 5 is the last chapter will be describing about conclusion of this analysis. The output and what is the best materials in High-k and reccomendation of project in the future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is by far the most prevalent semiconductor device in ICs. It is the basic building block of digital, analog, and memory circuits. Its small size allows the making of inexpensive and dense circuits such as giga-bit (Gb) memory chips. Its low power and high speed make possible chips for gigahertz (GHz) computer processors and radio-frequency (RF) cellular phones [5]. MOSFETS are transistors which contain four terminals, namely the gate, body, source and drain. When a sufficient voltage is supplied from the gate to the body terminal, an electrical connection is opened between the source and the drain terminals [6].

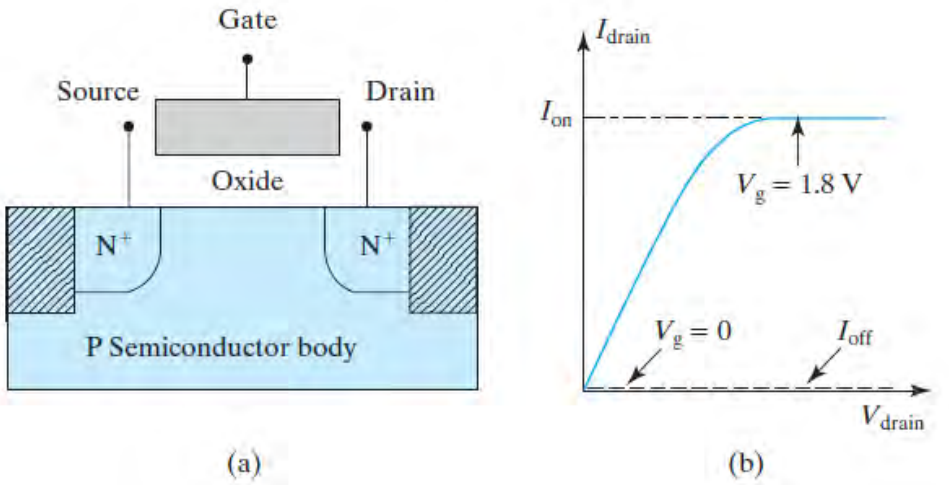

Figure 2.1: (a) Basic MOSFET structure and (b) IV characteristics [5]

MOSFETs operate in one of three stages: 1) Cut-off mode, 2) Triode mode, or 3) Saturation mode. During the cut-off mode, the gate source voltage is insufficient to activate the transistor and the connection between the source and drain terminals remain closed. During the triode mode the gate voltage is enough to establish a weak connection between the source terminal and the drain terminal. In this mode the transistor acts like a resistor whose resistance is a function of the voltage applied to the gate terminal. Finally, when sufficient voltage is applied to the gate terminal the transistor enters saturation mode and a full connection is established between the source and drain terminals [6].

2.2 Down Scaling

MOSFET technology is well-known in the industry, especially for switching application. It has been used widely since the early 60-70s. There have been a lot of gains in the performance of the MOSFET device since their size dimension keeps decreasing. [7]. Ingenious engineering has allowed its size to be shrunk again and again without change to its structural design. Yet the IC design window of performance, dynamic power, static power, and device variation has shrunk to the point that major investment for a new transistor structure can be justified. As gate length shrinks, MOSFET's Id-Vg characteristics degrade in two major ways. First the sub threshold swing degrades and Vt decreases [8].

CMOS technology scaling has been a basic key for continuous progress in silicon-based semiconductor industry. Scaling is followed by Moore’s Law since few decades which provided simple rules for transistor design to increase circuit density and speed. The improved circuit performance and density enable more complicated functionality, since more transistors can be integrated on one single chip. However, as

device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance followed by Moore's Law cannot be maintained only by the conventional scaling theory. Increasing leakage current does not allow further reduction of threshold voltage, which in turn prevents further supply voltage scaling for the speed improvement. Higher electric fields generated inside of the transistor worsen device reliability and increase leakage currents. Moreover, the required high channel doping causes significant challenges such as mobility degradation and random dopants induced threshold voltage fluctuations [9].

In addition, various researches have been actively carried out in device domain to find an alternative device to continue to sustain Moore's Law. Among these efforts, various kinds of alternative memory and logic devices (beyond CMOS devices) have been proposed. These nano devices take advantages of the quantum mechanical phenomena and ballistic transport characteristics under low supply voltage and consume low power. Furthermore, due to their extremely small sizes, those devices are expected to be used for ultrahigh density integrated electronic components having billions of devices in a single chip. However, it also increases defects and variations both during manufacture and chip operations [10].

The success of modern integrated circuits has been realized with continuous shrinkage of MOS transistors (Figure 2.2)[15]. The tininess of transistors has not only increased package densities, but also accelerated circuit speed and reduced power dissipation.

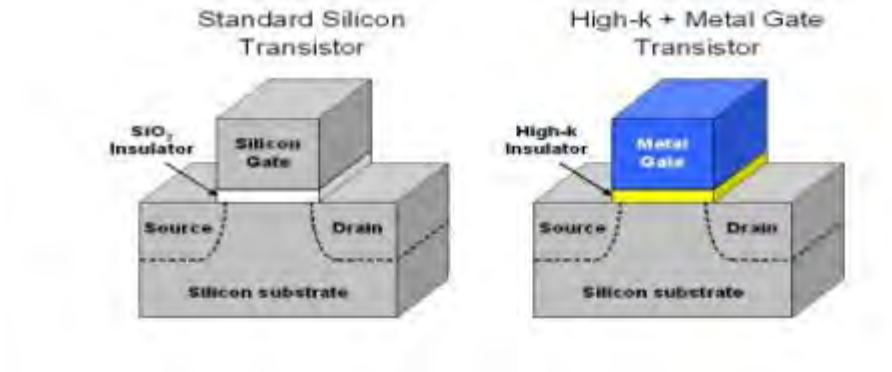

Figure 2.2: MOS transistor structure with dielectric gate [15].