DESIGN AND DEVELOPMENT OF A LOW POWER COMPACT INTEGRATED PROCESSOR OF AN EMBEDDED SYSTEM

SAM SENG YANG

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Disahkan oleh:

(TANDATANGAN PENULIS)

(COP DAN TANDATANGAN PENYELIA)
Dr. WONG YAN CHIEW
Pensyarah Kanan
Fakulti Kejuruteraan Elektronik & Kejuruteraan Komputer
Universiti Teknikal Malaysia Melaka
Hang Tuah Jaya
76100 Durian Tunggal, Melaka

Tarikh: 10 JUNE 2016

Tarikh: 10/06/2016

"I hereby declare that the work in this project is my own except for summaries and quotations which have been duly acknowledge."

Signature : 

Author : SAM SENG YANG

Date : 10 JUNE 2016

"I acknowledge that I have read this report and in my opinion this report is sufficient in term of scope and quality for the award of Bachelor of Electronic Engineering (Industrial Electronics/ Computer Engineering/ Electronic Telecommunication/ Wireless Communication) * with Honours."

Signature : .....

Supervisor's Name : DR WONG YAN CHIEW

Date : 10/06/2016

Dedicated to my beloved family, for your love and supports.
To my friends, for your wits, intelligence and guidance in life.

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ABSTRACT

Microprocessor without Interlocked Pipeline Stages (MIPS) is a popular implementation of a Reduced Instruction Set Computer (RISC). MIPS architectures are typically 32-bit, but 64-bit versions have been developed in more recent years. The demands for low cost and low power consumption are the characteristics to embedded processors. This project is to design and develop an integrated processor of an embedded system with low power consumption. Verilog language is used to design and construct the modules of processor in this project. There are two type of simulations tools which are Synopsis and Vivado are used to simulate the designs. This project will focus on designing a simple 16-bit Central Procession Unit (CPU) with onboard Static Random Access Memory (SRAM) memory. The designed processor is developed into a layout with 0.18μm Silterra process technology. The developed processor is compared to DW8051 core with the analysis on timing, power consumption and area of the core. A comparison between Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C) is done and developed to layout with the same process technology. The analysis of the processor is based on the timing, power and area that generated from the simulation. The developed processor should be effective yet simple that fulfills the features required in a modern embedded system but without too much unnecessary complexity.

ABSTRAK

Mikropemproses tanpa Peringkat Kuncikait Pipeline (MIPS) adalah pelaksanaan popular di Instruction a Mengurangkan Set Komputer (RISC). senibina MIPS biasanya 32-bit, tetapi versi 64-bit telah dibangunkan dalam tahun-tahun kebelakangan ini. Tuntutan untuk kos rendah dan penggunaan kuasa yang rendah adalah ciri-ciri kepada pemproses terbenam. Projek ini adalah untuk mereka bentuk dan membangunkan pemproses bersepadu sistem terbenam dengan penggunaan kuasa yang rendah. bahasa Verilog digunakan untuk mereka bentuk dan membina modul pemproses dalam projek ini. Terdapat dua jenis alat simulasi iaitu Sinopsis dan Vivado yang digunakan untuk mensimulasikan reka bentuk. Projek ini akan memberi tumpuan kepada mereka bentuk 16-bit Unit Perarakan Central mudah (CPU) dengan kapal Memory Statik capaian rawak (SRAM) ingatan. Pemproses direka dibangunkan ke dalam susun atur dengan teknologi 0.18μm proses Silterra. Pemproses maju berbanding DW8051 teras dengan analisis pada masa, penggunaan kuasa dan kawasan teras. Perbandingan Peripheral Interface Siri (SPI) dan Litar Inter-Bersepadu (I^2C) dilakukan dan dibangunkan untuk susun atur dengan teknologi proses yang sama. Analisis pemproses adalah berdasarkan kepada masa, kuasa dan bidang yang dijana daripada penyelakuan. Pemproses dibangunkan harus berkesan lagi mudah yang memenuhi ciri yang diperlukan dalam sistem terbenam yang moden tetapi tanpa terlalu banyak kerumitan yang tidak perlu.

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LIST OF ABBREVIATIONS

MIPS	Microprocessor without Interlocked Pipeline Stages
RISC	Reduced Instruction Set Computing
CISC	Complex Instruction Set Computing
IC	Integrated Circuit
HDL	Hardware Description Language
VHDL	VHSIC Hardware Description Language
CPU	Central Processing Unit
SRAM	Static Random Access Memory
SPI	Serial Peripheral Interface
I^2C	Inter-Integrated Circuit
RAM	Random Access Memory
ROM	Read Only Memory
VCS	Verilog Compiler Simulation
DC	Design Compiler
ICC	Integrated Circuit Compiler
DVE	Discovery Visual Environment
SDA	Serial Data
SCL	Serial Clock
SS	Slave Select
MOSI	Master Out Slave In
MISO	Master In Slave Out
CLK	Clock

CHAPTER I

INTRODUCTION

In this chapter, we are explaining about the details of the project which is design and development of a low power compact integrated processor of an embedded system. Besides that, we also explained about objectives, problem statement, scope of project and chapter organization.

1.1 Project Background

Microprocessor without Interlocked Pipeline Stages (MIPS) is a popular implementation of a Reduced Instruction Set Computer (RISC). MIPS architectures are typically 32-bit, but 64-bit versions have been developed in more recent years. An embedded processor consumed with low power and low cost are the demands nowadays. This project is to design and develop an integrated processor of an embedded system with low power consumption.

The growth of processor with its complexity are concerned to the design with hundreds or thousands of logic gates. The large memories with high speed interfaces which give a higher performance to the processor is the reason that processor become more complex. The designers are using VHLD as design methodology to develop high level hardware system[1].

Integrated circuit (IC) design can be divided into 3 phases from the early 70s, which are polygon pushing, schematic capture and Hardware Description Language (HDL).

Polygon Pushing is the earliest phase of IC design. Usually not many design tools are available for this technique. The designers draw the design using polygons in layout. The disadvantages for this technique is highly tedious and error prone. It also limited amount of transistors up to only a few thousand[2].

Schematic Capture is the second phase of IC design method in 80s. This technique utilizes schematic editors to capture schematics drawn using gates and transistors. It can fit up to several hundred thousand transistors. This method allowed more complex and complicated circuits to be designed[3]. This also allowed more functionality to be put together. This method is still used today at 20s.

Starting 90s, the speed growth of electronics all over the world. Time to market for IC design became more essential[4]. Every design house was trying to fit multiple functionality onto a single IC chip with max millions of transistors. Also, IC design time frame as shortest as possible. This lead to design with HDL (Verilog/VHDL).

HDL is used to describe the logic functionality of a circuit. It can also describe the behavioral aspect of a circuit function. This method is used to show the netlist of a circuit. There are few types of HDL such as Verilog, VHDL, C/C++ and Superlog which is still under research[5].

This project will focus on designing a simple 16-bit Central Procession Unit (CPU) with onboard Static Random Access Memory (SRAM) memory. The developed processor should be effective yet simple that fulfills the features required in a modern embedded system but without too much unnecessary complexity.

1.2 Problem Statements

In previous research, the instruction set of a simple 16-bit CPU with onboard SRAM memory is loosely based on the MIPS architecture with some significant simplifications. The large instruction size is mostly to accommodate large register files and large memory spaces. Therefore, a simple 16-bit CPU with onboard SRAM memory will be designed and developed using Verilog language. Low power consumption will be the focus of the design. CPU usually consumed more power because of their higher speed and complexity. With lower power consumption, processor will dissipate less heat energy from the action of the switching devices contained in the CPU. This will particular important for battery operated devices.

1.3 Objectives

There are few of objectives that should be focused in this project in order to achieve the design of project:

- To design and develop a low power compact integrated processor of an embedded system by using Verilog language.
- To verify the functionality of the developed processor.
- To develop the processor into a layout.

1.4 Scope of Project

This scope of the project is to design and develop a low power integrated processor based on the architecture of MIPS processor and using timing constraint method to identify the best frequency for the overall performance of the processor. The modules of processors are constructed in Verilog Language and synthesis using Synopsis tools. The

designed processor is developed into a layout with 0.18μm Silterra process technology. However, the designed processor is in 16-bit instead of 8-bit due to the limitations of the designed processor.

1.5 Chapter Organization

This thesis comprises of seven chapters.

Generally, chapter one is more to introduction of project. In this section, we are explaining about project background, objectives, problem statements, scopes of project and chapter organization.

Chapter 2 is describing about literature review of project. In part of that, we explained about the topologies of different processor from the journals or articles that are related to the project. Besides that, comparison and differences of every topology have been stated in this chapter.

Chapter 3 is the overall of methodology of project. We explained about project schedule such as workflow and method that used to complete this project. We are using 2 platforms which are Synopsis and Vivado to analyze our designs.

Chapter 4 ,5, 6 and 7 are the results and discussions of the project. We explained about the obtained results based on the timing, area and power that generated from the simulations.

In chapter 4, we analyzed on the designed 16-bit and 32-bit MIPS processor and the power optimization of the developed processor. The discussion will explain overall problem that occur during implementation of this project from beginning until ends.

In chapter 5, we analyzed on the DW8051 core with different frequencies. The modules of DW8051 core is simulated in coreConsultant and go through synthesization in Synopsys tools.

In chapter 6, we compared the designed 16-bit MIPS processor with DW8051 core under same frequency with their corresponding timing, area and power consumption. All the analysis is graphically present and tabulated in this chapter.

In chapter 7, we analyzed on the peripheral interface which are SPI and I^2C. Both are encoded in the Verilog and running in the Synopsis in order to get the data and results. The operation of SPI and I^2C are explained in the simulation.

In Chapter 8, we concluded the overall achievements of the project. Then, we recommended some future works for further research to enhance the quality and performance of the processor.