COMPARISON OF PERFORMANCE OF VARIOUS OP-AMP TOPOLOGIES USING CMOS 0.13µm TECHNOLOGY

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A special

feeling of gratitude to my loving parents, Ummi and abi whose have supported me and give words of encouragement throughout the process.

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ABSTRACT

Op-amp is a device that is commonly used in an analog circuit that was designed to perform several of functions. Typically, as the CMOS technology becomes more advance, various of op-amp topologies are invented to suit the technology. However, most studies on past technologies have found out that the parameters are still not sufficient enough in order to meet the performance goal of CMOS 0.13µm technology. In order to select the right op-amp for CMOS 0.13µm technology, various performance specifications need to be taken into consideration. Therefore, in this project four types of op-amp topologies (Folded-Cascode, Telescopic, and Multi-stage) are characterized based on gain, output voltage and power consumption using CMOS 0.13µm technology. The development of this project consists of designing each topology by using Cadence Virtuoso tool. These op-amp topologies are compared to select the one that can provide the best performance in term of high gain, and low power.

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ABSTRAK

Op-amp adalah alat yang biasa digunakan dalam litar analog yang direka untuk melaksanakan beberapa fungsi. Biasanya, apabila teknologi CMOS menjadi lebih maju, pelbagai topologi op-amp dicipta untuk disesuaikan dengan teknologi. Walau bagaimanapun, kebanyakan kajian mengenai teknologi masa lalu telah mendapati bahawa parameter masih tidak mencukupi untuk memenuhi matlamat prestasi teknologi 0.13µm CMOS. Untuk memilih op-amp yang sesuai untuk teknologi 0.13µm CMOS, pelbagai spesifikasi prestasi perlu diambil kira. Oleh itu, projek ini akan memberi tumpuan kepada tiga jenis topologi op-amp (Folded-Cascode, Telesopic, dan op-amp Two stage) untuk memeriksa prestasi mereka dengan menggunakan CMOS teknologi 0.13µm. Proses perlaksanaan projek ini terdiri daripada mereka bentuk topologi dengan menggunakan alat CADENCE Virtuoso. Topologi op-amp dibandingkan untuk mengetahui salah satu yang boleh memberikan prestasi yang terbaik dari segi keuntungan yang tinggi, dan tenaga yang rendah.

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CHAPTER I

INTRODUCTION

In this project, the implementation of circuit configurations for each op-amp topologies will use Cadence Virtuoso Platform. It is a software tools that allows us to design full custom integrated circuits which includes circuit simulation, custom layout, and physical verification.

Cadence Design System is an advanced electronic design automation (EDA) tools that support the designs of any technology which is from micrometer up to nanometre era and helps in addressing all aspects of electronic design. It enables any design from the design of individual transistor up to the development of software before any hardware is built.

The purpose of this project is to compare some of the performance parameters of different op-amp circuit configurations using CMOS 0.13µm technology. Each op-amp topology will be having a supply input of 1.2V. The op-amp topology that can gives the best performance in term of maximum gain and high output voltage with low power can be used in wide applications for example in

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designing analog-to-digital (A/D) and digital-to-analog (D/A) converters, high-order filters, signal amplifiers , video application and many more.

At the end of this project, a topology that can achieves the parameter specification to meet the high performance goal with low power using CMOS 0.13µm technology will be identified.

1.1 Objective

The main objective of this research study is to compare the performance of various Op-amp Topologies (i.e. Folded-Cascode,Telescopic, and Multi-stage) using CMOS 0.13µm Technology. The following sub objectives have to be met:

- To design a Folded-Cascode, Telescopic, and Multi-stage using CMOS 0.13µm Technology.
- To simulate each op-amp topologies using CADENCE software.
- To characterize the op-amp topologies based on gain, output voltage and power consumption.
- To analyze the performance of each op-amp topologies in term of gain and power.

The final objective is to select a topology that have the highest gain, and output voltage with low power using CMOS 0.13µm Technology.

1.2 Problem Statement

This project was carried out due to the demands for high performance operational amplifier using CMOS technologies which increased dramatically in recent years, especially for digital–analog interface circuits. With the downsizing of transistor length of CMOS over years, various op-amp topologies have been designed using past CMOS technology to obtain high gain, with low power at output. Unfortunately, many studies on past technologies have found out that the performance parameters are still not sufficient enough in order to meet the

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performance goal. Also, it is less clear which circuit topologies could gives the maximum performance in term of high gain when using CMOS 0.13µm technology.

1.3 Scope of Work

The research will focus on the investigation of folded-cascode, telescopic, and two-stage op-amp topologies using CMOS 0.13µm technology. The standard design platform of Cadence software which is Cadence Virtuoso Platform will be used for this project. The software is unlocked by using an invoke command. These op-amp topologies will be simulated to investigate effects on output voltage, power and gain. The process is until the schematic layout.

1.4 Project Significant

- The significance of this research is to choose an op-amp topology that can give the highest gain using 0.13µm technology
- The op-amp topology that have high performance with low power can be used to power up a wide range of products, such as Internet services, speech recognition, fingerprint authentication, and wireless video
- An optimum op-amp topology can be used to design an integrated CMOS Analog-to-Digital converter for communication and video applications.
- The performance specifications describe the amplifier, making it easier for the designer to access it impact on their circuit.

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1.5 Project Methodology

All the articles and journals were selected using on-line search databases including IEEE xplore, and Google scholar. The existing op-amp topologies were used in this project which includes Folded-Cascode,Telescopic, and Multi-stage. This type of op-amp topologies were selected as they are the most common modern op-amp used in IC. These op-amp topologies are implemented using Cadence software (Cadence Virtuoso Platform). Ability to design circuits using Cadence software is through the process of following step-by-step description from "Cadence Design Systems Composer-Schematic" module. YouTube also plays a role in understanding the process to design these op-amp topologies.

1.6 Project Structure

This research will consist of five chapters. Chapter 1 will introduces the background, objectives, problem statement, scope of work, and significance of the study. Chapter 2 consists of literature review that relates on CMOS op-amps and op-amp topologies. Information and facts are reviewed and compared from various references such as books, journals, articles with necessary figures. Chapter 3 consists of methodology of the research study. Chapter 4 consists of simulation results that are observed and found from the designed CMOS operational amplifier. The results are then discussed by the representation of graphs and related figures.

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CHAPTER 2

LITERATURE REVIEWS

In this chapter, reviews of the previous researches project that are related with this project will be discussed. The information will become an additional source for the project in becoming more successful. To have a brief understanding of the researches related to the project, a few literature reviews had been done. This chapter will describe the related literature reviews.

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2.1 Overview

By referring to Figure 2.1, there are several types of IC process technologies. For example, Bipolar, CMOS and BiFET. Each has different advantages when applied to single supply amplifier. Bipolar amplifier which is found on 1984 consists of NPN and PNP transistor at the input terminals which allow for higher open loop gain. Besides, it gives very low noise and low offset voltage between the input terminals as well as more faster compared to FET transistor. Despites having many advantages, it consist low packing density and quiet expensive in mass production. Bipolar is suitable to be used for high-performance operation[1].

While for BiFET amplifier, it is a combination of Bipolar and FET (Field Effect Transistor). For this op-amp, the designed is having FET at the input terminals while Bipolar for the rest of the circuit. BiFET owns the advantages of Bipolar and FET transistor. The combination gives higher slew rates compared to CMOS and Bipolar. However, it is not suitable for single supply devices and produce low open loop gain. When compared between BiFET and Bipolar, both shares similarity by having wider bandwidth and high output drive capability[2].

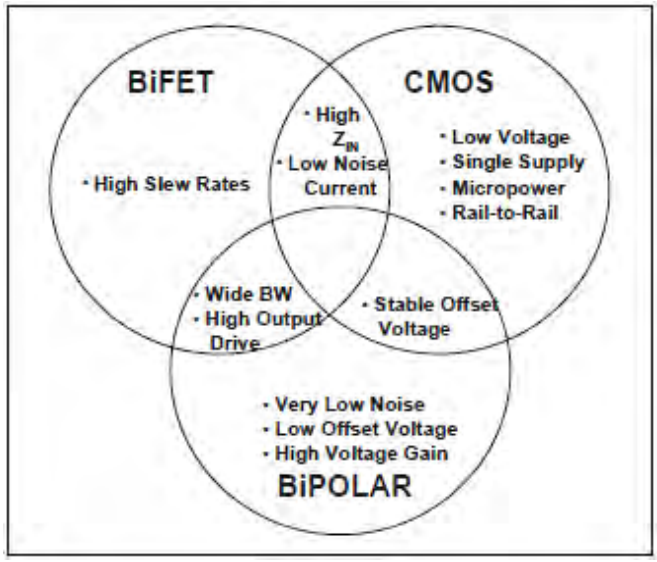

Figure 2.1:Comparison of different IC processors

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2.2 Operational Amplifier

Operational amplifier(op-amp) can be defined as a basic building block which consists two signal inputs and power supply with one output terminal[2]. The basic op-amp is given in Figure 2.2. Op-amps are used throughout the systems to perform several of function. For example, op-amps can be used to implement filters, buffers, to excite current and voltage, helps achieve the converter high performance, used to accomplish precision signal processing and many more[2]. In the past, op-amps were designed to satisfy the requirements of different applications, but now op-amp are build to satisfy specific applications by improving the important aspects of the performance[3]. Theoretically, an ideal op-amp have an infinite gain, zero power consumption, infinite input impedance, infinite bandwidth and zero output impedance. The quality of op-amp is determined by how close we come to these ideals[4].

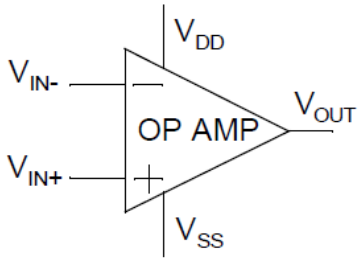

Figure 2.2 : Op-amp symbol

2.3 CMOS op-amp

Since most of the amplifier does not have a large enough gain, CMOS op-amp is used instead in order to meet the requirement of an op-amp which is to have an open loop gain that is sufficiently large to implement the negative feedback concept. CMOS op-amp is always known for its low power, single supply op-amp. The first CMOS circuit is introduced by a group led by Albert Medwin in 1968.

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