UNIVERSAL TIME AND CALENDAR SYSTEM IN FIELD PROGRAMMABLE GATE ARRAY (FPGA)

FATIN SHAJ BINTI AHMAD JAMAL

This Report is Submitted in Partial Fulfillment of Requirements for the Bachelor Degree of Electronic Engineering (Computer Engineering)

Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer

Universiti Teknikal Malaysia Melaka

June 2014

UNIVERSTI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN
PROJEK SARJANA MUDA II

Tajuk Projek : Universal Time and Calendar System in FPGA.

Sesi Pengajian : | | | | | |

Saya FATIN SHAJ BINTI AHMAD JAMAL.
(HURUF BESAR)
Mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hak milik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (√) :

☐	**SULIT***	*(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐	**TERHAD****	**(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)
☐	**TIDAK TERHAD**	

Disahkan oleh:

_____ (TANDATANGAN PENULIS)

_____ (COP DAN TANDATANGAN PENYELIA)

Tarikh: ……..

Tarikh: ……..

"Saya akui laporan ini adalah hasil kerja saya sendiri kecuali ringkasan dan petikan yang tiap-tiap satunya telah saya jelaskan sumbernya."

Tandatangan : …….

NamaPenulis : …….

Tarikh : …….

"Saya/kami akui bahawa saya telah membaca karya ini pada pandangan saya/kami karya ini adalah memadai dari skop dan kualiti untuk tujuan penganugerahan Ijazah Sarjana Muda Kejuruteraan Elektronik (Kejuruteraan Komputer)."

Tandatangan : …….

NamaPenyelia : …….

Tarikh : …….

For my beloved dad and mom

ACKNOWLEDGMENT

I take this opportunity to express my profound gratitude and deep regards to my supervisor Dr. Yosza bin Dasril for his exemplary guidance, monitoring and constant encouragement throughout the completion of this thesis. The blessing, help and guidance given by him time to time shall carry me a long way in the journey of life on which I am about to embark. I also take this opportunity to express a deep sense of gratitude to Mr. Sani Irwan bin Salim, for his cordial support, valuable information and guidance, which helped me in completing this final year project through various stages. Lastly, I thank almighty, my lovely dad and mom, brother and friends for their constant encouragement without which this project would not be possible.

ABSTRAK

Sistem masa dan calendar kebiasaannya dikawal oleh banyak cip untuk mengawal denyut frekuensi masa bagi memperolehi satu pusingan lengkap untuk saat, minit, jam, hari, haribulan, bulan, dan tahun. Dalam FPGA, system masa dan calendar adalah sebahagian daripada sistem yang besar yang telah dilaksanakan dalam kehidupan seharian kita contohnya seperti jam penggera, system pengkalan data, system pendaftaran, system kad perakam waktu dan banyak lagi. Walaubagaimanapun, kebanyakan system masa dan calendar digunakan dalam komponen diskret yang selalunya bersaiz besar dan mahal. Ini adalah kerana perbezaan penghubung yang digunakan dalam system terbenam banyak menggunakan litar bersepadu hanya untuk sistem yang mudah. Oleh sebab itu, matlamat utama untuk projek ini adalah untuk mereka Sistem Masa dan Kalendar menggunakan Field Programmable Gate Array melalui perkakasan penerangan bahasa Verilog tanpa menggunakan komponen diskret. Projek ini memaparkan maksimum masa 7 hari seminggu bersama bulan dan tahun. Masa akan dipaparkan daripada kosong ke maksimum tahun = 9999, hari = 6, jam = 23, minit = 59, saat = 59. Pada masa yang sama, ia juga boleh memaparkan daripada satu hingga maksimum bulan = 12, dan haribulan = 31. Sistem ini bergerak menggunakan jam kristal quartz rasmi 10 MHz. Papan latihan LP-2900 digunakan bersama cip Xilinx FPGA untuk menguji program tersebut. Program FPGA ini menggunakan Verilog.

ABSTRACT

A clock and calendar system is normally controlled by many chips in order to regulate the frequency of the clock pulse to obtain cycles for seconds, minutes, hours, days, days of the month, months and years. In FPGA, time and calendar system is a part of a bigger system that is implemented in our daily life such as in alarm clock, database system, registration system, punch card system and many more. However, most of the time and calendar system were used in a discrete component that are bigger in size and expensive. This is because of the different interface use in the embedded system that used many ICs for just a simple system. Therefore, the main goal of this project is to design a Time and Calendar System in Field-Programmable Gate Array through hardware description language (Verilog) without using discrete components. This project displays a maximum of 7 days weekly timer with months and year. The time will read from zero to a maximum year = 9999, day = 6, hour = 23, minutes = 59, seconds = 59. In addition, it is also can read from one to a maximum month = 12 and day of the month = 31. The system is run by a standard quartz crystal clock 10MHz. A LP-2900 trainer board is used to test the prototype with a Xilinx FPGA chip. The FPGA is programmed using Verilog.

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES

LIST OF SYMBOL / ABBREVIATION / TERM

FPGA	-	Field Programmable Gate Array.
IC	-	Integrated Circuit.
PIC	-	Programmable Interface Controller.
HDL	-	Hardware Description Language.
VHDL	-	Very High Speed Hardware Description Language.
LED	-	Light Emitting Diode.
BCD	-	Binary-coded-decimal.
RAM	-	Random Access Memory.
SDA & SCL	-	Serial data signal in I2C bus
RTC	-	Real-time Clock
PC	-	Personal Computer
SCM	-	Software Configuration Management software
Iobd	-	Input output block diagram
Am	-	Ante Meridiem (before noon)
Pm	-	Post Meridiem (after noon)
Cntr	-	Counter
LUT	-	Look-up Table
LSB	-	Least significant bit

CHAPTER I

INTRODUCTION

This chapter will discuss on the introduction of the project Universal Time and Calendar System using Field Programmable Gate Array (FPGA). This chapter includes the project introduction, objectives, scope of work, problem statement and methodology. The project introduction is the summary of all the important parts inside this chapter. There will be three objectives listed for this project. The problem statement stated on the problem occurred and why this project is proposed. The scope of work focused on what this project will likely involved and done until this project is successful. Last but not least, the methodology parts states the important point inside the methodology chapter.

1.1 PROJECT INTRODUCTION

In FPGA, time and calendar system is a part of a bigger system that is implemented in our daily life such as in alarm clock, database system, registration system, punch card system and many more. This time and calendar system also known as the real time and calendar system that needs to keep the accurate time and day and has benefits such as low power consumption and more accurate than other methods. Besides, time and calendar system is often used in the form of an integrated circuit such as the PIC microcontroller. However, most of the time and calendar system were used in a discrete component that are bigger in size and expensive. This is because of the different interface use in the embedded system that used many ICs for just a simple system. Using FPGA, this problem can be solved because it does not involve any discrete component.

FPGA is also an integrated circuit that was designed for a designer to configure their design after device manufacturing. The FPGA generally used with the hardware description language to specify the configuration. Along with the Verilog Hardware Description Language (VHDL), it is the most popular and standard hardware that were used among the designers [1]. This is because Verilog offers benefits of digital hardware design with a general-purpose hardware description language same as the C programming. Thus, it is making it user friendly and easy to understand.

Therefore, in this project a Time and Calendar System in Field-Programmable Gate Array is proposed through hardware description language (Verilog) without using discrete components. The scope of this project is to display a maximum of 7 days weekly timer with months and year. The time will read from zero to a maximum year = 9999, day = 6, hour = 23, minutes = 59, seconds = 59. In addition, it is also can read from one to a maximum month = 12 and day of the month = 31. The system will run by a standard quartz crystal clock 10MHz. A LP-2900 trainer board is used to test the prototype with a Xilinx FPGA chip. The FPGA is programmed using Verilog. A real time clock and calendar system that can display through 7-segment LEDs is expected to be produced.

1.2 PROJECT OBJECTIVES

The aim of this project is to produce a universal time and calendar system using Field Programmable Gate Array (FPGA).

The objectives of this project are:

i. To design a Time and Calendar System in Field-Programmable Gate Array.
ii. To simulate and synthesize the program using Xilinx XST.
iii. To display a Time and Calendar System through 7-segment LEDs on the LP-2900 trainerboard.

1.3 PROBLEM STATEMENT

A basic time and calendar system is usually designed by constructing a lot of gates and counters to obtain and control the functions of time and calendar. An existing basic time and calendar with a basic function such as showing time, day, month and year may need circuit constructions which consist of a few gates, BCD-to-seven-segment decoder, multiplexer, counter or some other specific ICs.These complicated structures were added more with lots of wire and ICs chip and could not be reduced due to the complex circuit.

Most of the time and calendar system were used in a discrete component that are bigger in size and therefore expensive in the matter of construction, maintenance and manufacturing. This is because of the different interface use in the embedded system by using many ICs for just a simple system. However, using FPGA can solved all of these problems because it only used the hardware description language, Verilog. With the FPGA, designer will only have to debug the code written in hardware description language if any errors occur before producing it massively. Besides, it will save the cost, size and space because the FPGA chip is small.

1.4 SCOPE OF WORK

The scope of this project is to display a maximum of 7 days weekly timer with months and year. The time will read from zero to a maximum year = 9999, day = 6, hour = 23, minutes = 59, seconds = 59. In addition, it is also can read from one to a maximum month = 12 and day of the month = 31. The system will run by a standard quartz crystal clock 10MHz. A LP-2900 trainer board is used to test the prototype with a Xilinx FPGA chip. The FPGA is programmed using Verilog.

1.5 METHODOLOGY

The flow chart of overall project and flow chart of the Verilog program in designing the universal time and calendar system with explanation are covered in Chapter 3, Methodology.

CHAPTER II

LITERATURE REVIEW

This chapterwill discuss about the research and reviews on works of other researchers that have done to this related project. This chapter contained six subtopic which include the review on Cadence Design of clock/calendar using 240*8 bit RAM using Verilog HDL. This paper is from K.L University, Guntur by K.R.N. Karthik et.al. Second subtopic is about FPGA Based Digital Electronic Education Clock-Calendar Design. This paper is from Turgut Ozal University, Turkey by Vedat Kiray. Third subtopic is about Design of Calendar Clock Based on DS12C887 Chip. This paper is from Nanjing University of Information Science and Technology by Xiao Chen. Forth subtopic is about Design and Construction of a Four-hourly Digital Alarm Clock. This paper is from Pelagia research Library by Ochala, I, Momoh, O. Y, and Gbaorun, F. The fifth subtopic is about Real Time Calendar Applications in Actel Fusion Devices. This paper is from the Actel Corporation. At the end of this chapter, it is briefly explain on the difference between the proposed project and other work that has been discussed in this chapter.

2.1 Cadence Design of clock/calendar using 240*8 bit RAM using Verilog HDL.

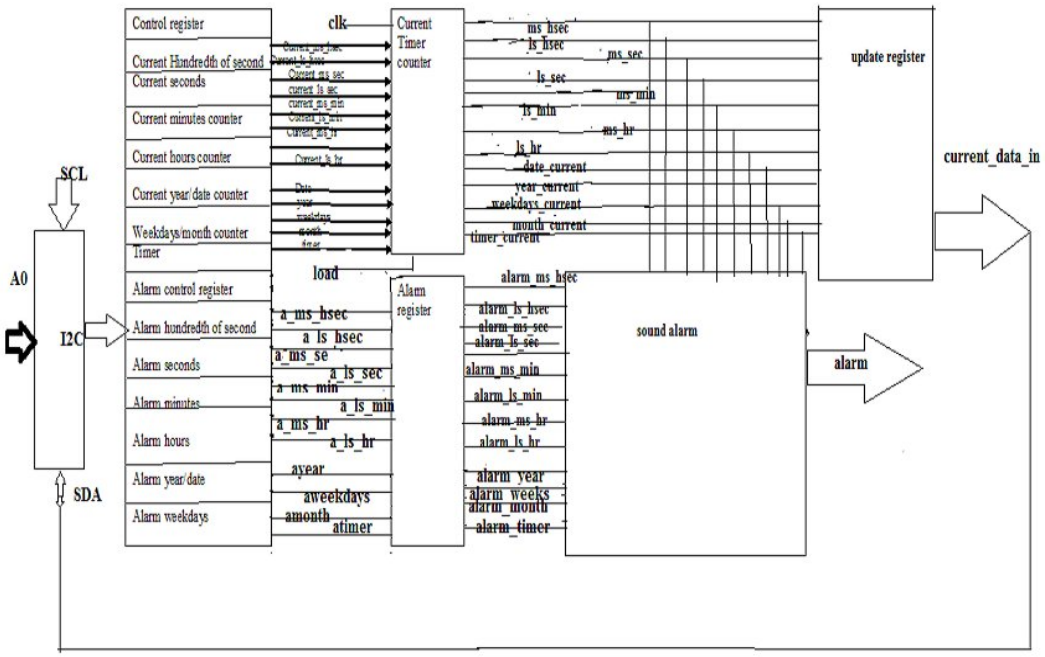

Figure 2.1: Block Diagram of clock/calendar.

In this paper, it is about Cadence design clock calendar using 2048 bit RAM using Verilog HDL. This design is organized as 256 words by 8 bits with address and data are transferred serially via the two-line bidirectional I2C-bus [2]. This module is using the Verilog language with Xilinx and Cadence 90nm in Linux environment.

From the above block diagram, it consists of six modules which are counter, alarm register, sound alarm, update register, RAM and I2C. It is also included the SDA and SCL line which consist of nine clock pulse of 8 bit data. This module has a standard clock of 100 kHz.

As a conclusion, this paper is about designing a clock calendar using Cadence with Verilog HDL. It can be used in various digital circuitry at the same time reduces the design time of the digital circuits. Practically, it designs its layout using Cadence 90nm technology and implements it in Verilog using Xilinx.

2.2 FPGA Based Digital Electronic Education, Clock Calendar Design.

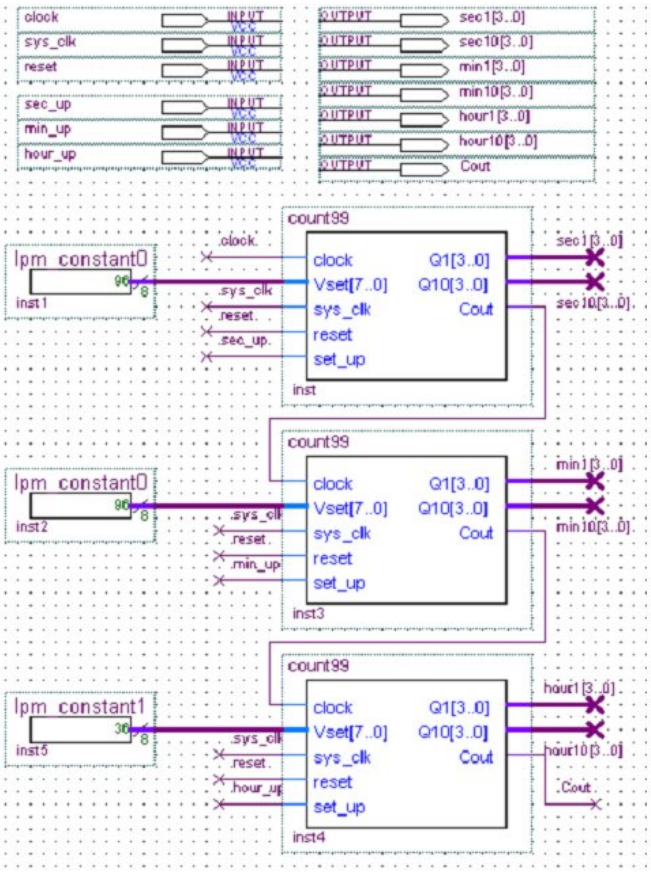

Figure 2.2: The full counting circuit block.

This paper is a case study based on the Project Based Learning for the Electronics and Computer Engineering students to design a circuit and implemented it in the FPGA. It involved with building a block from a circuit and putting the block together to get new blocks. The designed is divided into three sub block as counting, setting and display.

In the counting block, it taught the students to design a comparator, convert the circuit into counter and obtain the block to have a counter for seconds, minutes, hour, day, month and year. It then used the simulation results to evaluate the performance.The difference between the clock and calendar is from the signal that was sent to calendar block as input pulse [3].

In the setting block, this is where the students will have to add something for the design according to the other blocks. This section is to help the students understand the function of the block better. It shows steps to set for the block such as using the AND gate, multiplexer, counter and decoder to be add in their design. The last task given to the student is to solve the up counting problem where it causes difficulty in usage and waste time.

The last sub block is the display block. This is the most difficult part for the student as to display the results in a flash with intervals of a second for indicating the selected unit. It used many of multiplexer in the designed thus make it more complex. This part is to analyze the results on the board and understand if the clock calendar is at normal working condition.

As for conclusion of this paper, it contains the information to study the graphic design of clock calendar system. It teaches from the basic of what circuits are involved and steps in designing a clock calendar system.This graphic design can be redesigned again using HDL codes.

2.3 Design of Calendar Clock Based on DS12C887 Chip.

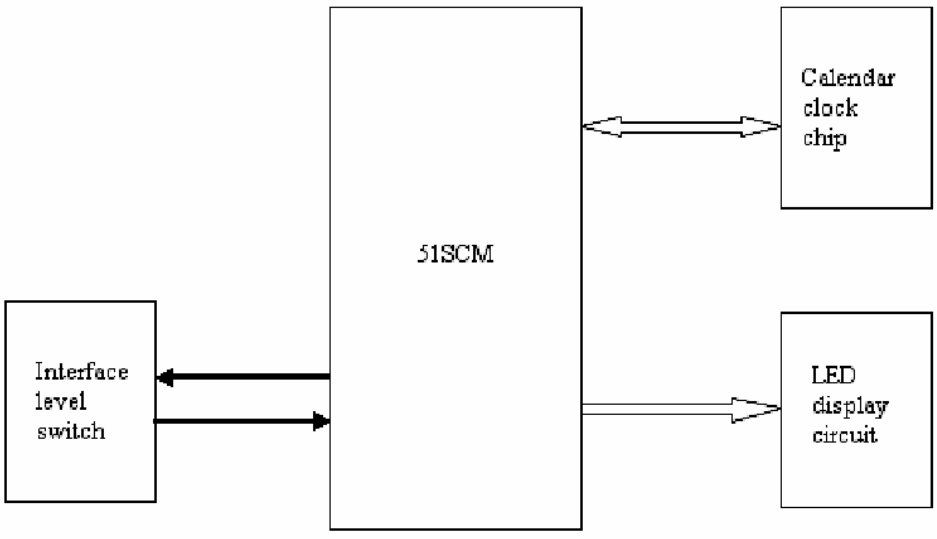

Figure 2.3: The structure of system hardware.