# IMPLEMENTATION OF RISC ARCHITECTURE IN SIMULINK AND FPGA

**MOHD RASHIDI BIN MD PUZI**

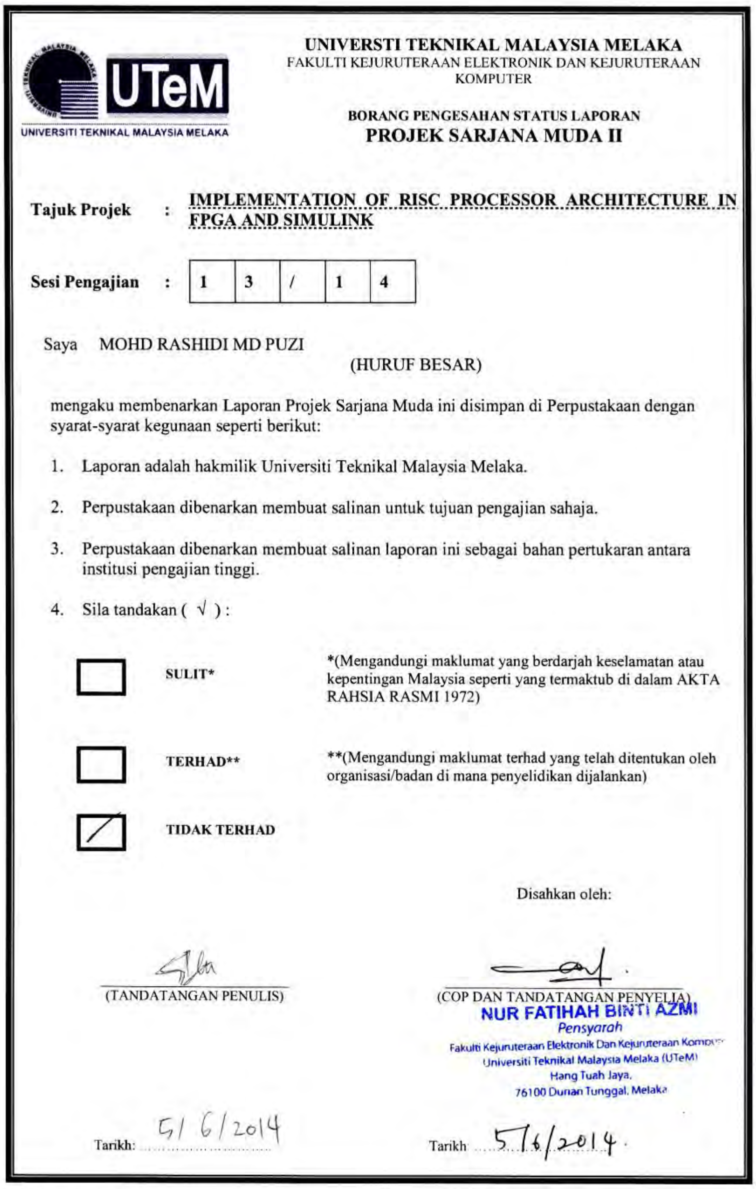
**This Report Is Submitted In Partial Fulfilment of Requirements For**

**The Bachelor Degree of Electronic Engineering (Computer Engineering)**

**Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer**

**Universiti Teknikal Malaysia Melaka**

**JUNE 2014**



**UNIVERSTI TEKNIKAL MALAYSIA MELAKA**
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

**BORANG PENGESAHAN STATUS LAPORAN**
**PROJEK SARJANA MUDA II**

**Tajuk Projek** : **IMPLEMENTATION OF RISC PROCESSOR ARCHITECTURE IN FPGA AND SIMULINK**

**Sesi Pengajian** : | 1 | 3 | / | 1 | 4 |

Saya MOHD RASHIDI MD PUZI
(HURUF BESAR)

mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan ( √ ) :

□ **SULIT*** *(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)

□ **TERHAD**** **(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)

☑ **TIDAK TERHAD**

Disahkan oleh:

(TANDATANGAN PENULIS)

(COP DAN TANDATANGAN PENYELIA)

NUR FATIHAH BINTI AZMI
*Pensyarah*
Fakulti Kejuruteraan Elektronik Dan Kejuruteraan Komputer
Universiti Teknikal Malaysia Melaka (UTeM)
Hang Tuah Jaya,
76100 Durian Tunggal, Melaka

Tarikh: 5/ 6/ 2014

Tarikh: 5/6/2014.

*CATATAN : Jika laporan ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/organisasi berkenaan dengan menyatakan sekali tempoh laporan ini perlu dikelaskan sebagai SULIT atau TERHAD.

"I hereby declare that this report is result of my own effort except for quotes as cited in the references"

Tandatangan : ..........................................

Nama Penulis : MOHD RASHIDI MD PUZI

Tarikh : $6^{TH}$ JUNE 2014

"I hereby declare that I have read this report and in my opinion this report is sufficient in terms of the scope and quality for the award of Bachelor of Electronic Engineering (Computer) with honours"

Tandatangan : ..............................................................

Nama Penyelia : PN NUR FATIHAH BT AZMI

Tarikh : 6TH JUNE 2014

***Specially dedicated to***

***My beloved family,***

***My supervisor,***

***My friends who have encouraged, guided and***

***Inspire me throughout my journey of education.***

# ACKNOWLEDGEMENT

First of all, I would like to take this opportunity to express my deepest gratitude to my project supervisor, Madam Nur Fatihah bt Azmi for her guidance, encouragement and endurance during the whole course of this project. It is indeed my pleasure for her support, invaluable advices and enthusiastic towards my project. My special gratitude is to my beloved family, especially my parents Ramlah bt Awang and Md Puzi bin Daud for their fullest support throughout the years study in University of Technical Malaysia Malacca (UTeM). It is because of them, I am the person who I am today, for all their moral support all these while so that I will be to complete my project successfully. My appreciation is also to my friends especially to my course mates, for their technical advice. To all the people that are assisting me directly and indirectly in this project, once again I would like to say thank you. Thank you

# ABSTRACT

This project is about the implementation of RISC processor architecture in Simulink and FPGA (Field Programmable Gate Array). RISC processor has been used in many computer-based applications nowadays comparing to CISC. This project aims to design RISC processor architecture in Simulink environment where it used a model-based design. The RISC architecture block diagram and designed in the Simulink, and then the architecture can be developed by gathering the entire required source for the MATLAB function be create the architecture. Most of the block used is the MATLAB function block source code. In the source code, the input and output for the entire module will be defined. To produce a working architecture, all the parameters for the RISC processor architecture can be set in the given parameter setting. Therefore, the error on the architecture can be minimized. By integrating the entire module, the architecture test program to test the functionality of the architecture. The test program used is the bubble sorting, where there will be an array of data to be sorted. The output can be display in the scope provided in the architecture. The HDL code can be generated using the HDL Coder provided in the simulink setting. Using the HDL Coder, the Verilog code can be provided for verification in the FPGA. This project focuses on 8-bit RISC processor and implemented using MATLAB 2013a/Simulink. As for the testing purpose, it will be implemented in Virtex 6 FPGA board.

## ABSTRAK

Projek ini adalah mengenai perlaksanaan senibina pemproses RISC di dalam *Simulink* dan FPGA. Pemproses RISC telah digunakan di dalam kebanyakan sistem yang menggunakan aplikasi computer berbanding CISC. Tujuan projek ini adalah untuk merekabenuk senibina pemproses RISC di dalam Simulink di mana ianya menggunakan rekabentuk berasaskan model. Di dalam Simulink, senibina RISC dibentuk dengan berpandukan blok diagram yang berkenaan. Selepas itu, senibina RISC dapat dibangunkan dengan menggabungkan kesemua kod yang diperlukan oleh fungsi MATLAB. Kebanyakan blok yang diguanakan adalah sumber-kod-blok-fungsi MATLAB. Di dalam sumber kod, segala masukan dan keluaran untuk keseluruhan modul senibina ditakrifkan. Untuk menghasilkan senibina yang berjaya, segala parameter untuk pemproses RISC ditetapakan di dalam applikasi Simulink. Dengan itu, segala ralat di dalam senibina dapat dikurangkan kepada tahap minimum. Dengan menggabungkan kesesmua modul yang berkaitan, senibina pemproses RISC dapat diuji dengan menggunakan program ujian yang telah dibentuk. Tujuan program ujian ini adalah untuk mengenal pasti fungsi di dalam pemproses RISC dalam keadaan yang baik. Program ujian yang digunakan adalah algoritma isih yang asas, iaitu isih gelembung. Algoritma isih gelembung digunakan untuk megisih data yang dimasukkan ke dalam masukan pemprose RISC dalam bentuk menaik, iaitu dari nilai yang sedikit ke nilai yang banyak. Keluaran data dipamerkan di dalam skop yang telah disambungkan. Seteleah itu, kod HDL dapat dikeluarkan dengan menggunakan Koder HDL yang terdapat di dalam tetapan Simulink. Dengan mengguanak koder tersebut, kod Verilog dapat dihasilkan untuk tujuan pengesahan di dalam FPGA. Projek ini difokuskan kepada pemproses RISC 8-

# TABLE OF CONTENTS

## LIST OF TABLES

## LIST OF FIGURES

## ABBREVIATIONS

| | | |
|---|---|---|
| RISC | - | Reduced Instruction Set Computer |
| CISC | - | Complex Instruction Set Computer |
| FPGA | - | Field Programmable Gate Array |
| DSP | - | Digital Signal Processing |
| VHDL | - | Verilog High Description Language |
| HDL | - | High Description Language |
| MIPS | - | Million instructions per second |

# CHAPTER I

# INTRODUCTION

## 1.1 Overview

Embedded system application had been used in much computer application. The main core for this application is its processor, whether RISC or CISC. Through many had used CISC for its wide range of use, RISC has its own advantages over the complexity of architecture construction.

## 1.2 Objectives

The objectives of this project are to design RISC processor architecture in Simulink environment and to generate RISC processor design code using FPGA platform

## 1.3 Problem statement

This project addresses the limitations for embedded system design using processors. Nowadays, a lot of embedded system are incorporating signal processing algorithm to make the system more suitable in real world applications. As a discrete component, processor possesses limited capabilities in executing complex algorithm such as DSP. Therefore, integrating process design with Simulink software would simplify the development phase of the embedded system.

## 1.4 Scope

This project will focus on 8-bit RISC processor architecture and it will be implemented using MATLAB 2013a Simulink. For testing purpose, the design will be implemented in Virtex 6 FPGA board.

# CHAPTER II

# LITERATURE REVIEW

This chapter presents the details about literature review of Implementation of RISC Processor Architecture in Simulink and FPGA. It consist reviews on related paper. There are 12 papers involved, but in this project, I will focus on 3 main papers, which are Implementation of RISC Processor in FPGA, FPGA Prototyping of a RISC Processor Core for Embedded Application and Design of FPGA Controlled Power Electronics and Devices Using MATLAB Simulink. The main paper for reference is the Implementation of RISC Processor in FPGA. All the details about the paper will be explained later on.

## 2.1 Implementation of RISC Processor in FPGA[1]

### 2.1.1 Introduction

A true 16-bit RISC processor has been designed using VHDL. Hierarchical approach has been used so that basic units can be modelled using behavioural programming.

RISC processor has been designed for specific application to function efficiently and can meet minimum requirements for application in hand. In such design, the main criteria that had been focused is the performance of the processor. The purpose of this project is to match the requirements for small application having such efficient performance of processor. Over the years, CISC processor had gained the most used processor in the marketplace. The reason behind this is the wide range of addressing modes and data types they can support while RISC processor operates on very few data types and does simple operations. RISC supports very few addressing modes and are mostly register based.

### 2.1.2 Problem statement

The problem stated in this paper is structural hazards, data hazards and control hazards. Data hazards are due to sharing of destination and source resources in succeeding instruction. Structural hazards are due to common program and data memory while control hazards are due to non-sequential execution of instruction.

### 2.1.3 Methodology

Data hazards can be handled by using method of forwarding. Structural hazards are handled by using the method of prefetching queue in processor and control hazards can be solved by using flushing.

### 2.1.4 Result

The design has been implemented in FPGA. FPGA is a device used for the verification purpose. Working as a raw IC, where user can implement its design and verify the correctness of design. By using this method, cheaper prototyping can be achieve plus with shorter time for market of hardware design.

## 2.2 FPGA Prototyping Of A RISC Processor Core For Embedded Applications[2]

### 2.2.1 Introduction

This paper presents the usage of MIPS RISC processor core as a starting point for hardware/software codesign space exploration. There are numbers of factors that contribute to the choosing of the architecture, such as the provision of a clean starting point for application specific extension and the architecture's popularity in the embedded control market. The lengthy software simulation of a designed model holds very important role in the deploying new architecture.

### 2.2.2 Problem statement

Software-based simulation has its own disadvantage as it not allow all aspects of a design's functionality to be exercised. Adapting an instruction set is a difficult task.

### 2.2.3 Methodology

Using the processor core as the basis for designing several application-specific processors, the evaluation of the instruction set architecture is the main issue. A common approach is to extend the instruction set by application-specific instructions. To optimized the processor performance, the number of instruction set is minimized only to necessary.

### 2.2.4 Result

Using the processor extensions generated by the processor core HDL description, the new functionality is added such as fuzzy processing, logic programming and vector and list processing.

## 2.3 Design Of FPGA-Controlled Power Electronics And Devices Using MATLAB Simulink[3]

### 2.3.1 Introduction

The design of modern power electronic circuits and system requires knowledge from multiple discipline areas including digital control, to develop innovative and custom-designed products and solutions in a short period of time. Manual coding is tedious, time consuming and error prone. On the other hand, code generation lets designer to make changes is the system level model, and produce an updated HDL implementation in minutes by generating the HDL code. In addition, MATLAB model-based design facilitates creation of FPGA based prototypes and automates HDL code verification by co-simulating it with Simulink and optimizes the models to meet speed-area-power objectives for FPGA.

### 2.3.2 Problem statement

The main problem is the manual coding that are tedious, time consuming and error prone.

### 2.3.3 Methodology

A. Code conversion: MATLAB Simulink to VHDL Code

The HDL describes electronics circuits in terms of the circuits operation, design and test to verify its operation by the means of simulation. The first step to code conversion is the new design ideas and algorithms are represented in terms of mathematical models and are tested in MATLAB/Simulink floating point data types. However, implementation of control algorithms in FGPA's and ASICs require fixed-point data type conversion to reduce hardware resources.

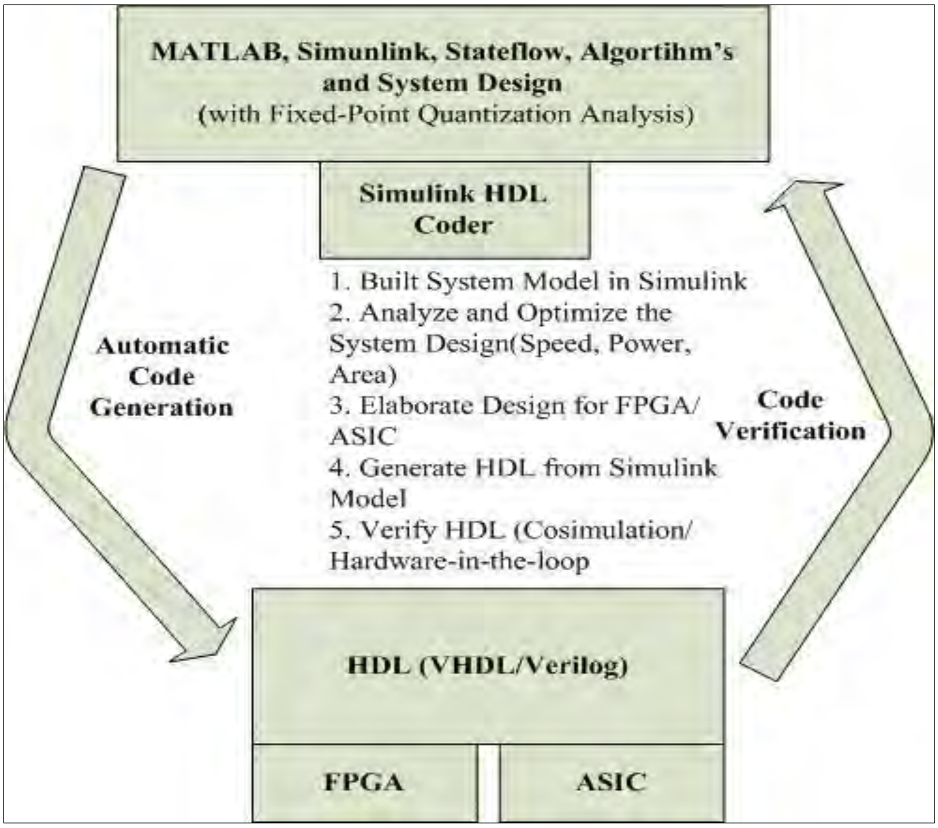

MATLAB, Simunlink, Stateflow, Algortihm's and System Design
(with Fixed-Point Quantization Analysis)
Simulink HDL Coder
1. Built System Model in Simulink
2. Analyze and Optimize the System Design(Speed, Power, Area)
3. Elaborate Design for FPGA/ ASIC
4. Generate HDL from Simulink Model
5. Verify HDL (Cosimulation/ Hardware-in-the-loop
Automatic Code Generation
Code Verification
HDL (VHDL/Verilog)
FPGA
ASIC

Figure 2.3.1 Method to generate HDL Code from MATLAB and Simulink, with code verification

### 2.3.4 Result

The method is to facilitate the development and implementation of FPGA-based digital controllers in power electronic converters and drives. The method is faster and provides a greater degree of confidence than traditional manual HDL coding.

# CHAPTER III

# METHODOLOGY

## 3.1 Introduction

This chapter will explain more detail about the project methodology that used in the project. This part will explain more detail on the project development, from beginning until it's completed. The steps will be explained in detailed manner.

## 3.2 8-bit RISC Processor Block

### 3.2.1 Control unit

The main part of the RISC processor block is the control unit, where its job is to control the flow of the process, programs and functions able to work properly. The control unit also connected with the input and output. It reads and interprets instructions and determines the sequence for processing the data.

It implements the instruction set and performs the tasks of fetching, decoding, managing execution and finally storing results. The control unit manage the translation the instructions to micro-instructions and handles the scheduling of the micro-instructions between various executions. Control unit also controls the flow of data through the processor and coordinates the activities with the other units within it.