DESIGN AND CHARACTERIZATION OF 20NM SOI MOSFET DOPING ABRUPTNESS DEPENDENT

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This report is submitted in partial fulfillment of requirement for the award of the Bachelor Degree of Electronic Engineering (Computer Engineering)

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Tajuk Projek : Design and Characterization of 20nm SOI MOSFET Doping Abruptness Dependent

Sesi Pengajian : 14/15

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I declare that this project report entitled *"Design and Characterization of 20 nm SOI MOSFET Doping Abruptness Dependent"*, is the result of my own research except as cited in the references.

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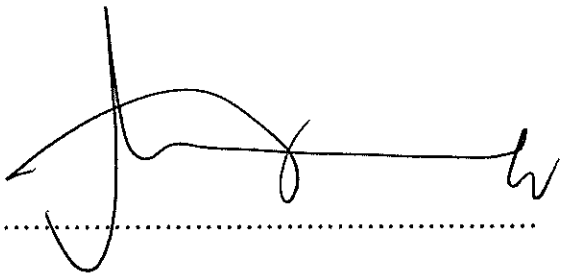
I hereby declare that I have read this project report and in my opinion this report is sufficient in terms of scope and quality for the award of the Bachelor Degree of Electronic Engineering (Computer Engineering)



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ABSTRACT

SOI MOSFET based currently becomes a trend for low power device such as palmtops, cell phone and other device due to increment of speed, density and circuit performance. Various efforts have been done to continue device shrinking dimensions and higher-frequency performance will be driven by market application. Reduction of SOI MOSFET dimension will lead to power reduction, reduce body effect, reduce parasitic capacitance and increase the density of chips. The internal resistance of the device is one of the factors that affect the device performance. Internal resistance can be controlled by choosing suitable doping abruptness of the device. In this project, I will focus on the doping abruptness of source/drain of the SOI MOSFET. The doping abruptness will varied to find the best of doping profile since the device is shrieked. In order to vary the doping abruptness of source/drain, there are several problems encountered, such as increasing of the internal resistance, threshold voltage, sub-threshold slope. The purpose of this project is to design the SOI MOSFET with an ideal doping abruptness and to investigate the impact on threshold voltage, drain current and sub-threshold slope due to the variation of the doping abruptness of source/drain of SOI MOSFET. This project will be designed by using Silvaco Athena and Silvaco Atlas. Silvaco Athena is used to simulate the device structure and Silvaco Atlas to obtain the device characteristic of the SOI MOSFET. This whole project will be implemented on 20nm of gate length of SOI MOSFET doping abruptness dependent.

ABSTRAK

Sejak kebelakangan ini, SOI MOSFET menjadi berleluasa untuk peranti berkuasa rendah seperti peralatan mudah alih, telefon bimbit dan lain-lain kerana ia mempunyai banyak kelebihan dari segi kelajuan, ketumpatan dan keuntungan prestasi. Pelbagai cara telah diusahakan untuk meneruskan process pengecilan dimensi dan berprestasi frekuensi tinggi kerana didorong oleh aplikasi pasaran. Pengurangan saiz SOI MOSFET akan membawa kepada pengurangan kuasa, mengurangkan kesan badan, mengurangkan kemuatan parasit, meningkatkan kepadatan dan sebagainya. Dalam projek ini, saya akan memberi tumpuan kepada kecerunan pendopan SOI MOSFET pada Sumber/Aliran. Nilai kecurunan pendopan akan diperbagai untuk mencari nilai yang terbaik seinring dengan pengecilan saiz SOI MOSFET. Dalam usaha untuk mempelbagaikan kecerunan dopand beberapa masalah akan dihadapi antaranya peningkatan rintangan, kenaikan voltan ambang, pengecilan cerun sub-ambang dan sebagainya. Tujuan project ini adalah untuk mereka bentuk SOI MOSFET dengan kecerunan pendopan yang sesuai dan kesan terhadap voltan ambang, arus dan cerun sub-ambang berikutan variasi nilai kecerunan dopand SOI MOSFET. Projek ini akan direka bentuk mengunakan perisian Silvaco Athena dan Silvaco Atlas. Silvaco Athena digunakan untuk simulasi struktur peranti dan Silvaco Atlas untuk mendapatkan ciri-ciri peranti SOI MOSFET. Keseluruhan projek akan dilaksanakan pada 20 nm panjang gerbang SOI MOSFET kebergantungan kecerunan pendopan.

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal Oxide Semiconductor
FET	-	Field-Effect Transistor
MOSFET	-	Metal-Oxide-Semiconductor Field Effect Transistor
nm	-	nanometer
BJT	-	Bipolar Junction Transistor
JFET	-	Junction field-effect transistor
OFET	-	Organic field-effect transistor
SOI	-	Silicon on Insulator
BOX	-	Buried Oxide
SIMOX	-	Separation by IMplantation of OXygen
TFT	-	Thin-Film Transistor
GIDL	-	Gate Induced Drain Leakage
ITRS	-	International Technology Roadmap for Semiconductor
LOP	-	Low Operating Power
EOT	-	Equivalent oxide thickness
TCAD	-	The technology Aided Design
V	-	Volt

LIST OF SYMBOLS

Vgs	-	Gate Voltage
Vds	-	Drain Voltage
I_{on}	-	Drain Current
Id	-	Drain Current
I_{off}	-	Leakage Current
SS	-	Sub-threshold Slope
Vth	-	Threshold Voltage
SiO_2	-	Silicon Oxide
σ	-	Doping Abruptness
y_1	-	First Point in y-axis
y_2	-	Second Point in y-axis
x_1	-	First Point in x-axis
x_2	-	Second Point in x-axis

LIST OF APPENDICES

CHAPTER I

INTRODUCTION

1.1 Introduction

In VLSI (Very Large Scale Integration) era, reducing power consumption becomes most important issue. Lots of techniques have been done to solve this problem such as they reducing the size of MOSFET, change the material, increase and the doping concentration. Since bulk MOSFET has reached its scaling limit, Silicon On Insulator (SOI) is introduced as one of the alternative to solve the problems occur in bulk MOSFET. SOI technology features a low capacitance, which enables high-speed operation. The supply voltage can be lowered to cut power consumption while adequate speed is provided. The SOI technology not only limited to power and speed, it also has other advantage in term of isolation, density and performance gain in low power electronics. Because of those advantages, the demand toward further downscaling of the device feature size is increased. However, the continuous device scaling invites the parasitic component of device such as the series resistance in the source/drain region that starts to limit the device performance. In this project, I will focus on the impact of doping abruptness of the source/drain SOI MOSFET on threshold voltage, drain current, current leakage and sub-threshold. The concentration of the doping of the SOI MOSFET will varies

and the gate control of the channel potential will enhanced. In order to vary of the doping abruptness of SOI MOSFET, there are several problems to be encountered, which are increasing the resistance, smaller the sub-threshold slope, degrades the device on-current and other. The purpose of this project is to design the SOI MOSFET with the best of doping abruptness of source/drain and to investigate the impact on threshold voltage, drain current, leakage current and sub-threshold slope of the SOI MOSFET due to the variation of doping abruptness of SOI MOSFET. This whole project will be implemented in 20nm SOI MOSFET gate length.

1.2 Project Objective

The objectives of this project are:

i. To design 20nm SOI MOSFET with an ideal doping abruptness of source/drain.

ii. To investigate the impact on threshold voltage, drain current, leakage current and sub-threshold slope of SOI MOSFET due to variation of doping abruptness of SOI MOSFET.

1.3 Problem Statement

In order to obtain the best doping abruptness of SOI MOSFET, the leakage current, drain current, sub-threshold slope and threshold voltage need to consider. But the problems that will be encounter are decreasing the sub-threshold slope, high sub-threshold current leakage in high speed circuit and reducing the doping abruptness will leads to high extrinsic parasitic resistance, this degrades the device on-current.

1.4 Project Scope

The scope of this project is to design and characterization of 20nm SOI MOSFET doping abruptness dependent. This project will be designed by using Silvaco ATHENA and Silvaco ATLAS software. Silvaco ATHENA was used to design the physical structure of the device, while Silvaco Atlas was used to obtain the electrical characteristic of the device. The design considers the doping abruptness, drain current, leakage current, sub-threshold slope and threshold voltage. The design is expected to get the best of doping abruptness of SOI MOSFET with same or better characteristic.

1.5 Report Structure

This report is a combination of five chapters that consist of introduction, literature review, methodology, result and discussion and lastly the conclusion and recommendation of the project. Details of this report structure are as follows:

Chapter 1 is an introduction of the project. This chapter will explain the objective of the project, the problem statement and the scope of the project.

Chapter 2 will discuss the study background related with the project which included the fundamental and the history of the creation of the device. The limitation of past generation MOSFET scaling also will discussed.

In Chapter 3, the methodology or approach to projects that have been implemented will discuss. Each selection and actions that may be done during project implementation will be clear and deep in stages until the project is successfully produced.

Chapter 4 describe the result was obtain from the project. It is include the new design of the SOI MOSFET and the new characteristic of the device.

Lastly, Chapter 5 is a conclusion for the whole project had been done and the recommendation for the future progress for this project.

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

This chapter will discuss a background study related to the project which includes a fundamental and the history of the creation of the device. The limitation of past generation MOSFET scaling also will be discussed.

2.2 Field-Effect Transistor (FET)

The Field-Effect Transistor (FET) is a device that consists of three terminals called source terminal, gate terminal and drain terminal. It is a semiconductor device that widely used in almost electronic application for example in an amplifier, medical instrument, mobile electronic etc. FET is the device that controls the voltage and can perform both amplifying and switching actions [4]. In general, FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particular useful in integrated-circuit (IC) design [2]. In the market consists various type of FET for example Junction field-effect transistor (JFET), metal-oxide-semiconductor field-effect transistor

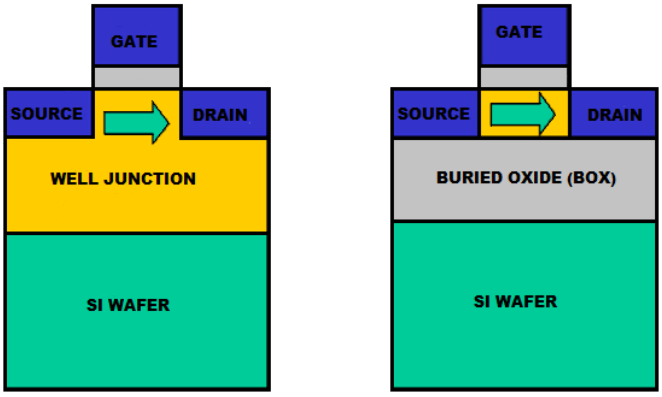
(MOSFET), Organic field-effect transistor (OFET) and others. In this project MOSFET categories will focus on Silicon on Insulator (SOI) which will be discussed at the next subtopic.

2.3 What is Silicon on Insulator (SOI)

Silicon-On-Insulator is a technology introduces because of the limitation of the bulk silicon technology. The benefits of SOI are provided lot of the benefit compare to bulk silicon technology. It is provide up to 90% power junction capacitance, reduce device cross-talk, near ideal sub-threshold swing, increased radiation hardness, no latch up and full dielectric isolation of the transistor [5].

2.3.1 Basic Construction

Silicon-On-Insulator is a silicon based device that constructs on an insulating substrate. Commonly substrate material made up from silicon dioxide but some of other cases, material such as ruby, diamond and sapphire are selected [6]. The structure of the SOI MOSFET is very similar with the bulk-MOSFET. The only difference is the presence of a thick layer if insulating material under the depletion region under the depletion region.



MOSFET on bulk Silicon MOSFET of SOI

Figure 2.1: Comparison of bulk and SOI structure

Silicon dioxide insulator is created by implement of oxygen into the silicon substrate. This fabrication process is known as separation by implanted oxygen (SIMOX). SIMOX process will create thick oxide layer at silicon substrate with specified depth. This process requires an oxygen ion implementing dose 200 to 500 times higher than the process implementing dose in bulk MOSFET fabrication [7]. This silicon layer is known as Buried Oxide Layer or BOX. Beside the BOX, there are two other important layers in SOI structure which is device layer and handle layer. Device layer is placed above the BOX which it is a this surface layer where the transistor are formed. Handle layer is placed underneath the BOX. It is un-doped silicon that is only used for handling the wafer during the fabrication.

2.4 History of Silicon on Insulator

The introduction of Silicon on Insulator MOSFET start around sixth decade ago which is from 1960's and the first implemented in the thin-film transistor (TFT). SOI device was born by the development of Separation by Implemented Oxygen (SIMOX) fabrication process by Watanabe and Tooi. They implement oxygen ion into silicon substrate using an RF gas discharge. In 1978, Izumi discover the way to produces a continues buried SiO_2 layer with the excellent characteristic by implantation of oxygen into silicon at an acceleration voltage 150 kV and a dose of 1.2×10^{18} cm^{-2} with the annealing temperature of 1150° C. This process will left a thin layer of single-crystal silicon on the surface [1].

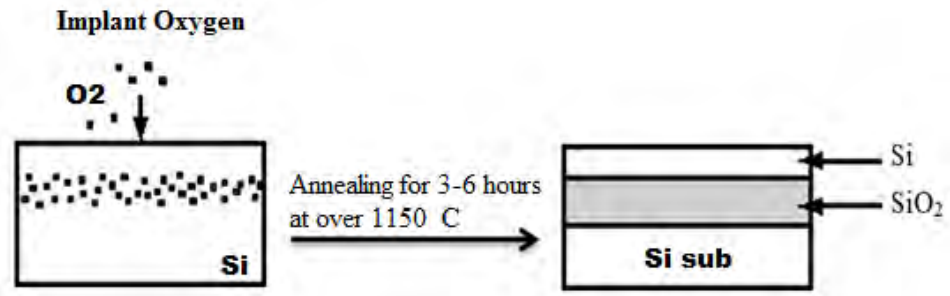


Figure 2.2: SIMOX Process

In early 80s, intensive research on the technique of recrystallization with laser or e-beam. It turned out, however, to be possible circumvent photolithography limitation by using a shorter wavelength of the light source [13]. In the middle 80s Fully-depleted SOI MOSFET began attracting attention because of their advantage. Engineers concentrate analysis of drain breakdown phenomena and improvement of the drain breakdown voltage [1].

Moreover, in 90s, new technology was discovering which is using 'dose window'. It is known as ITOX technology. The throughput of SIMOX technology was increased by a factor of 5, the dislocation density was reduces to