CHARACTERIZATION AND OPTIMIZATION OF PLANAR POWER MOSFET DEVICE

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For my beloved family and wonderful friends.

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ABSTRACT

Electronic world nowadays demands devices to function at their optimum performance. Power MOSFET is a device which can offer to fulfil the demand. Power MOSFET is well known for their low gate driver power, fast switching speed, and superior paralleling capability. In this project, we analyze the electrical characteristics of Planar Power MOSFET and do the optimization approach of Planar Power MOSFET by using L9 Orthogonal Array in Taguchi method. The simulation of the fabrication process of Planar Power MOSFET is performed by using ATHENA module. Meanwhile, the simulation of electrical characteristics process of Planar Power MOSFET is performed by using ATLAS module. Planar Power MOSFET device performs best when the V_{TH} value at 1.47901V which is within the range of standard V_{TH} value (1V to 2V), I_{ON} value at 62.3916μA/μm, I_{OFF} value at 0.5138pA/μm and SS values at 102.61mV/decade. From the electrical characteristics values obtained, R_{ON} value calculated is 160.277kΩ and I_{ON}/I_{OFF} value calculated is 121.3417×10^6. The extracted and calculated electrical characteristics values are all within the range which suggested by Taguchi method. This shows that Taguchi method can predict the optimum solution of fabrication for a good performance of Planar Power MOSFET.

ABSTRAK

Dunia elektronik masakini memerlukan peranti untuk berfungsi pada kadar yang optimum. MOSFET kuasa merupakan satu peranti yang mampu memenuhi kriteria tersebut. MOSFET kuasa terkenal dengan kuasa pemacu gate yang rendah, kelajuan pensuisannya, dan kebolehan berjajaran yang tinggi. Dalam projek ini, kami menganalisis ciri-ciri elektrik dan melakukan pendekatan pengoptimuman bagi MOSFET kuasa berbentuk satah dengan menggunakan L9 *Orthogonal Array* dalam kaedah Taguchi. Simulasi proses fabrikasi untuk MOSFET kuasa berbentuk satah dilakukan dengan menggunakan modul ATHENA. Manakala simulasi proses ciri-ciri electrik untuk MOSFET kuasa berbentuk satah dilakukan dengan menggunakan modul ATLAS. Peranti MOSFET kuasa berbentuk satah berfungsi pada kadar terbaik apabila nilai V_{TH} pada 1.47901V yang berada dalam lingkungan nilai V_{TH} standard (1V ke 2V), nilai I_{ON} pada 62.3916μA/μm, nilai I_{OFF} pada 0.5138pA/μm dan nilai SS pada 102.61mV/dekad. Berdasarkan nilai ciri-ciri elektrik yang diperoleh, nilai R_{ON} yang dikira adalah 160.277kΩ dan nilai I_{ON} / I_{OFF} dikira adalah 121.3417×10^6. Semua nilai ciri-ciri elektrik yang diperoleh dan dikira berada dalam ramalan lingkungan nilai yang dicadangkan oleh kaedah Taguchi. Ini menunjukkan bahawa kaedah Taguchi boleh meramalkan solusi fabrikasi yang optimum untuk MOSFET kuasa berbentuk satah berfungsi dengan baik.

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LIST OF ABBREVIATIONS

Abbreviation	Full Word
AC	Alternating Current
ANOVA	Analysis of Variance
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Silicon
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DOF	Degree of Freedom
IC	Integrated Circuit
MOSFET	Metal-Oxide-Silicon Field-Effect Transistor
N	Noise
NPN	Negative-Positive-Negative
OA	Orthogonal Array
S/N	Signal to Noise Ratio
S	Signal
TCAD	Technology Computer-Aided Design
VLSI	Very-Large-Scale-Integrated

LIST OF SYMBOLS

Symbol	Meaning
BV_{DSS}	Breakdown Voltage
C_{DS}	Drain-to-Source Capacitance
C_{GD}	Gate-to-Drain Capacitance
C_{GS}	Gate-to-Source Capacitance
I_D	Drain Current
I_{OFF}	Leakage Current
I_{ON}	Drift Current
R_{ON}	On-Resistance
SS	Subthreshold Swing
V_D	Drain Voltage
V_{DON}	On-Voltage
V_{DS}	Drain-to-Source Voltage
V_G	Gate Voltage
V_{GS}	Gate-to-Source Voltage
V_{TH}	Threshold Voltage

CHAPTER 1

INTRODUCTION

1.1 Background

Electronic world nowadays demands devices to function at their optimum performance. Power Metal Oxide Semiconductor Filed Effect Transistor (MOSFET) is a device which can offer to fulfil the demand. Power MOSFET is well known for their low gate driver power, fast switching speed, and superior paralleling capability. Engineers believe that with further research and designing in the Power MOSFET switching function, would definitely make Power MOSFET become an ideal switch. Power MOSFET does perform the same function as the NPN of Bipolar Junction Transistor (BJT) in terms of amplifying and switching applications, and come with the additional benefits which are it can handle specific power levels. Power MOSFET came in several types of structures such as D-MOSFET, U-MOSFET, SC-MOSFET, CC-MOSFET, GD-MOSFET and SJ-MOSFET. By records, double diffused MOSFET structure which is famously known as D-MOSFET structure is the first Power MOSFET structure commercially introduced by the power semiconductor industry. However, all types of structures have their own advantages and disadvantages [1].

Most Power MOSFET features a vertical structure with source and drain on opposite sides of the wafer in order to support higher current and voltage. The

channel length of Power MOSFET device could be reduced by sub-micron dimensions by controlling the diffusion depth of the P- base and N+ source region. Power MOSFET can also perform best when it comes to the high-voltage applications. This approved by its ability to support hundreds amperes of drain current, compare to conventional MOSFET, which normally supports milliampere of drain current [1].

1.2 Objectives

The main objectives of this project are to design and simulate Planar Power MOSFET device by using SILVACO TCAD tools. Other objectives also being described as the guideline for this project as following;

i) To analyze the electrical characteristics of Planar Power MOSFET device.
ii) To do optimization approach of Planar Power MOSFET device by using L9 Orthogonal Array in Taguchi method.

1.3 Scopes of Project

The scope of this project presents the overall performance of Planar Power MOSFET device by using SILVACO TCAD tools. This project research is based on simulation and programming development of Planar Power MOSFET device. Several electrical characteristics that will be studied based on the simulation and programming development are I_{ON}, I_{ON}/I_{OFF} current ratio, threshold voltage (V_{TH}) and subthreshold swing (SS). The parameters of the device will also be studied. The study of parameters will involve an effect of varying doping dose for source and body implementation, effect of varying the diffuse time for diffusion method, and effect of varying gate oxide thickness. Other than that, L9 Orthogonal Array in Taguchi method will be utilized in order to result in optimum performance of the device.

1.4 Problem Statement

With the enormous expansion of the mobile equipment market, great needs of the sophisticated and efficient high-current DC/DC converters (sub-10V) arise, entailing in struggles to improve the electrical performance of the switching Planar Power MOSFET or pass transistors, which is the key element of the low-voltage smart power integrated circuits (ICs) [2]. A high-current driving, a low on state drain to source on-resistance (R_{ON}), which is obtained by the inverse of the slope of the drain current (I_{DS}) as a function of the drain voltage (V_{DS}) curve, for a given gate voltage (V_{GS}) in the triode region of MOSFET, and a low parasitic capacitance are the main specifications of a Planar Power MOSFET [3]. In order to improve the performance of Planar Power MOSFET, the parameters of the device will be varied and L9 Orthogonal Array in Taguchi method will be utilized in order to result in optimum performance of the device.

1.5 Outline of Report

This thesis is a combination of five chapters that consists of introduction, literature review, methodology, result and discussion, and the last chapter is conclusion and recommendation of the project.

The first chapter is an introduction to the project. In this chapter, we will explain the overview of the project briefly. This chapter also includes the objectives of the project, the scopes of the project, and the problem statement.

Second chapter is mostly discussing about the literature reviews which are related to this project based upon previous researches done. This chapter also contains theories related to the project which is mostly about the electrical characteristics of the Planar Power MOSFET. The electrical characteristics of the Planar Power MOSFET are discussed in detail because it is important to understand the characteristics of the device before optimize it by using Taguchi method.

Third chapter is on the method used in designing and simulating the device. This chapter also focuses on the characterization and optimization of the device. Chronology of the project and the methods used at each step are explained in detail. In supporting the chronology and methods, flowchart and diagrams will be shown throughout this chapter.

The fourth chapter is focused on the result obtained from the process of characterizations and optimization of the Planar Power MOSFET. The results are also analyzed and discussed to ensure that it meets the objectives of the project.

Fifth chapter is the conclusion and recommendation of the project. This chapter concludes the whole project and proposes recommendations for the future works.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The continuous growth in integrated circuit (IC) density and speed is the heart of the rapid growth of electronics [4]. The electronics industry is now the largest industry in terms of output as well as employment in many nations. It will be no doubt that this big industry will continue playing more important role in economic, social, and even political development throughout the world [5].

This importance is the motivation as well as a formidable driving force that urges the continued rise in IC integration density and speed. The rise in circuit density and speed has been accompanied by the scaling of MOSFET to lower the cost per function and meanwhile increase the performance and functionality of the circuits. Metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important and fundamental building block of very-large-scale-integrated (VLSI) circuits today in IC industry. MOSFET is extremely popular in electrical components. MOSFET is transistors, which contain four terminals, namely the gate, body, source, and drain. When the sufficient voltage is supplied from the gate to the body terminal, an electrical connection is opened between the source and the drain terminals [6].

2.2 Planar Power MOSFET Structure

The cross section of Planar Power MOSFET is shown in the Figure 2.1. From the figure, the main difference compared to the Lateral MOSFET is the location of the source and drain. In the Lateral MOSFET, the source and drain appear side by side in horizontal but in the Power MOSFET the source and drain appear in vertical as to withstand the higher voltage applied. The other reason for this is to make possible lower on-state resistances and faster switching than the Lateral MOSFET. The existence of the epitaxial layer is mainly to support the high voltage applied [8]. In most of Power MOSFET structures, the N+ source and P- body junction are shorted through source metallization to avoid accidental turn on of the parasitic bipolar transistor.

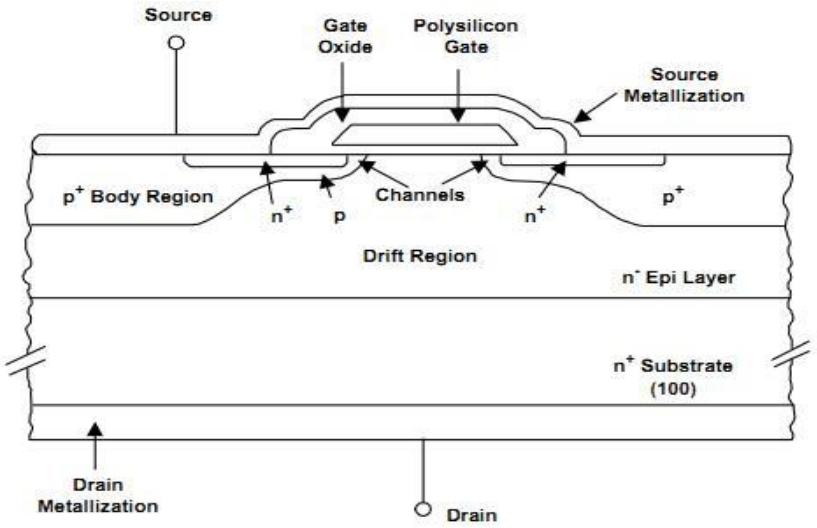

Figure 2.1: Planar structure of Power MOSFET with junction indicator [7].

This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N+ substrate. The channel is formed by the difference in lateral extension of the P- base and N+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand-side and right-hand-side of the gate region during ion-implantation to introduce the respective dopants. Polysilicon which will act as the refractory gate electrodes is required to allow diffusion of the dopants under the gate electrode at elevated temperatures.