APPLICATION OF TAGUCHI METHOD IN THE OPTIMIZATION

OF THE SOI MOSFET

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This report is submitted in partial fulfilment of the requirements for the Bachelor of Electronic Engineering (Computer Engineering) with Honors

Faculty of Electronic and Computer Engineering

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Dedicated to my beloved family especially my parents, supervisor, lecturers and all my friends who helping me whether directly or indirectly.

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ABSTRACT

This project is about the optimization of Silicon-On-Insulator (SOI) MOSFET device by applying Taguchi Method. Silicon-On-Insulator (SOI) wafers are bound to play a key role in next generations Complementary Metal Oxide Semiconductor (CMOS) nanometre technology. This method was used to analyse the experimental data in order to get the optimum results. In this paper, there are four factors were varied for 3 levels to perform 9 experiments which are Pocket-Halo Implant Dose, Pocket-Halo Implant Energy, Source/Drain Implant Dose and also Source/Drain Implant Energy. The traditional SOI structure consists of a silicon dioxide layer sandwiched between a top thin silicon layer in which devices are built and the silicon substrate. Meanwhile, SILVACO TCAD tools will be used to design SOI Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The aim of this project is to design an 10nm SOI MOSFET device by using SILVACO TCAD tool, to analyse the electrical characterization of SOI MOSFET by using ATLAS SILVACO TCAD tool and to optimise the performance of SOI MOSFET device by applying Taguchi Method. One of the way to optimize the performance of the SOI MOSFET is to alter the SOI layer thickness and the electrical characteristic degraded when the effective gate length of SOI MOSFET was reduced. The best thickness is 10nm thickness layer of SOI MOSFET.

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ABSTRAK

Projek ini adalah mengenai pengoptimuman peranti Silikon Pada Penebat (SOI) MOSFET dengan menggunakan Kaedah Taguchi. Wafer Silikon Pada Penebat (SOI) terikat memainkan peranan penting dalam generasi seterusnya Komplementari Metal Oxide Semiconductor (CMOS) teknologi nanometer. Kaedah ini telah digunakan untuk menganalisis data ujikaji untuk mendapatkan hasil yang optimum. Dalam kertas ini, terdapat empat faktor yang telah diubah untuk 3 peringkat dengan melaksanakan 9 eksperimen seperti Pocket-Halo Dos Implan, Pocket-Halo Implan Tenaga, Sumber / Parit Dos Implan dan juga Sumber / Parit Tenaga Implan. Struktur SOI tradisional terdiri daripada lapisan silikon dioksida yang diapit di antara bahagian atas lapisan silikon nipis di mana peranti dibina dan substrat silikon. Sementara itu, alat TCAD SILVACO akan digunakan untuk mereka bentuk SOI Metal Oxide Semiconductor Field Kesan Transistor (MOSFET). Tujuan projek ini adalah untuk mereka bentuk alat 10nm SOI MOSFET dengan menggunakan alat SILVACO TCAD, untuk menganalisis pencirian elektrik SOI MOSFET dengan menggunakan alat ATLAS SILVACO TCAD dan mengoptimumkan prestasi peranti SOI MOSFET dengan menggunakan Kaedah Taguchi. Salah satu cara untuk mengoptimumkan prestasi SOI MOSFET adalah dengan mengubah ketebalan lapisan SOI dan ciri-ciri elektrik dibina apabila panjang pintu berkesan SOI MOSFET dikurangkan. Ketebalan terbaik adalah lapisan yang berketebalan 10nm pada SOI MOSFET.

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LIST OF ABBREVIATIONS

SOI	-	Silicon-On-Insulator
MOSFET	-	Metal-Oxide Semiconductor Field Effect Transistor
ITRS	-	International Technology Roadmap Semiconductor
SIO_2	-	Silicon Dioxide
TCAD	-	Technology Computer Aided System
SNR	-	Signal to Noise Ratio
Nm	-	Nanometre
NMOS	-	N-Channel MOSFET
PMOS	-	P-Channel MOSFET

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LIST OF SYMBOLS

I_D	-	Drain Current
I_{OFF}	-	Leakage Current
V_{DS}	-	Drain to Source Voltage
V_G	-	Gate Voltage
V_{TH}	-	Threshold Voltage
I_{ON}	-	Drive Current
V_{SS}	-	Subthreshold Voltage
S/N	-	Signal to Noise

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CHAPTER 1

INTRODUCTION

1.1 Background.

Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is a unique form of Field-Effect Transistor (FET) that works by electronically varying the width of a channel along which charge carriers (electrons or holes) flow. The wider the channel, the better the device conducts. The charge carriers enter the channel at the source, in addition to exit over the drain. The width of the channel is controlled by the voltage on an electrode called as the gate, which are located bodily between the supplier as well as the drain. The Gate is insulated from the channel by an exceedingly thin layer of metal-oxide.

There are two ways of MOSFET can be functioning. Firstly, the MOSFET is known as depletion mode. When there is no voltage on the gate he channel demonstrates its maximum conductance. Since the voltage about the gateway is actually increased, the channel conductivity can reduce. Secondly, a MOSFET can work that called as enhancement mode. When there is no voltage on the gate, the device does not conduct. A channel is produced by the application of a voltage to the gate. As a conclusion, the greater the gate voltage, the better the device conducts.

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The MOSFET has several advantages than the conventional junction FET or JFET. The gate of the MOSFET is insulated electrically from the channel, no current flows between the gate and also the channel. So, the MOSFET has pretty much infinite impedance. This makes MOSFETs very useful for power amplifiers. The device also suitable to high-speed switching applications. Some integrated circuit (ICs) contains MOSFET and used in computers.

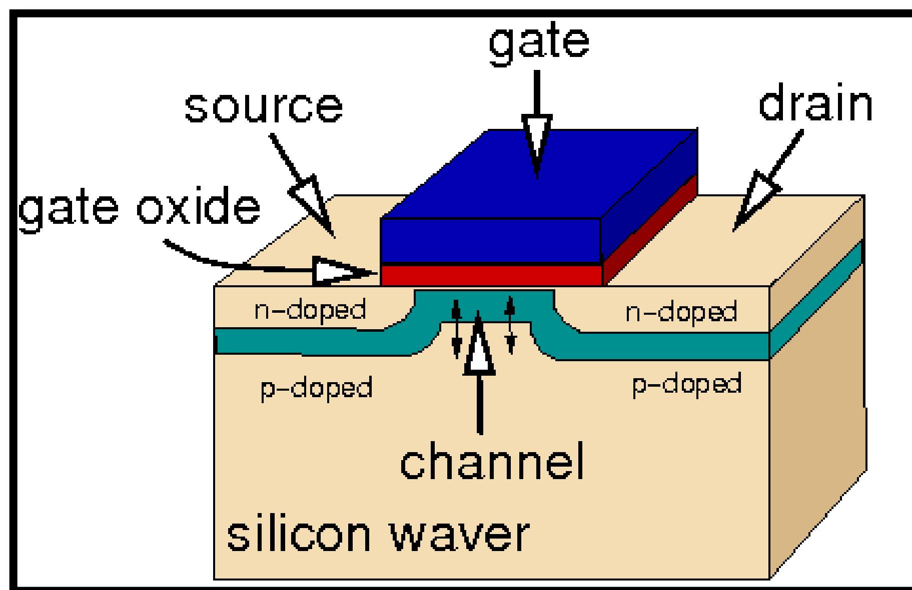

Figure 1.1: The basic structure of the MOSFET.

Silicon-On-Insulator (SOI) is a new way of starting the chip making process, by replacing the bulk silicon wafers (approximately 0.75 mm thick) with wafers which consist three layers of Handle layer, Buried Oxide layer (BOX) and Device layer. Handle layer, also known as a thin surface layer of silicon (from a few hundred Angstroms to several microns thick) where the transistors are formed, an underlying layer of insulating material and a support or "handle" silicon wafer. The Buried Oxide layer (BOX) also known as an insulating layer, usually made of silicon dioxide is usually a few thousand Angstroms thick. When transistors are built within the thin top silicon layer, they switch signals faster, run at lower voltages and much less vulnerable to signal noise from background cosmic ray particles. Since on an SOI wafer each

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transistor has been isolated from its neighbour by a complete layer of silicon dioxide, they are immune to "latch-up" problems and can spaced closer together than transistors built on bulk silicon wafers. Latch-up is a type of short circuit which can occur in an improperly designed Integrated Circuit (IC). Building circuits on SOI allows for more compact chip designs, resulting in smaller IC devices (with higher production yield) and more chips per wafer (increasing fab productivity). SOI enables increased chip functionality without the cost of major process equipment changes (such as higher resolution lithography tool). The advantages of IC devices built on SOI wafers (mainly faster circuit operation and lower operating voltages) have produced a powerful surge in the performance of high-speed network servers and new designs for handheld computing and communication devices with longer battery life. Advanced circuits, using multiple layers if SOI-type device silicon, can lead the way to a coupling of electrical and optical signal processing into a single chip resulting in a dramatic broadening of communication bandwidth with new applications such as global ranging, direct-link entertainment and communication with handheld devices. Figure 1.1 shows that Silicon-On-Insulator (SOI) in MOSFET layer.

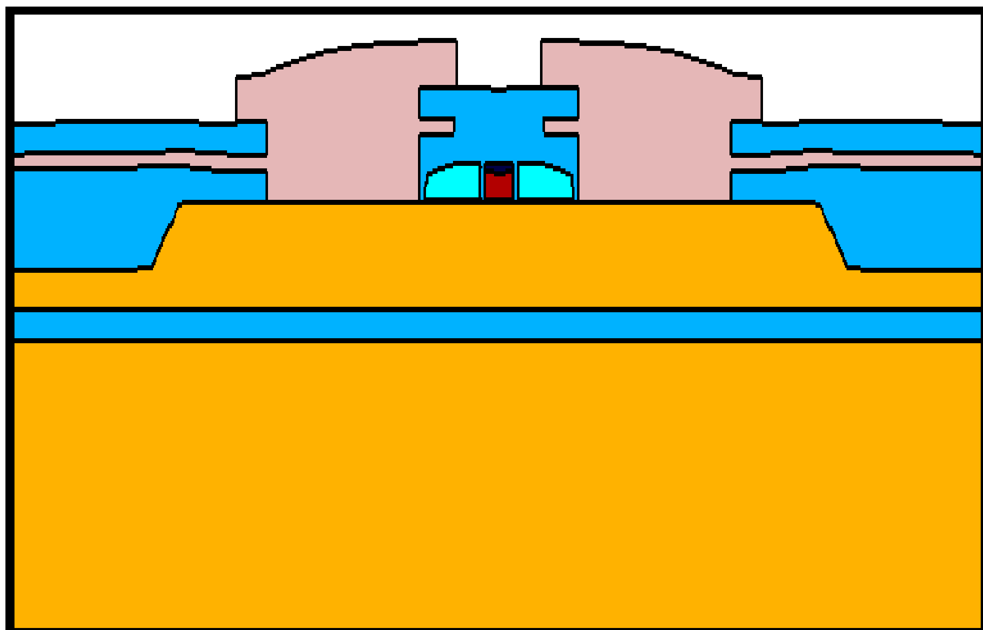

Figure 1.2: SOI MOSFET structure.

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The purpose of this research is to design and analyse the application of Taguchi Method within the search engine optimization associated with Silicon-On-Insulator (SOI) Metal-Oxide-Semiconductor Field Effect transistor (MOSFET) performance using Technology Computer-Aided Design (TCAD) tool. TCAD tool is a program that's been made to allow the creation, fabrication, and simulation of semiconductor devices. This TCAD tool is used for designing various applications for semiconductor device. Silicon-On-Insulator (SOI) device is a silicon-based device built upon insulating substrate.

1.2 Objectives of the project.

The main goal of this research is to apply the Taguchi Method in the optimization of SOI MOSFET. Specifically, the objectives are:

I. To analyse the characterization of SOI MOSFET by using the ATLAS SILVACO TCAD tool.
II. To compare the electrical characteristic between SOI MOSFET and conventional bulk MOSFET.
III. To design an initial SOI-MOSFET device design by applied of Taguchi Method.

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1.3 Problem Statement.

In the material universe, before certain MOSFET device, proceed with the fabrication process the SILVACO TCAD tool (virtually fabrication tool) will be used to design it at the first hand. This will make the cost of production been minimized effectively. In current MOSFET devices, there is physical limitation, which is the short channel effect that is found in conventional MOSFETs as the gate length is further downsized. SILVACO TCAD tool (virtually fabrication tool) will be used to design the MOSFET device at the first hand before certain devices proceed with the fabrication process. This will make the cost of production been minimized effectively. In current MOSFET devices, there is physical limitation, which is the short channel effect that is found in conventional MOSFETs as the gate length is further downsized.

There are also a few problems in device performance for such an example, switching effect, which came from the higher leakage current (IOFF) [1]. Besides, the high-power usage and low speed characteristic of conventional circuit MOSFET must be improved to a new level so that this device can improve and be a lot more useful for future. Hence, the new device concept that has more improved than conventional MOSFET is introduced. That device calls Silicon-On-Insulator (SOI) MOSFET. To prove that statement, research has been conducted to analyse the characteristic of SOI MOSFET by applying the Taguchi Method.

1.4 Scope of the project.

This research mainly focused on the application of Taguchi Method in the optimization of Silicon-On-Insulator (SOI) MOSFET. Other than that, this project was conducted by using SILVACO's TCAD tool. The SILVACO's TCAD simulation tool is software that simulates and design device structures to minimize the cost of fabrication. This project consists of ANTHENA and ATLAS TCAD tool.

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1.5 Project Outline.

This project contains five chapters. Chapter One is describes about the introduction of Silicon-On-Insulator MOSFET by applying the Taguchi Method that will be studied in the research, problem statement of the project, objective of the project, the aim of the project that describe the cause for developing this project, the scope of the project and organization of the project.

Chapter Two is a literature review about Taguchi Method and Silicon-On-Insulator MOSFET. This chapter reviews on previous research about the topic related to the task. Several method and approaches that related to the project are discussed and critiqued.

Chapter Three explains the methodology of the project. This project will use ATHENA and ATLAS simulation tool. The flow chart of the project and the algorithms use is explained in this chapter. This is also where the MOSFET structure is designed and produced using the SILVACO software.

Chapter Four is discussing on the TCAD simulation and elaboration regarding the results obtained and to more specifically be the characteristic of SOI MOSFET. In the conclusion of the report writing Chapter Five will concludes the project findings and recommendation for the further work.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction of MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor).

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is very common and widely utilized in electronic fabrication. This device are uses in microprocessor and semiconductor memories. This MOSFET also an important power device in industry. Figure 2.1 shows basic structure of MOSFET device [4].

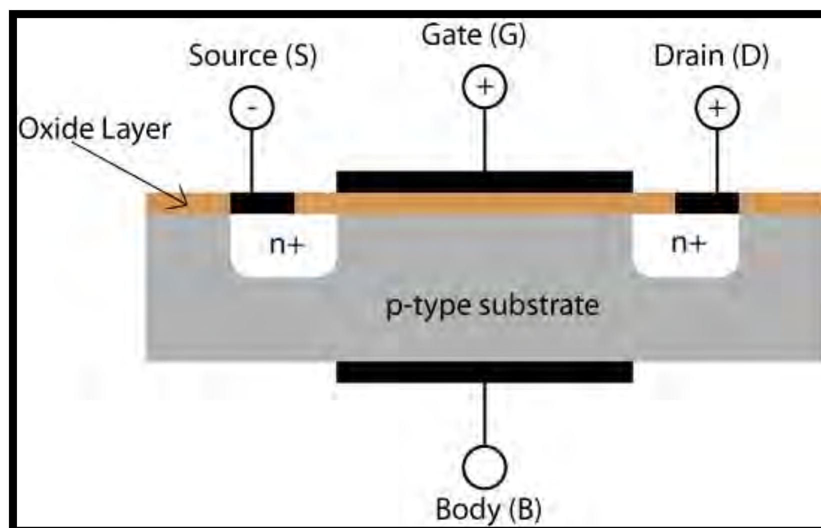

Figure 2.1: Basic structure of MOSFET device.

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