THE IMPACT OF SILICON BODY THICKNESS ON DEVICE PERFORMANNCE OF 18nm LOW POWER SILICON ON INSULATOR

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This Report Is Submitted In Partial Fulfilment Of Requirement For The Bachelor Degree Of Electronic Engineering (Computer Engineering) With Honours

FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

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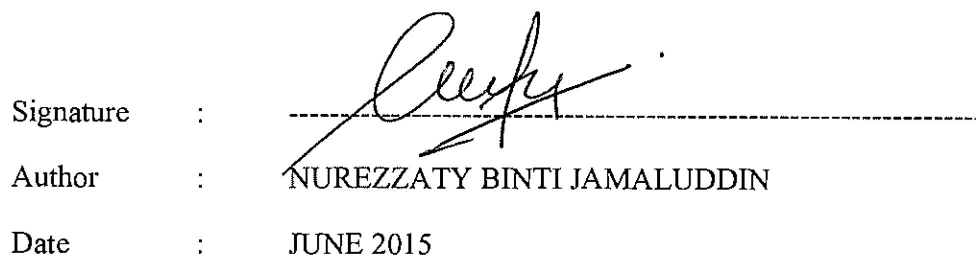

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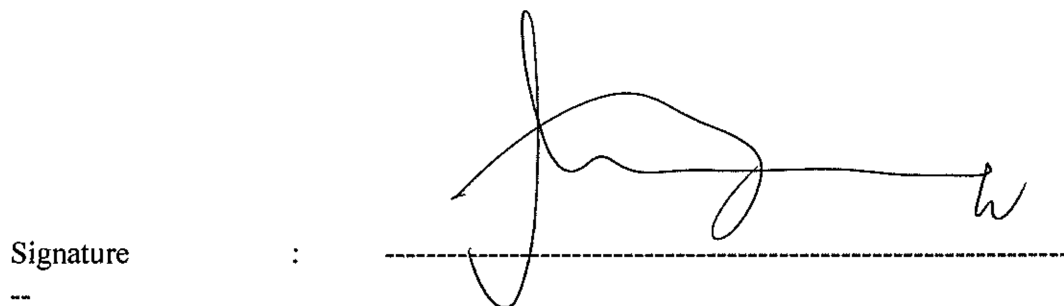

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ABSTRACT

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is type of transistor that used for switching and amplifying electronic signals. Year by year, MOSFET continuously been shrinking down in size in order to fulfil the market demand but this downsizing of MOSFET is come to the end due to many problems occur. Silicon on Insulator (SOI) is being introduced to overcome the problem in bulk MOSFET such as short channel effect. This project aimed to study the impact of silicon body thickness on device performance SOI for low power application. The studies will include the analysis of electrical characteristic of device which is threshold voltage, current leakage and subthreshold slope. Body thickness plays an important role to produce a good device performance where it has high potential solution to the ultimate scaling of SOI MOSFET. Designs parameters use in this project are from International Technology Roadmap Semiconductor (ITRS) 2011 edition. In order to design, SILVACO software using ATHENA and ATLAS are used. ATHENA is used to design the structure of device by following the parameter set in the ITRS while ATLAS used to obtain the electrical characteristic of device. The impact of this project can be clearly analysed by electrical characteristic for five different thickness of silicon body which used 18nm gate length for all design. In order to achieve the target performance some trade off occurs such as large leakage current.

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ABSTRAK

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) adalah sejenis transistor yang digunakan sebagai penguat atau pensuisan isyarat elektronik. Tahun demi tahun, saiz MOSFET dikurangkan secara beterusan untuk memenuhi permintaan pasaran tetapi pengecilan MOSFET sudah tiba keakhirnya berikutan banyak masalah yang timbul seperti kesan seluran pendek. Projek ini bertujuan untuk mengkaji kesan ketebalan badan silikon pada prestasi peranti untuk aplikasi kuasa rendah. Kajian ini melibatkan analisis ciri-ciri elektrik bagi peranti seperti voltan ambang, arus bocor dan kecerunan sub-ambang. Ketebalan badan memainkan peranan penting untuk menghasilkan prestasi peranti yang baik di mana ia mempunyai potensi yang tinggi untuk pengecilan saiz SOI MOSFET ketahap maksimum. Parameter yang digunakan dalam projek ini diambil dariInternational Technology Roadmap Semiconductor (ITRS) edisi 2011. Untuk mereka bentuk peranti, perisian SILVACO menggunaka ATHENA dan ATLAS digunakan. ATHENA digunakan untuk mereka bentuk struktur peranti dengan mengikut parameter yang ditetapkan dalam ITRS manakala ATLAS digunakan untuk mendapatkan ciri-ciri elektrik bagi peranti. Kesan daripada projek ini boleh dianalisis dengan jelas bagi lima jenis ketabalan badan silicon yang berlainan yang mengunakan panjang gate yang sama iaitu 18nm. Dalam usaha untuk mencapai prestasi yang disasarkan beberapa kekurangan akan berlaku seperti kebocoran semasa yang besar

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CHAPTER I

INTRODUCTION

1.1. Project Introduction

MOSFET is used as a switching device in electronic world. Year by year, the size as be continuously scaled down to make the transistor smaller to pack more and more devices in a given chip area. Smaller physical size can make transistor switching process faster compare to larges size. The main part that been normally scaled are channel length, channel width, and oxide thickness. However, the more the size had been reducing, many problems occur during designing the MOSFET.

SOI has been introduced in 1980s in order to improve the SIMOX technology. The silicon layer thickness can be in range in micron which is very small in size. With SOI technology it can increase chip functionality without big changes of the design. Silicon on insulator consists of three main layer silicon body, buried oxide (BOX) and bulk. The difference between SOI MOSFET and bulk MOSFET is the existing of the BOX layer between the silicon body and the bulk. SOI is a planar process technology that relies on primary innovation which is ultra-thin layer of insulator called the buried oxide that positioned on top of the base silicon.

There are several advantages of SOI MOSFET which are negligible drain to substrate capacitance which can help to improve the switching speed of the device. Besides there is no latch up occurs, and not requires any extra circuit to prevent the

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latch up. The leakage current more smaller in SOI structure in order to apply for low standby power device such as a mobile phone. [1]

This project will focus on impact of silicon body thickness on device performance of 18nm gate length for low power application. Refer to 2011 overall roadmap technology characteristic (ORTC) by ITRS the parameter changes in every year. The main focus in this project is reducing the body thickness because it is has potential for ultimate scaling of MOSFET. Besides that, it can improve the power consumption, threshold voltage and current. But, reduction of body thickness will lead to transistor gate leakage current and change the slope of threshold voltage as it affected by deducting of SOI body thickness.

1.2. Problem Statement

Semiconductor industry never fails to undergo improvement of device in every year consistent with advancement in nowadays technology. Scaling down size of device is major topics in semiconductor industry due to many problems occur such as large current leakage, increases of threshold voltage and increase of internal resistance. In this project, all the problems will be given more attention in order to gain a better device.

1.3. Objective

1. To design and simulate the SOI with reduction of silicon body thickness by using ATHENA and ATLAS from SILVACO.
2. To analyse the impact of silicon body thickness on device performance using 18nm gate length.
3. To analyse the threshold voltage, current leakage and sub threshold slope.

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1.4. Scope

This project is focused on analysing the impact of silicon body thickness on device performance using 18nm gate length. All design parameters will be Refer to 2011 ORTC. First, main design of SOI will be created and all the parameters will be analysed. After that, the thickness of body silicon will be deducted by 0.2nm continuously and the impact of these changes will be analysed. In order to analyse this result, simulation tools that will be used are ATHENA and ATLAS by SILVACO. ATHENA used for designing the structure of device and ATLAS used to obtain the device electrical characteristic. This project will success if the good impact is produce by reduction of silicon body thickness.

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CHAPTER II

LITERATURE REVIEW

2.1 Silicon on Insulator (SOI)

Research on SOI has been done about two decades in order to have better device performance for electronic industry [3]. Structure of SOI is not much different compared to normal bulk MOSFET. The major difference is the insertion of insulation layer beneath on device [2]. SOI MOSFET is the evolution of bulk MOSFET in order to overcome the problem that occurs in bulk MOSFET. SOI is becoming mainstream technology for future high performance and low power application. SOI contains three main layer which are body silicon, buried oxide (BOX) and bulk. BOX is a new layer that makes the major difference between SOI and bulk MOSFET as shown in figure 2.1.

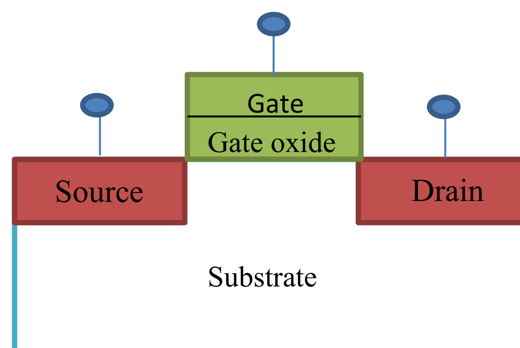

Figure 2.1: Bulk MOSFET

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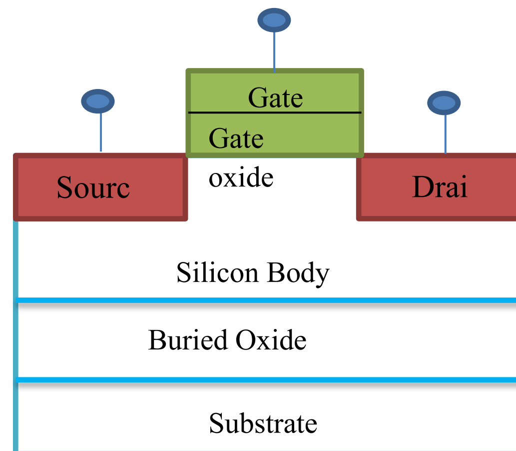

Figure 1.2: SOI MOSFET

2.2 Miniaturization

SOI is one of manufacturing strategies to miniaturize of microelectronic device. A long before SOI technology been introduced, bulk MOSFET has been continuously scaled down in size for the purpose to make the transistor smaller so that more chips can be placed on the wafer. The benefit of the miniaturization size can lead to slowing down the price per chip at the same time still has the same function as before. In fact the number of transistor per chip has been double every 2 to 3 years [4].

It already proved that smaller transistor will switch faster. So that, the reduction of size will scale down overall MOSFET parameters involving it channel length, channel width and the thickness of overall body. Year by year the size of MOSFET is getting smaller and many difficulties arises such as higher sub-threshold voltage is needed but the shrinking of size will reduce the voltage in order to maintain the reliability. As for that, sub-threshold voltage also been reduce but the problem occurs because the transistor cannot be switched from turn off to turn on. The MOSFETs also face with increases of junction leakage, lower output resistance and interconnect capacitance [2]. Research have found that SOI MOSFET could overcome the problem occurs in bulk MOSFET.

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After SOI MOSFET is been introduced SOI technology also begins to shrink down to fulfil the market demands. Shrinking down the size will lead to several problems as many layer and part of the transistors already changed. It is no doubt that SOI have a lot of advantage as it has faster speed and low power consumption [5]. But the shrinking down the size will cause the high series resistance [7], higher source/drain patristic resistance and thermal instability [6].

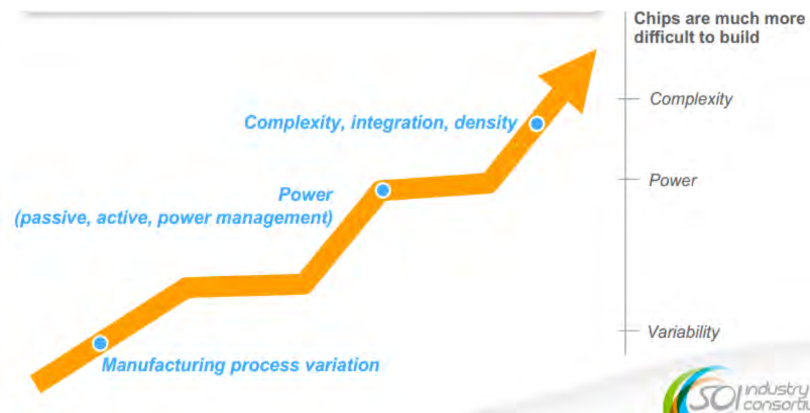

Figure 2.3: Challenge in Chips Development [17]

2.3 Moore's Law

Dynamic of silicon revolution has followed the guide of Moore's Law that predict the economic and technical trends of integrated circuit. It already describe that long term trend in history that the number of transistor can be placed on integrated circuit are doubling increased year by year [18]. Moore's law already serves as the emblem for the whole of technologies change [9].

Moore's law already described the increment of transistor density. It said that the reduction of size of the physical MOS device has improved the circuit speed and it density [8].

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2.4 Silicon Body Thickness

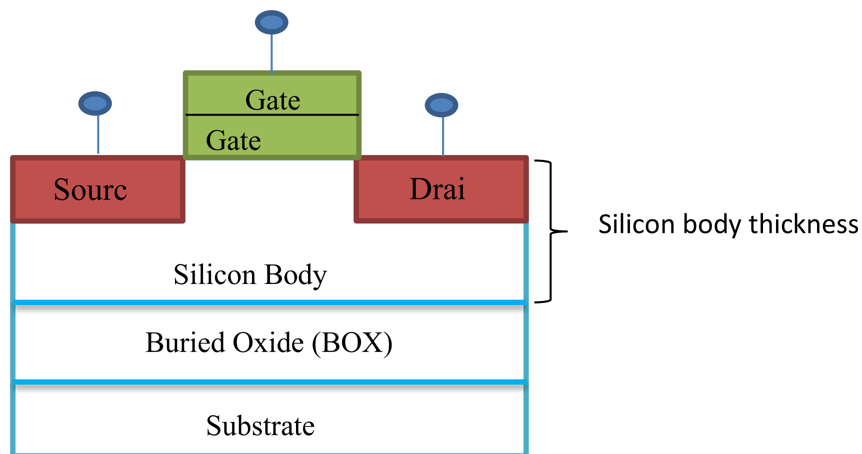

Figure 2.4: Silicon body thickness as manipulated parameter in this project

From the figure 2.4.1, it shows that the source and drain are part of silicon body thickness. If any changes regarding silicon body will affect the source and drain region. As mentioned bulk MOSFET already scaled down the thickness but control of short channel effect is become more difficult and it also leading to increase of sub-threshold leakage current. This happen because source and drain influence over the channel potential become significant relative to the gate control [8].

By using ultra-thin body SOI the scalability of MOS device has been improved well. These due to points in the silicon channel are close enough to have a good control thus eliminating the sub-surface leakage currents. Even though, the SOI MOSFET is allowed the scalability of the thickness, the problem still arises when the thickness is far shrink [8]. Besides that, the impact of scaling down the thickness may lead to negative threshold voltage which is not described for device [10].

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2.5 SOI Scaling Effect

As the devices are scaled down, it is more difficult to achieve a scaled transistor with high performance [19]. Even though they can reduce a short channel effect (SCE), leakage current and maintain good scaling capability. SOI transistor still has its own deficiency as it is being shrinking down to nano scale device [20].

2.5.1 Threshold voltage

Referring the PIDS table of ITRS, it shows that SOI device is attracted considerable attention as potential alternative substrate for low power device application. Since the reduction of size, the power supply is also being reduced accompanied by the threshold voltage reduction. However, the lower limit of the threshold voltage is set by the amount of the off-state leakage current that can be tolerated [12]. As for the future invention, controlling the threshold voltage has become more important.

Several factors are uses to control the threshold voltage one is the channel doping. The channel doping will affect the Fermi potential directly with the channel doping increases. With the channel doping increase different threshold voltage can be achieve by adjusting the channel doping [12]. Gate oxide thickness is one of the factors as in increase the gate oxide capacitance is decrease which means the gate has less control to the channel and threshold voltage increase [12].

As the body thickness is more shrink down the size, it affected the threshold voltage. Threshold voltage is very sensitive to the thickness fluctuation [7] [21]. The main factor is because of the quantum confinement effect whereby the dopant fluctuation can cause the variation in scaled SOI act together with the quantum confinement effect cause larger threshold voltage [11]. Thus, to have the low power device, the low threshold voltage is required [10].

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