ULTRA THIN BODY 18nm SOI N-MOSFET (The Effect of Sidewall Spacer Oxide Thickness to the Device Performance)

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Tajuk Projek : ULTRA THIN BODY 18nm SOI N-MOSFET

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To my beloved family

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ABSTRACT

This research focus on Ultra-Thin Body Silicon On Insulator (UTB SOI) which is fully depleted. The structure is an improvement from the conventional MOSFET which further improve the performance of the device. UTB SOI is much preferred than conventional MOSFET because of thinner body thickness, smaller leakage current and able to improve power consumption. This research project is focus on the design of UTB SOI device which can be scaled down to 18nm with 5.8nm body thickness. The metal gate is used for the gate known as titanium instead of polysillicon gate. It is much more ideal for charging and discharging the gate capacitance of the transistor and resulting in faster operating circuit. Furthermore, the utilization of metal gate is important to get the smallest value of gate resistance near to 0 and able to reduce leakage current. This research also includes the effect of sidewall spacer oxide thickness variation on the UTB SOI performance. Athena and Atlas of Silvaco Simulator have been used to design and simulate in order to obtain the result of MOSFET structure, IV characteristic, the leakage current, the drive current and the sub threshold slope.

ABSTRAK

Kajian ini tertumpu kepada *Ultra Thin Body Silicon On Insulator (UTB SOI)* untuk *Fully Depleted*. Strukturnya adalah penambah-baikan daripada MOSFET konvensional yang memperbaiki lagi prestasi peranti tersebut. *UTB SOI* lebih diutamakan berbanding MOSFET konvensional kerana kenipisan ketebalan badannya, kebocoran arus yang lebih kecil dan mampu untuk meningkatkan penggunaan kuasa. Kajian projek ini fokus kepada reka bentuk *UTB SOI* yang boleh diskala kecilkan sehingga 18nm dengan 5.8nm ketebalan badannya. *Metal gate* yang digunakan sebagai *metal* dikenali sebagai titanium berbanding menggunakan *metal* polisilikon. Ianya lebih sesuai untuk mengecas dan menyahcas *gate capacitance transistor* dan menyebabkan operasi litar yang lebih laju. Tambahan pula, penggunaan *metal gate* sangat penting untuk mendapatkan nilai *gate resistance* yang terkecil yang menghampiri 0 dan mampu mengurangkan kebocoran arus. Kajian ini juga merangkumi kesan variasi ketebalan *sidewall spacer oxide* kepada prestasi *UTB SOI*. Athena dan Atlas (Simulator Silvaco) telah digunakan untuk mereka-bentuk dan mensimulasikannya untuk mendapatkan hasil struktur MOSFET, ciri-ciri IV, kebocoran arus, pemanduan arus dan *sub-threshold slope*.

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ABBREVIATIONS

MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
nm	-	Nanometer
ITRS	-	International Technology Roadmap for Semiconductor
TCAD	-	Technology Computer Aided Design
VLSI	-	Very Large Scale Integrated Circuits
NMOS	-	N-Channel MOSFET
UTB	-	Ultra Thin Body
SOI	-	Silicon On Insulator
SS	-	Sub-threshold Slope
RF	-	Radio Frequency
IC	-	Integrated Circuit

LIST OF SYMBOLS

I_D	-	Drain Current
V_D	-	Drain Voltage
V_{GS}	-	Gate-To-Source Voltage
V_{TH}	-	Threshold Voltage
L_G	-	Gate Length
I_{ON}	-	Drive Current
I_{OFF}	-	Leakage Current
SS	-	Sub-threshold Swing

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CHAPTER I

INTRODUCTION

1.1 INTRODUCTION OF THE PROJECT

Fully Depleted Ultra-Thin Body Silicon On Insulator (FD UTB SOI) able to further improve the performance of the device as compared to conventional MOSFET. MOSFET is actually a type of transistor used for amplifying and switching electronic signals. It is known as the fundamental block in digital logic circuit and FD UTB SOI is one of the examples of MOSFET. It shows an improvement on its performance where it can be proven through the higher switching speed and smaller leakage current. This research was extended to see the impact of different sidewall spacer oxide thickness on the device performance. For this purpose, 3 different thickness has been chosen which are 4nm, 6nm and 8nm. So, Athena and Atlas of Silvaco Simulator have been used to

complete this project in order to obtain the result of MOSFET structure, IV characteristic, the leakage current, the drive current and the sub threshold slope.

1.2 OBJECTIVES

- To design and examine the performance of Ultra Thin Body SOI 18nm N-MOSFET including IV characteristic, the leakage current, the drive current and the sub threshold slope
- To investigate the effects of gate sidewall spacer thickness on UTB SOI performance.

1.3 PROBLEM STATEMENT

- UTB control over short-channel effect which eliminate sub-surface leakage path and extend the scalability of Si CMOS technology
- Sidewall spacer oxide thickness is one of the concerns that affect the performance of the device

1.4 SCOPE OF THE PROJECT

This project is about designing FD UTB SOI through the use of Silvaco software. Under Silvaco software, Athena and Atlas are very important platform in order to obtain the result. Athena is a simulator that provides general capabilities for numerical, physically-based, two dimensional simulation of semiconductor processing. While Atlas is a modular and extensible framework for one, two and three dimensional semiconductor device simulation, it is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. So in order to

complete the simulation, ITRS (International Technology Roadmap for Semiconductor) is used as a guideline and reference to design the Ultra-Thin Body SOI N-MOSFET.

- Working bench on 18nm UTBSOI with 5.8nm body thickness
- Investigating its performance
- Future study will extended to gate sidewall spacer thickness for 3 different thickness

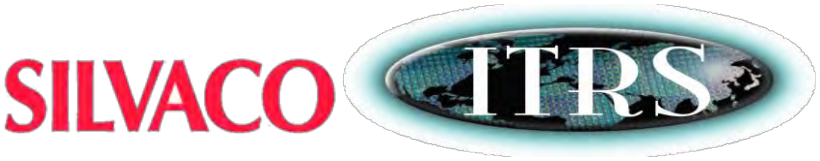

Figure 1.1 : Logo of Silvaco and ITRS

1.5 IMPORTANCE OF PROJECT

- Ultra-thin body (UTB) silicon-on-insulator (SOI) devices have shown great potential for scaling toward channel lengths of 10 nm and below
- UTB provides much promising performance and much flexible than bulk MOSFET
- Can be used in microelectronics industry, high performance RF applications and can be used in photonics
- UTB enable the industries to design much smaller ICs but with complex functions

1.6 PROJECT OUTLINE

In chapter 1, it tells more about the background of the project as well as the purpose of doing this project. It consists of several elements such as introduction, objective, problem statement, scope and importance of the project.

For chapter 2, it is actually to define key terms, definitions and terminology that are related to the topic. This chapter is very useful to identify case studies and existing facts which can be used as supportive evidence of the research.

Chapter 3 is telling more about the project flow from the beginning till the end. In this chapter, it tells the readers about the tools or software that need to be used in order to obtain the desired outcome. As already mentioned before, there are 2 platforms that must be used which known as Athena and Atlas to obtain the results.

In chapter 4, it explains in details the results obtained for different length of Sidewall Spacer Oxide on the device. There are 3 different lengths used which are 4nm, 6nm and 8nm. Based on the results, further analysis must be performed to obtain the hypothesis and conclusion of the project.

Finally, chapter 5 is important to conclude the project based on the obtained results in chapter 4. It is important to know whether this project is successful or not depends on the achievement of objectives stated in chapter 1. Last but not least, several recommendations must be presented to improve the results in the future.

CHAPTER II

LITERATURE REVIEW

2.1 INTRODUCTION

This section describes review of previous studies that are related with this case study in much more detail. The literature review is conducting to understand the concept and also to get some ideas about the overall structure of the project.