VIRTUAL FABRICATION PROCESS OF PLANAR POWER MOSFET USING SILVACO TCAD TOOLS

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FakultiKejuruteraanElektronikdanKejuruteraanKomputer

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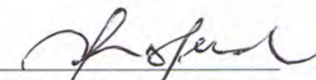

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DECLARATION

This declaration is to clarify that all of the submitted contents of this project are original in its figure, excluding those, which have been admitted specifically in the references. All the work process involves is from my own idea and creativity. All contents of this project have been submitted as a part of partial fulfilment of Bachelor of Electronic Engineering in Computer Engineering.

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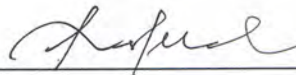

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Special Dedication, to my beloved family members for their love, prayers and encouragement. Also, to my supervisor for her guidance and moral support. Special thanks to all my friends for their support throughout my educational journey.

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ABSTRACT

In this thesis, the structure of planar power MOSFET were designed and developed using Synopsis Silvaco Technology Computer Aided Design (TCAD) tools using several variation of N+ source implant dose, P-Body implant dose, gate oxide thickness and finally the diffuse time of arsenic doping with time. The planar power metal–oxide–semiconductor field-effect transistor (MOSFET) is considered to be ideal power switches due to their high input impedance and fast switching speed. The performance of the planar power MOSFET was analyzed from the Ids vs Vgs curves. The electrical characteristic such threshold voltage, subthreshold swing and current ratio for the proposed device structures were investigated.

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ABSTRAK

MOSFET kuasa berbentuk satah telah dianggap sebagai mempunyai ciri-ciri pensuisan kuasa ideal disebabkan input impedannya yang tinggi dan kelajuan pensuisannya yang tinggi . Dalam tesis ini, struktur MOSFET kuasa berbentuk satah telah direka dan dibangunkan menggunakan Sinopsis Silvaco Reka bentuk bantuan teknologi komputer (TCAD) menggunakan dos implan untuk “N+ Source”, dos implan “P-Body”, ketebalan “Gate Oxide” dan akhirnya “diffuse time” arsenic. Prestasi MOSFET kuasa berbentuk satah telah dianalisis dari menggunakan graph Ids vs Vgs. Ciri-ciri keelektrikan seperti voltan “threshold subthreshold swing“ dan nisbah arus untuk struktur peranti yang dicadangkan itu telah disiasat.

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CHAPTER I

INTRODUCTION

This first chapter provided a basic introduction of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device as the commonly used power devices in the semiconductor industry. Power MOSFET is a new technology in Integrated Circuit (IC) fabrication technology. There are two types of Power MOSFET, trench and planar. One is for low voltage applications while another one is for high voltage applications. Since this research focused on high voltage applications, planar Power MOSFET has been chosen. This chapter started with a basic introduction of the whole chapter on the existing of MOSFET. After that, it stated the brief explanation about the problem statements, objectives, project scope and project significance. Lastly, the thesis organization of this research was stated.

1.1 MOSFET

Nowadays, electronic appliances such as television, computers and mobile phones are getting smaller in size. More applications were added to these appliances due to the growth of technology. Smaller size in electronics appliances need smaller size of transistor. The size of transistor in the market has reached to 32nm and 45nm. To produce a transistor with smaller channel lengths is a challenge, and the difficulties in device fabrication are always a limiting factor in integrated circuit (IC) technology.

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MOSFET are the most commonly used power devices. Power MOSFETs are famous for their superior switching speed, which with further research and designing can make it become "ideal switch". Power MOSFETs does perform the same function as the NPN, bipolar junction transistor (BJT) which is for amplifying and switching applications, and come with additional benefits which is it can handle specific power levels. [1]

The main difference of Power MOSFETs compare to the lateral MOSFETs is the location of the source and drain. In the lateral MOSFETs, the source and drain appear side by side in horizontal but in the power MOSFETs the source and drain area appear in vertical as to withstand the higher voltage applied. The other reason for this is to makes possible lower on states resistances and faster switching than the lateral MOSFETs. The existence of the epitaxial layer is mainly to support the high voltage applied.

In most of Power MOSFETs structure, the N+ source and P-body junction are shorted through source metallization to avoid accidental turn-on of the parasitic bipolar transistor. There are two types of Power MOSFETs which are Planar Power MOSFETs and Trench Power MOSFETs. In planar structure, the poly silicon and the channel are displaced on the horizontal silicon surface of a planar device, same like Trench. For a low-voltage power MOSFET device, a channel conduction is best constructed using a trench channel structure. [1]

1.2 PROBLEM STATEMENTS

This project addresses current issues in high voltage applications. Recently, Bipolar Junction Transistor (BJT) has been used to perform in high voltage applications. The key to the fabrication of a bipolar junction transistor is to make the middle layer, the base, as thin as possible without shorting the outside layers, the emitter and collector. As time passes, technology realized that Bipolar Junction Transistor did not perform well in the high voltage application. Bipolar Junction Transistor consume more power because it is wasting current when it is switch on. Also, the Bipolar Junction Transistor generally has a 0.3v voltage drop in the input pin, and it takes a lot of base current to do that. [1] In order to fulfill the need of high

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voltage devices, many researchers have started looking for a new structure of transistor based on conventional MOSFET. So, Planar Power MOSFET is a better choice.

1.3 OBJECTIVES

The main objective is to design and simulate Power MOSFETs with vertical planar Silvaco TCAD Tools. Other than that, the objectives are:

1. To design the structure of Planar Power MOSFETs using Silvaco TCAD Tool.
2. To analyze the electrical characteristics of Planar Power MOSFETs device.
3. To identify the Planar Power MOSFETs performance in high voltage device.

1.4 PROJECT SCOPE

This project presents the overview on the performance of Power MOSFETS by using computer Silvaco TCAD Tools. The aim of the project was to analyze and identify the device electrical characteristic such as threshold voltage (Vth) and Subthreshold Swing. The study of the device is on designing the structure if Planar Power MOSFET, effect of varying doping dose for source and body implantation, effect of varying time for diffusion method and effect of varying gate oxide thickness.

1.5 PROJECT SIGNIFICANCE

The project brings benefits such as follows:

1. Consume less power so no wasting current occurred during the fabrication process.
2. It fulfill the need of high voltage devices in semiconductor industry.

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1.6 THESIS ORGANIZATION

This thesis is consists of five chapters. The first chapter provides an introduction for this project to the reader. In this chapter, the background and objectives of the project is stated. The problem statements behind the project and scope of study of the project is also discussed within this chapter.

The second chapter is discussing about literature review. This chapter contains the theories related to the project which is mostly about the characteristics of the power MOSFET. The characteristics of the power MOSFET are discussed mostly because it is important to understand it to further study the device.

The third chapter is on the methodology in this project. The chapter explains the flow of this project from the beginning until the acceptable results. It also introduces the ATHENA software and ATLAS software.

The fourth chapter is focusing on the collected and analyzed data in this project. The simulation results were discussed in this chapter. The electrical characteristics were extracted, compared and analyzed.

Finally, the fifth chapter describes the conclusion and the some recommendations for the future work. It also determines the achievements of this project.

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CHAPTER II

LITERATURE REVIEW

This chapter provides and overview of relevant literature as well as the basic theoretical concept of the fabrication process of Planar Power MOSFET and how this device functioning. It explains the theory of Power MOSFET basic and the review.

2.1 INTRODUCTION

Power MOSFETs have become the standard choice as the main switching device for low-voltage switch mode power-supply (SPMS) converter applications. The standard value for low voltage SMPS is <200V. However, to size the right device for a specific topology using manufacturer's datasheets is becoming increasingly difficult. With a large variety of topologies, switching speeds, load currents and output voltages available, it has become impossible to identify a generic MOSFET that offers the best performance across the wide range of circuit conditions. [2] Low-voltage power MOSFETs are widely used in portable electronics for dc/dc conversion applications. As the operating voltage of portable electronics is reduced, the drain and threshold voltages of power MOSFETs have to be reduced as well.

A figure of merit to evaluate the switching performance of power MOSFETs is defined as the product of the specific on-resistance (*R*ON · AA) and the gate–drain charge density (*Q*GD/AA). [3] The planar and trench power MOSFETs are two vertical power transistors commonly used in low-voltage power switching applications. The planar power MOSFET is easier to be fabricated than the trench power MOSFET because the critical trench process is not required. When compared

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to the trench power MOSFET, the planar power MOSFET usually has a smaller gate–drain charge density but a higher specific on-resistance. In recent years, a number of approaches have been reported to improve the performance of the low-voltage planar power MOSFET. A split gate together with a dummy gate shorted to the source is employed to reduce the gate–drain overlap area and to protect the ends of the split gate from electric field crowding [4]

Until the 80's, Bipolar Junction Transistor (BJT) was the main technology used for Power IC's. The BJT was the best transistor because of its "amplification and matching properties". As time passed by, the high demand for gate logic led to the need for a better switching technology. The BJT then became outdated because of its power consumption needs and complex design. At low frequencies, CMOS was the apparent choice for gate logic design. Power Integrated Circuit (IC) was expanded to include BJT and CMOS technology. BJT has reached a limit in delivering power to the load. [5]

2.2 THE POWER PLANAR MOSFET STRUCTURE

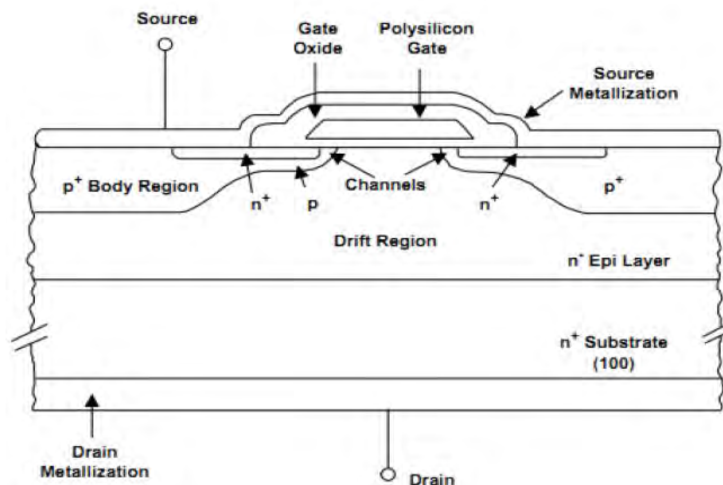

Figure 1.0 Planar Structure of Power MOSFET [4]

In most power MOSFETs, the N^{+} source and P-body junction are shorted through source metallization. This is to avoid accidental turn-on of the parasitic bipolar

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transistor. When no bias is applied to the Gate, the Power MOSFET is capable of supporting a high drain voltage (V_d) through the reverse-biased P-body and N^- Epi junction.

In high voltage devices, most of the applied voltage is supported by the lightly doped Epi layer. A thicker and more lightly doped Epi supports higher breakdown voltage but with increased on resistance. In lower voltage devices, the P-body doping becomes comparable to the N^- Epi layer and supports part of the applied voltage. If the P-body is not designed thick or heavy enough, the depletion region can punch-through to the N^+ source region and cause lower breakdown. But if it is over designed, the channel resistance and threshold voltage will also increase. [6]

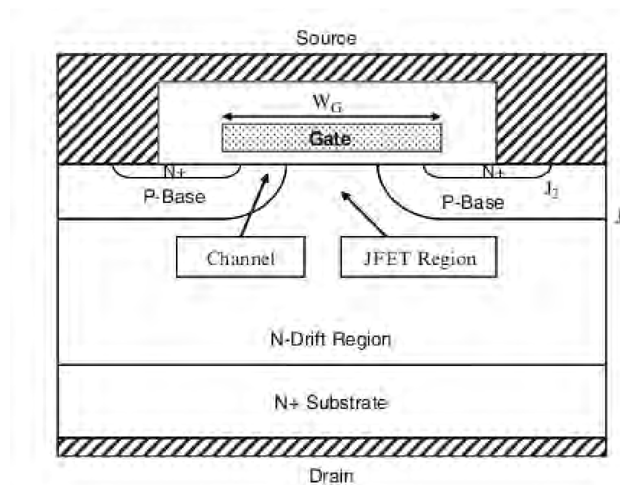

Figure 1.1 Another representation of Power MOSFET [6] ref

2.2.1 Lateral Channel Design

1. **VMOSFET Design**
   This was the first design to be commercialized. The design has a V-groove at the gate region. VMOSFETs then were replaced by DMOSFET due to stability problem in manufacturing and a high electric field at the tip of the V-groove.
2. **DMOSFET Design**
   This design is the most commercially successful design because it has a double-diffusion structure with a P-base region and a N+ source region.

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3. **UMOSFET Design**

The higher channel density in UMOSFETs reduces the on-resistance as compared to the VMOSFETs and the DMOSFETs. This design consists of U-groove at the gate region. UMOSFET designs with the trench etching process were commercialized in the 90's. [7]

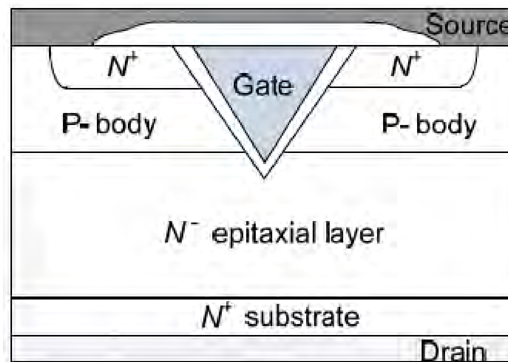

Figure 1.2.1 VMOSFET Vertical

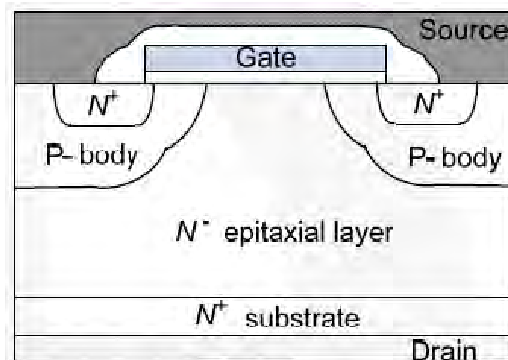

Figure 1.2.2 DMOSFET Vertical

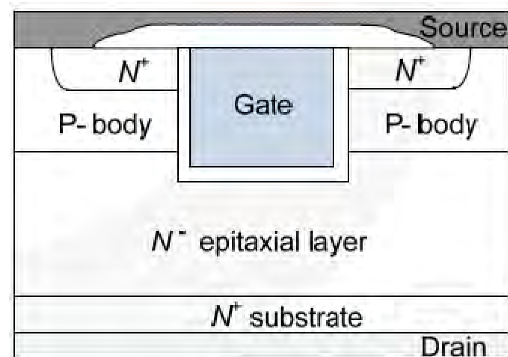

Figure 1.2.3 UMOSFET Vertical

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The drain, gate, and source terminals are placed on the surface of a silicon wafer. This is suitable for integration, but not for obtaining high power ratings because the distance between source and drain must be large to obtain better voltage blocking capability. The drain-to-source current is inversely proportional to the length. [7]

2.2.2 Trench and Planar MOSFET Structure

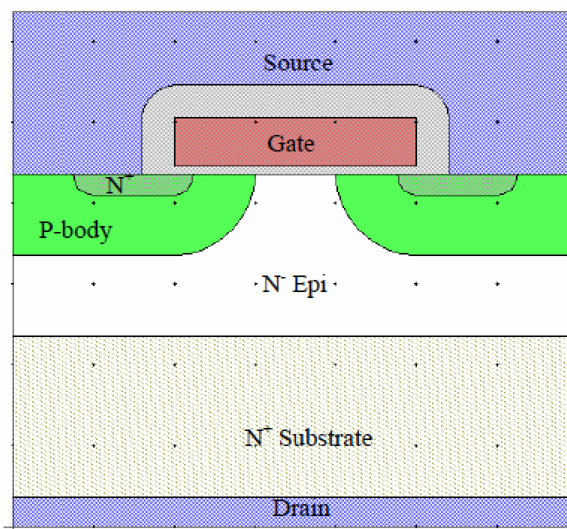

Figure 1.3 Planar MOSFET Structure [6]

Planar gate structure takes advantage of its vertical current flow between the source and drain electrodes placed at the front and back side of silicon die. Current flows under the planar gate, then turns down between the P-body regions and flows under the planar gate and flows vertically through the epitaxial layer to the substrate. The lightly doped epitaxial layer easily supports high breakdown voltage. Vertical current flow allows large current densities to be handled as opposed to the difficulties in scaling up the area of MOSFET's with lateral layout. [8]

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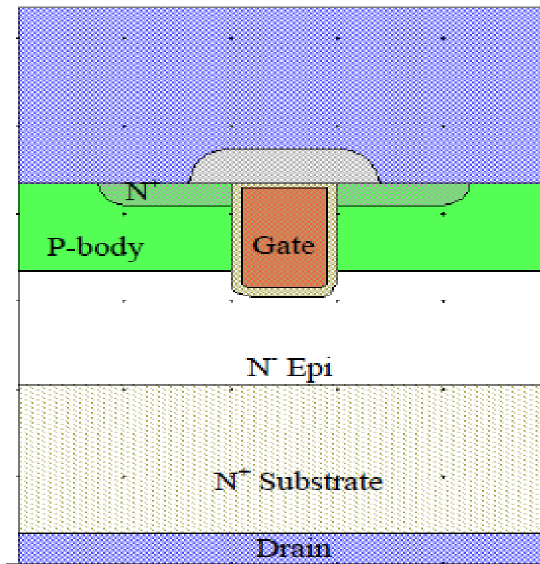

Figure 1.4 Trench MOSFET Structure [6]

In a Trench structure, the MOS channels are designed along the vertical walls of the trenches. This allows for a high density of channels per silicon unit. By removing the JFET structure, the cell pitch can be made small, reducing the specific RDSON. The large trench wall area leads to a large value of built-in capacitors. When the trench bottom overlaps the epitaxial layer, which is part of the drain terminal, it creates a large capaci tance from gate-to-drain (CGD). This is a major drawback, especially if a high switching speed is required. [8]

2.3 BREAKDOWN VOLTAGE

Breakdown voltage (BVDSS), is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. BVDSS is normally measured at 250mA drain current. For drain voltages below BVDSS and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift p-n junction.

Two related phenomena can occur in poorly designed and processed devices which are punch-through and reach-through. Punch through is observed when the depletion region on the source side of the body-drift p-n junction reaches the source

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