DESIGN AND ANALYSIS OF A LOW POWER OPERATIONAL AMPLIFIER USING CADENCE

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This report is submitted in partial fulfillment of requirements for the bachelor degree of electronic engineering (computer engineering)

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Universiti Teknikal Malaysia Melaka

JUNE 2014

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Dedicated to my beloved family especially my father, lecturer and to all my beloved friends.

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ACKNOWLEDGEMENT

Alhamdullilah, thanks to Allah for giving me chance to complete my final year project. Firstly I would like to express my gratitude towards people who always supported me and believed in me. I am very thankful to my project supervisor Engr. Muhammad Idzdihar for giving me the opportunity to work under him and giving every support at every stage of this project work. I truly appreciate and value all his guidance and encouragement from the beginning to the end of this thesis.

I also want to express my thankful to my friend Norzayani who always guide and help me when I face difficulty during finishing my project. I would also like to thank my project panel Ms. Hashimah and Mdm. Syafeeza for their useful comment regarding on my project. It really helps me a lot on improving my project and also for my future career. Special thanks to my classmate friend Muhammad Hazari for his help and support during completing my writing thesis.

Finally, I wish to thank to my lovely father and my siblings whom always pray the best for me.

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ABSTRACT

In this paper a low power operational amplifier consisted of two stages and operates at 1.8V power supply is design by using 130nm technology. It is designed to meet a set of provided specification. Designers are able to work at low input bias current and also at low voltage due to the unique behavior of the MOS transistors in sub-threshold region. The design of two-stage operational amplifier provides a gain of 69.73dB and a 28.406MHz of gain bandwidth product for a load of 2pF capacitor. It has CMRR of 62.93dB and output slew rate of 20V/μs. The two-stage op-amp has a PSRR+ of 99.76 dB and PSRR- of 90.91dB. The presented op-amp has an Input Common Mode Range (ICMR) of 0.8V to 1.6V and power consumption of 0.389mW. This two-stage op-amp is design using the Silterra 130nm technology library. The layout has been draw and its area had been calculated. The proposed two stage op-amp consist of NMOS current mirror as bias circuit, differential amplifier as the first stage and common source amplifier as the second stage. The first stage of an op-amp contributed high gain while the second stage contributes a moderate gain.

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ABSTRAK

Dalam laporan ini penguat kuasa operasi yang rendah dibentangkan dimana skematiknya terdiri daripada dua peringkat dan beroperasi pada 1.8V bekalan kuasa dengan menggunakan teknologi 130nm . Ia direka untuk memenuhi satu set spesifikasi yang disediakan. Pereka mampu untuk bekerja di rendah input berat sebelah semasa dan juga pada voltan rendah kerana tingkah laku transistor MOS yang unik di rantau sub-ambang. Reka bentuk dua peringkat penguat operasi menyediakan peningkatan sebanyak 69.73dB dan 28.406MHz peningkatan jalurlebar produk bagi beban 2pF kapasitor. Ia mempunyai CMRR degan nilai 62.93dB dan slew rate 20V/μs . Kedua-dua peringkat penguat kuasa mempunyai PSRR+ dengan nilai 99.76 dB dan PSRR – dengan nilai 90.91dB . Penguat kuasa yang dibentangkan ini juga mempunyai Input biasa Mod Range (ICMR) dari nilai 0.8V sehingg 1.6V dengan penggunaan kuasa 0.389mW. Dua peringkat penguat kuasa ini telah direka bentuk dengan menggunakan Silterra perpustakaan teknologi 130nm . Susun atur ini telah direka bentuk dan luas kawasannya telah dikira. Dua peringkat penguat kuasa yang di gunakan ini terdiri daripada NMOS arus semasa sebagai litar berat sebelah , penguat kebezaan sebagai peringkat pertama dan sumber penguat biasa sebagai peringkat kedua. Peringkat pertama penguat kuasa selalunya menyumbang peningkatan yang tinggi manakala peringkat kedua menyumbang peningkatan yang sederhana.

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LIST OF ABBREVIATIONS

Op-Amp	–	Operational Amplifier
PM	–	Phase Margin
CMRR	–	Common Mode Rejection Ration
PSRR	–	Power Supply Rejection Ration
ICMR	–	Input Common Mode Range
DC	–	Direct Current
AC	–	Alternating Current
VCM	–	Voltage Common Mode

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CHAPTER I

INTRODUCTION

1.1 Background

The operational amplifier (op-amp) is a core part in designing an analog electronic circuitry and mixed signal systems[1][2]. There are various levels of complexities when designing an operational amplifier and thus make it a versatile device that ranging from a dc bias generation to a high speed amplifications to filtering[3][4][5]. Operational amplifier is widely used in electronic devices today as it being used in industrial, scientific devices and in a vast array of consumer.

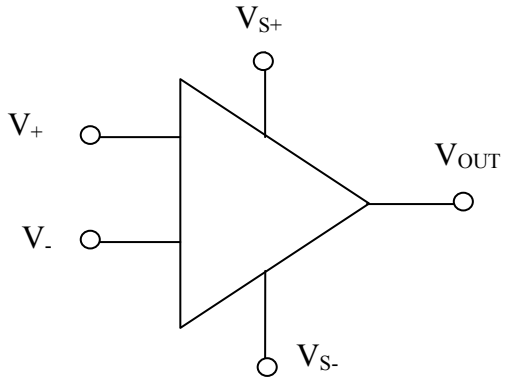

Figure 1-1 Symbol of Op-Amp

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Op-amps is said to be a linear devices as it has nearly all the properties required for not only ideal DC amplification but also widely used for signal conditioning, filtering and performing mathematical operations such as additional, subtraction, differentiation, integration etc[5][4]. A general operational amplifier consist of 3 terminal devices which two of it are inverting input represent by a negative sign ("-") and non-inverting input represent by a positive sign ("+") and both of its have a very high input impedance. The third terminal of an operational amplifier is output port where it can both sinking and sourcing either a voltage or a current. The difference between the two signals being applied to the two inputs of an operational amplifier is called the amplified output signal. Due to this, a differential amplifier is generally used as the input stage of an operational amplifier and hence an operational amplifier is also called a DC-coupled high-gain electronic voltage amplifier. Block diagram of an operational amplifier is described in figure 1-2 where differential input amplifier is a first stage with two input voltage and common source stage as the second stage.

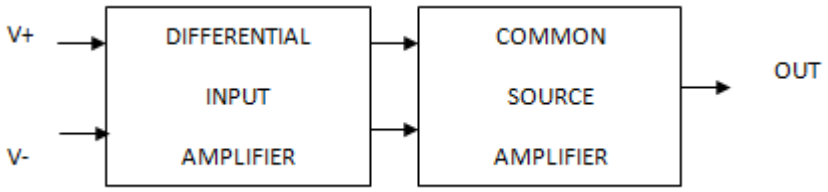

Figure 1-2 Block Diagram of Two Stage Op-Amp

1.2 Op-Amps Applications

It is difficult to describe all of op-amps application as op-amps itself are used in many applications. In this chapter, only some simple but widely used applications of op-amps will be explained which are:

1) Differential Amplifier: The differential amplifier have two inputs, so this two input wil produces the algebraic difference as shown in figure 1-3. As RA=RB

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and RF=Rin, the output of differential amplifier can be given as $Vo = \frac{RA}{RF}(V_A - V_B)$. This connection will amplifies the differences of this two voltages by a constant gain set by the used resistances[5].

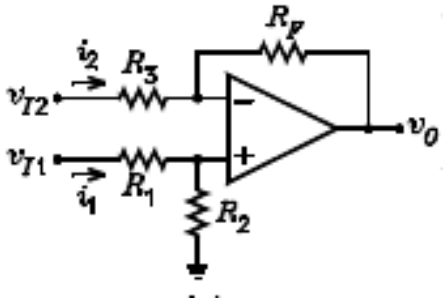

Figure 1-3 Differential Amplifier [6]

2) Summing Amplifier (Adder): This type of amplifier is handy circuit where it's enabling to add several signals together. From figure 1-4, by keeping the negative terminal approximate to 0V or close to ground, the op-amp will essentially nails one leg of R1, R2 and R3 to a 0V potential and thus makes it easier to write the current in these R1,R2 and R3 resistors.

$$I_1 = \frac{V_1}{R_1};\quad I_2 = \frac{V_2}{R_2};\quad I_3 = \frac{V_3}{R_3} \qquad \text{.....(1)}$$

Based on Kirchhoff's law, the total current, $I_t = I_1 + I_2 + I_3$ and

$$V_O = -R_F\left(\frac{V_1}{R_2} + \frac{V_2}{R2} + \frac{V_3}{R_3}\right) \qquad \text{.....(2)}$$

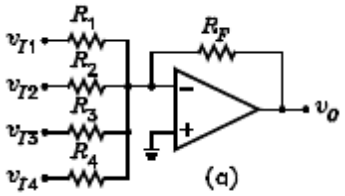

Figure 1-4 Summing circuit[6]

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1.3 Low Power of Operational Amplifier

A low power operational amplifier gives advantages in many applications as it prolonging the battery life and thus making it suitable for portable devices. In analog devices product development, it offers in term of power efficient without compromising in term of speed, noise and precision. Low power op-amp is widely used as a bio-potential amplifier where it is used to amplify and filter extremely weak bio-potential signals[7]. In industry it is widely used in the usage of barcode scanner.

1.4 Problem Statement

Nowadays, the need on smaller size chip with very small power dissipation had increase the demand on low power design. But the obstacles on designing a good performance of a low power op-amp are on operating with power supplies that is smaller than 1 Volt, on getting an ideal characteristic of op-amp specification and on designing a circuit with the same or better performance than circuits designed for a larger power supply.

1.5 Objectives

The objectives of this project are:

i. To design a low power of operational amplifier and implement it using 130nm CMOS process technology
ii. To simulate and analyze the performance of the proposed design

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1.6 Scope of Work

This project scope focus on designing a low power of operational amplifier using Cadence tool, to simulate and analyze the operational amplifier schematic design and to draw the layout of the schematic

1.7 Thesis Organization

This thesis comprises five chapters: Introduction, Literature Review, Project Methodology, Result and Discussion, and Conclusion and Recommendation. The introduction of the project in Chapter 1 will explains the background of the project before move on to the details of the thesis. Chapter 2, the Literature review, reviews the theory on each stage of the design op-amp, and existing work, also several other topics related to the project. Chapter 3 discusses the methodology of the overall project from beginning till the end of the project. The results and discussion are explained in further details in Chapter 4. Finally, the thesis ends with Chapter 5 which concludes the overall project followed by some recommendation for future work.

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CHAPTER II

LITERATURE REVIEW

2.1 Current Mirror

The current mirror is one of the most basic circuits which commonly used in linear IC design and it is made by using active devices and used as biasing elements and also as load devices in the amplifier stages. It is a circuit block functions to produce a copy of the current in one active devices the replicated the current in second active devices. Current mirror is a relatively high in output resistance that helps to keep the input current constant regardless of drive conditions.

Practically, an ideal current mirror is considered as an ideal current amplifier. There are three main specifications of current mirror characterization. One of it is the current level it produces. Second is the AC output resistance and it determines how much the output current varies with the voltage applied to the mirror. The last specification is the minimum voltage across the output current mirror terminal that needs to be maintained in order for it to work properly. This minimum voltage will also keep the output transistor of the mirror is in active mode.

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For an ideal current mirror, the output current produce is a product of the input current and a desired voltage gain. The input current is reflected to the output due to a unity gain. This ideal current mirror gain must be independent of input current frequency while the output current must be independent to the voltage at the output node. For instance neither is the gain independent of the input frequency nor does the current mirror output current stays independent of voltage variations at the output node[5].

2.1.1 Basic Current Mirror

Figure 2.1 below show the basic current mirror implemented using MOSFET transistor. M1 and M2 transistor in the figure 2-1 is assume operating in saturation or active mode. The output current I_{OUT} is directly related $I_{REF.}$

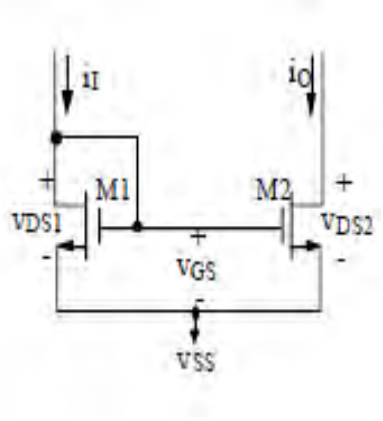

Figure 2-1 Basic Current Mirror[8]

The function for both the gate-source voltage (V_{GS}) and the drain-to-gate voltage (V_{DS}) is the drain current of a MOSFET, I_D and is given by I_D=f (V_{GS}, V_{DG}). This relationship is derived from the functionality of the MOSFET device. The drain-to-source voltage is expressed as:

$$V_{DS} = V_{DG} + V_{GS} \quad \text{..... (3)}$$

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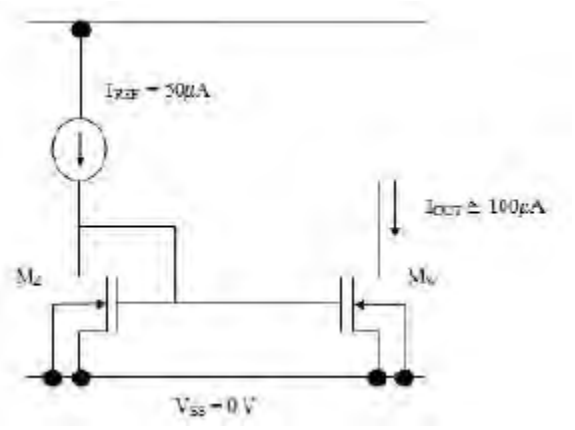

Figure 2-2 NMOS Current Mirror[9]

Figure 2-2 shows the NMOS Current Mirror circuit where this two MOSFET have the same V_{GS} since their gates are shorted and both of their sources are connected to V_{SS} or ground terminal.

The MOSFET current mirror with the usage of R_{REF} as shown in figure 2-3 below is for NMOS. From this figure, M2 will acts as a current sink since it pull the current $I_O=I_{D2}$ from the load which in this case it will be the amplifier of the op-amp.

Figure 2-3 MOSFET Current Mirror Using Resistor R_{ref} [5]

For PMOS current mirror in figure 2-4, the PMOS source is connected to the V_{DD} and Q2 acts as a current source since it pushes current $I_O=I_{D2}$ into the load

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