OPTIMIZATION OF POWER AND GAIN IN MOSFET MULTI-STAGE OPERATIONAL AMPLIFIER USING TAGUCHI'S APPROACH

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"Saya akui laporan ini adalah hasil kerja saya sendiri kecuali ringkasan dan petikan yang tiap-tiap satunya telah saya jelaskan sumbernya ."

Tandatangan : ……..

Nama penulis : NURHAZWANI BT HASHIM

Tarikh : 2014

"Saya/kami akui bahawa saya telah membaca karya ini pada pandangan saya/kami karya ini adalah memadai dari skop dan kualiti untuk tujuan penganugerahan Ijazah Sarjana Muda Kejuruteraan Elektronik (Electronik Industri)."

Tandatangan : ……...
Nama Penyelia : ENGR. HAZLI RAFIS BIN ABDUL RAHIM
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DEDICATION

Special for the beloved parents and siblings who have a lot of support in order to complete this study may all appreciate the sacrifice you are rewarded by Allah SWT.

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"In the name of Allah, the most Gracious, most Powerful, and the most Merciful"

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ABSTRACT

The title for this project is about optimization of power and gain in MOSFET muti-stage operational amplifier using Taguchi's approach. Operational amplifier (op-amp) has a high gain value and widely used in all types of electronic gadget nowadays. It is a fundamental building block for many electronic analog circuits. Although the op -amp itself composed of various types of MOSFETs, it is usually considered as one of the ideal circuit. Designing high-performance analog circuits is becoming increasingly challenging with the insistent trend toward reduced supply voltages. The sophisticated of today's CMOS technology resulted in the various design of op-amp circuits to obtain optimum power and gain. By down scaling the size of the MOSFET channel length (L), the transition frequency increases (more speed) and at the same time the gain and power are optimized. Therefore, the Multi-stage op-amp was tested with different CMOS technologies of 0.13μm and 0.18μm with Cadence software to compare the performances in terms of power and gain. The best performances will be applied in Taguchi method to get the actual value of power and gain. From the simulation, the results shown both power and gain are increase from the original value.

ABSTRAK

Tajuk bagi projek ini ialah pengoptimuman *power* dan *gain* dalam penguat operasional *Multi-stage* menggunakan kaedah Taguchi. Penguat operasional (op-amp) mempunyai nilai *gain* yang tinggi dan kebayakkannya digunakan dalam semua jenis alatan-alatan electronic pada masa kini. Ianya merupakan komponen asas dalam semua litar analog elektronik. Walaupun op-amp itu sendiri terdiri daripada pelbagai jenis mosfet, ia biasanya di kira sebagai satu litar yang ideal. Kecanggihan teknologi CMOS pada hari ini menyebabkan reka bentuk litar op-amp juga diubah untuk mendapatkan *power* dan *gain* yang optimum. Melalui pengurangan saiz panjang saluran mosfet, kadar peralihan frekuensi akan bertambah dan pada masa yang sama *power* dan *gain* dapat di optimumkan. Oleh itu, *Multi-stage* op-amp di uji dengan teknologi CMOS yang berlainan iaitu 0.13 µm, 0.18 µm dan 0.2 µm melalui perisian Cadence untuk melihat perbezaan *power* dan *gain* di antara satu sama lain. Nilai *power* dan *gain* yang paling terbaik akan diaplikasikan menggunakan kaedah Taguchi untuk mengetahui nilai yang sebenar. Daripada hasil kajian tersebut, masing-masing *power* dan *gain* dapat dioptimumkan jauh lebih baik daripada nilai yang asal.

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CHAPTER 1

INTRODUCTION

Chapter 1 covers about the introduction part of this Final Year Project of Degree. It contains subchapter of objectives, problem statements, scopes of project and project significance.

1.1 Introduction of Project

Recently everyone is familiar with the electronic devices, whether it is radio, television, mobile phones or computers. However, most people have no knowledge of what goes inside these devices and that is the way they like. Fortunately for them, there are others who are more curious. Electronic devices generally have even thousands of components. One of them is operational amplifier; which is one type of amplifier.

The common IC operational amplifier is one which has very high gain and finds widespread use in many electronics. Its application is not limited to linear amplification system, but includes digital logic system as well. A common IC takes the form of an operational-amplifier (op-amp) which provides various choices in its applications e.g. the input can be either or non-inverting.

Similarly, op-amp can be used as differential amplifiers in which the output signal is proportional to the difference of two input signals. It is quite usual that a single amplifier cannot provide the gain which we desire. We therefore use two or more cascode amplifier.

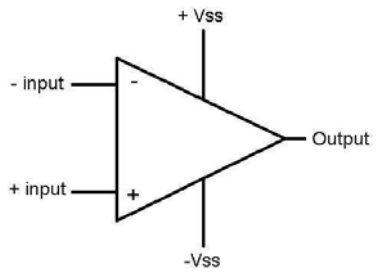

Figure 1.1 Operational amplifier

1.12 Basic op-amp

There are several of op-amp exist in basic literature, each having the positive and negative aspects in terms of performances. Below are few types of op-amp:

I. Telescopic amplifier
II. Folded cascode amplifier
III. Two stage amplifier

Some topologies have a very high gain but less swing and speed, some have high speed but the gain is very low and others are combination of more than one basic topology [1].

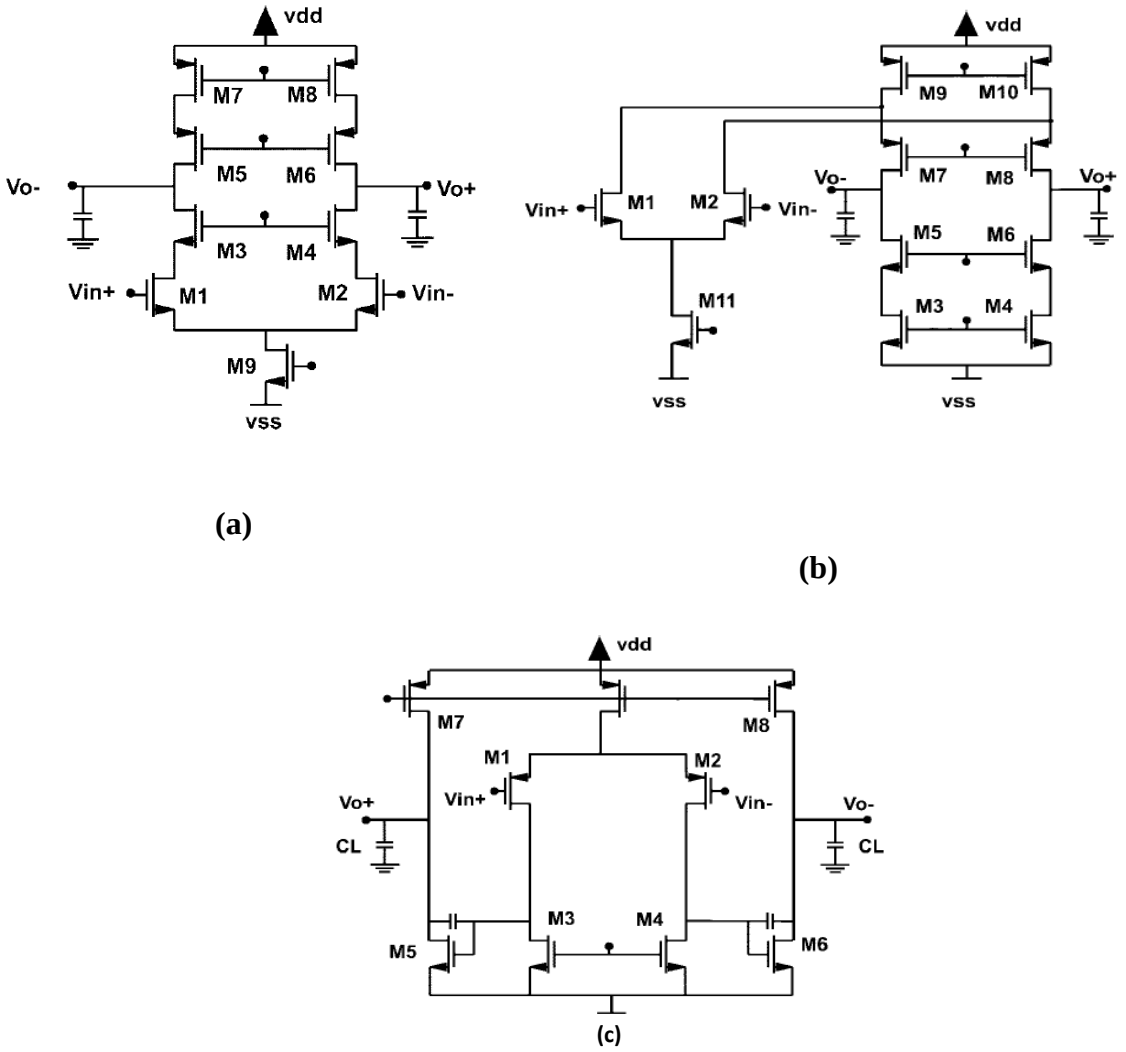

Figure 1.2 Conventional op-amp topologies (a) Telescopic amplifier (b) Folded-cascade amplifier (c) Two-stage amplifier

A. Telescopic amplifier

It is simply similar to differential amplifier but typically has higher frequency and consumes less power than other topologies. It is extension of differential amplifier where input and load are replaced by cascode pairs so as to increases the gain of the output given as:

$$A_v = g_{m1}\,[(g_{m3}.r_{o3}.r_{o1}) || (g_{m5}.r_{o5}.r_{o7})]$$

Even it has high gain, this amplifier is not used due to its small voltage swing which is controlled by the overdrive voltage of cascode.

B. Folded cascode amplifier

It is used quite widely compare to telescopic topologies, because of the input and outputs can be shorted together and the choice of the input common-mode level is easier. This amplifier is used to increase the output swing by folds the input transistor to either to V_{dd} or ground and two tail current sources. The gain is:

$$A_v = g_{m1} \{[(g_{m3}.r_{o3}.(r_{o1} || r_{o5})] || [g_{m7}.r_{o7}.r_{o9}]\}$$

C. Two-stage amplifier

A single stage has low frequency gain which is $A_v = g_{m1} (r_{o1} || r_{o3})$ compare to two-stage amplifier. It can gives good gain but lesser in swing output. Hence, the two-stage can be designed in such that the gain and swing are independent. At the first stage, it can provide a high gain whereas at second stage it can gives a high swing and each can be controlled independently.

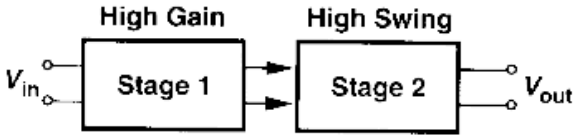

Figure 1.3 Block Diagram

A_v, first stage = $g_{m1,2}(r_{o1,2} || r_{o3,4})$

$A_{v,}$ second stage = $g_{m5,6}(r_{o5,6} || r_{o7,8})$

Overall gain $A_v = A_v$, first stage × A_v, second stage

Technology in manufacture of op-amp is rapidly increased with smaller and smart technology. This technology produced to make life easier, faster and secure to be used in daily life environment. Due to this phenomenon and global desire, it needs to

provide higher caliber of quality in products and accommodations for incrementing market continue competitively among the manufacturers to ascertain customer gratification. Optimization is needed as it result in better performances and reducing cost. After all, optimizing the parameters has become mandatory now a day in operational amplifier design.

There are a lot of methods have been developed to optimize parameters in a circuit to achieve high gain and low power such as

I. Geometric Programming
II. Gain-Boosted Op-Amp (GBO)
III. Taguchi Method

The feature of geometric programs introduced new method for determining components values an transistor dimensions for CMOS op-amp. It can be used to synthesize robust design that is design guaranteed to meet the specifications for a variety of process conditions and parameters. [2]

The methodology of gain-boosted op-amp (GBO) allows the optimization in terms of ac response and settling performance and is incorporated into an automatic computer-aided design (CAD) tool, called GBOPCAD. [3]

Taguchi method is based on statistical approach and it will be used to optimize selected parameters such as W/L ratio of transistors, chopping frequency, size of chopper modulator and bias current to achieve low noise and low offset. [4]

The concept of this method is towards the quality and reliability in the design stage, which is prior to manufacturing. Typically, it is a prototyping technique that enables engineers and designers to produce a robust design in order to deliver the functionality needs by the customer.

1.2 Objective of Project

The main objective of this study is to optimize power and gain in MOSFET multi-stage op-amp. This objective is supported by the following sub objectives:

I. To design new multi-stage op-amp
II. To investigate the performances of Multistage using CMOS 0.13 µm, 0.18 µm and 0.2 µm technology.
III. To apply Taguchi method on the best CMOS technology

1.3 Problem Statement

Designing high-performance analog circuits is crucially important and challenging with the insistent trend toward reduced supply voltages. Operational amplifier is used in this project due to it offers good voltage gain, good common mode range and good output swings. Nevertheless, there are few problems arise within those topologies, some have a very high gain but less speed and swing, some have good speed but the gain is imbalance. From the background research, two-stage operational amplifier gives the better output compare to others topologies because gain and swing can be control independently.

In order to achieve high gain and low power, a lot of methods have been introduced such as geometric programming and gain-boosted op-amp. However, these methods require systematic and precise parameters. Therefore, easier method that not require systematic design is proposed known as Taguchi method. Therefore, the research done on the two-stage operational amplifier using the Taguchi's approach.

1.4 Scope of Project

The scope of this study had been identified. The problem characteristics will be on;

I. The investigation of two stage op-amp using the Taguchi approach.

II. Redesign and simulate the circuit by using the Cadence software and until the schematic result with layout.

III. Analyze the performance of op-amp based on CMOS technology

1.4.1 Software Design

This project focuses on the redesign circuit using Cadence software. It is an essential role in the creation of today's electronics such as software, hardware and expertise to verify today's mobile. In short it is tools for designing full-custom integrated circuits of operational amplifier.

1.4.2 Target User

Target users who will be using this in future is IC manufactures and the industries for optimizing the cost of manufacture at the same time produce more high quality of devices so that the user will satisfy and no concerns after using that devices.

1.5 Project Significance

The optimization of power and gain will improve the modeling accuracy for sub-micron technologies especially in operational amplifier. Hence, the new modeling design of multi stage op-amp will optimize power and gain such as in signal processing circuit and instrumentation. As for Taguchi method, it is an efficient problem solving tools which can improve the performance of the product, process design, and system with the experimental time and cost.

1.5 Report Structure

The report consists of five chapters which is Chapter 1 will discusses about the introduction of the project which includes the objectives of the project, problem statements, scope of the project, project significance and report structure. The problem statement describes the problem that faced by the performance of each topologies and follow by the discussion of the scope and significance of the project.

Chapter 2 is discussed about Literature review. The first part is about the importance of optimization in power and gain in each device. Then, analyze the effect of redesign two-stage operational amplifier and the process involving Taguchi method.

The next chapter, chapter 3 discusses about Project Methodology of the project. The methodology involved system analysis, system design, and system testing.

Then, chapter 4 discusses about Result and Discussion of the project. It is about result full decision after the completion of this project.

The final chapter is chapter 5 that explains about conclusion and recommendation for future work related to this project.

CHAPTER 2

LITERATURE REVIEW

This chapter presents an overview of the previous works on the related topic for providing the background of this study.

2.1 Overview of two-stage operational amplifier

Two stage op-amp consists of a cascade of V to I and I to V stages [5]. It is divided into two parts; first stage and two stage as shown in Figure 2.1. The first stage consists of a differential amplifier which is convert the differential input voltages to differential currents. These differential currents are applied to a current-mirror load by replacing the differential voltage [7]. This is known as differential voltage amplifier. The second stage consists of a common-source MOSFET that convert the second stage input voltage to current known as current-sink inverter. This two stage op-amp is so widely used in current technology

Based on Figure 2.1, M5 provides biasing for the entire operational amplifier. The input of the first gain stage is triggered by M1 and M2 forming a differential pair input. The M5 and M7 supplies the differential pair with bias current IB_1. The input differential pair is actively loaded with the current mirror formed by M3 and M4.

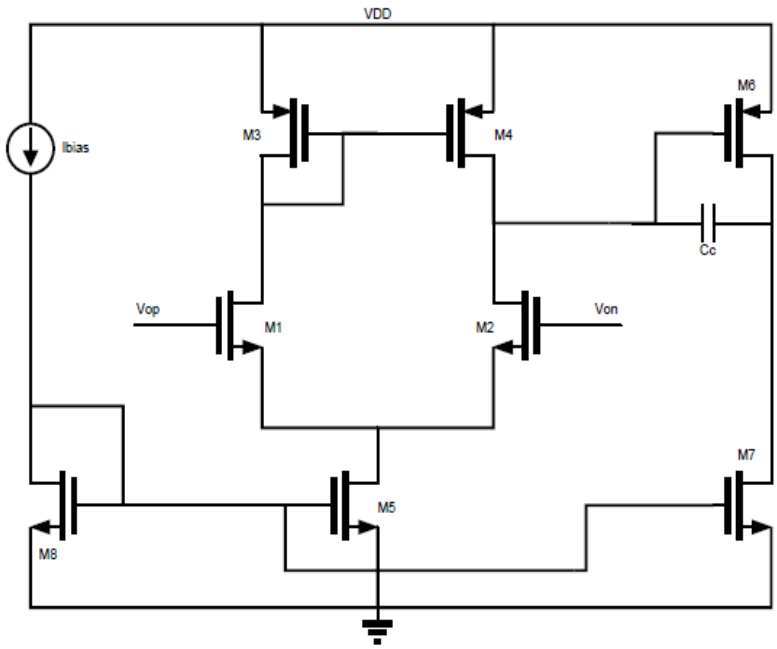

Figure 2.1 Two-stage op-amp

Node 1 forms the output of the first stage of the op amp. The second stage consists of M6 which is a common-source amplifier actively loaded with the transistor M7. The transistor M7 does not provide biasing for M6, instead M6 is biased from the gate side. The capacitor CC known as Miller compensation is to increase the phase margin of the system [6]. The design parameters of the two stage op-amp are discussed below:

I. The minimum value for the tail current (I_5) from the largest of the two values is determined.

$I_5 = SR.C_c$

I_5 is nearly equal to $\frac{10(V_{DD} + |V_{SS}|)}{2T_S}$