BOOTH'S ALGORITHM DESIGN USING FIELD PROGRAMMABLE GATE ARRAY

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Tajuk Projek : **BOOTH'S ALGORITHM DESIGN USING FIELD PROGRAMMABLE GATE ARRAY**

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Signature	:
Supervisor	: Mr Anuar Bin Jaafar
Date	: 2 June 2014

To my beloved family, my project Supervisor Mr Anuar Bin Jaafar, all the lecturers that involve in my project, my friend and also to all my classmate that has been participated in this report session and the report project.

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ABSTRACT

Nowadays, digital device is very important to all people in this world. The high speed operation and less space and energy required had made the digital devices more preferred. This project is to design digital system which performed fixed point Booth Multiplier Algorithm where the design system would be developed using hardware description language (HDL), in this case, VHDL (VHSIC Hardware Description Language), VHSIC stands for Very High Speed Integrated Circuit. In this project would be used Xilinx ISE 10.1which is the software used to designed digital system for Xilinx manufactured FPGA board. In Xilinx have two main languages which are VHDL and Verilog. For design Booth"s Multiplier Algorithm we used Verilog code which is have to create the program module and testbench. In that case, to design digital system will have input and output which is input is 8 bits and output is 16 bits. Finally, it is proven that the system created can calculate and yield a fixed point multiplied output of the input value.

ABSTRAK

Pada masa kini, alat teknologi digital sangat penting kepada masyarakat di seluruh dunia. Operasi berkelajuan tinggi dengan ruang yang kecil serta tenaga yang sedikit membuatkan teknologi digital ini lebih dikenali dan digemari ramai. Projek ini adalah untuk merekabentuk alat digital yang berfungsi sebagai integer Pendaraban Booth di mana sistem digital tersebut akan dihasilkan menggunakan bahasa penggambaran perkakasan (HDL), di dalam kes ini , VHDL (VHSIC bahasa penggambaran perkakasan), VHSIC bermaksud litar integrasi berkelajuan tinggi. Pengatur cara komputer yang digunakan adalah Xilinx ISE 10.1 dimana pengatur cara komputer tersebut digunakan untuk merekabentuk sistem digital untuk Xilinx menggunakan litar FPGA. Perisian Xilinx dapat digunakan dalam dua jenis bahasa pengatucaraan iaitu VHDL dan bahasa Verilog. Untuk merekabentuk Pendaraban Booth menggunakan bahasa Verilog yang digunakan untuk merekabentuk modul dan modul penguji. Projek ini menggunakan dua jenis masukan 8 bit yang menghasilkan keluaran 16 bit dengan mengaplikasikan Algoritma Pendaraban Booth. Akhirnya, sistem yang telah direka ini terbukti dapat mengira dan mengeluarkan nilai keluaran dalam bentuk integer daripada hasil pendaraban nilai masukan.

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LIST OF ABBREVIATIONS

ALU	-	Arithmetic Logic Unit
FPGA	-	Field Programmable Gate Array
ISE	-	Integrated Software Environment
VHDL	-	Verilog High Description Language
LSB	-	Least Significant Bit
MSB	-	Most Significant Bit
FIR	-	Finite Impulse Response
DSP	-	Digital Signal Processing
FA	-	Full Adder
RAM	-	Random Access Memory
DCM	-	Digital Clock Manager
ASIC	-	American Standard Integrated Circuit
RTL	-	Register Transfer Level
UCF	-	User Constraint File
LCD	-	Liquid Crystal Display
LED	-	Light Emitting Diode
XST	-	Xilinx Synthesis Technology
HDL	-	Hardware Description Language
VHSIC	-	Very High Speed Integrated Circuit
PLL	-	Phase Locked Loop
DLL	-	Delay Locked Loop
CLB	-	Configuration Logic Block
LUT	-	Lookup Table

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CHAPTER I

INTRODUCTION

1.1 Project Overview

Addition and subtraction process for normal computer is proceeds as if the two numbers were unsigned integer. On any addition and subtraction, the result may be larger than can be held in the word size being used. This condition is call overflow. When overflow occurs, the ALU must signal this fact so that no attempt is made to use the result. Compare with addition and subtraction, multiplication is a complex operation whether performed in hardware or software.

A wide variety of algorithms have been used in various computers. The purpose of this subsection is to give the reader some feel for the type of approach typically taken. The system begin with the simpler problem of multiplying to unsigned (non-negative) integers, and then we look at one of the most common techniques for multiplication of number in two‟s complement representation [1]. Booth algorithms have three reasons that are looking here by refer [1]. First, this will give you an example of an algorithm which is in multiplication has an addition and subtraction algorithm. In booth‟s algorithm will show the process of multiplier. Second, it will show you one way a computer can do multiplication, given only the kinds of functional units we have so far seen. By design the multiplication algorithm, it can be process to the hardware. Before implement to the hardware, test the design by using Xilinx simulator and check the functionality. Lastly, Booth‟s Algorithm is an example of how insights from mathematics can lead to efficiency, albeit at the expense of some increase in complexity. That mean more arithmetic can be more complex circuit of combinational logic gate.

Before discuss the booth algorithm, the first important thing must know is the theory by refer [1], the first digress for a moment to talk about how many numbers are represented in computers. The subject is considerably more complex than is presented here. For instance, the design is not representing floating point numbers [1].

1.2 Problem Statement

Nowadays, digital system has been used in daily life or industrial field because of the benefits compared with analog system. Due to crucial developing of digital system, many new complex digital devices had been design. Some of the devices are called microprocessor, microcontroller or microchip. It is very important to have a very high speed performance in all the devices. Booth Multiplier is one of the most important parts in the devices which can affect the performance of the devices.

So, the high speed and efficient multiplier system is important for the designers of microprocessor, microcontroller and others digital devices. As we know, multiplication algorithm can be operating on binary, decimal and hexadecimal number. But, to do the operation in binary number is very complex operation.

This project is being done to help design or create a prototype of digital system design that can operate as multiplier operation that would be implemented into microprocessor, microcontroller and other digital devices.

1.3 Objective

This project is more towards on implement multiplication technology with using FPGA as a device for design booth‟s algorithm. The first objective of this project is to design a digital multiplier using Booth Multiplier Algorithm in Verilog. The second objective is to design the booth‟s algorithm in two integer complement multiplication. Finally, the system that has design will implement to the FPGA trainer.

1.4 Project Scope

The scope project is the input will be in 4 bit multiply by 4 bit which will produce 8 bit output of accurate multiplied answer. The input and output of the system will only process and produce fixed point value. The system also can be accepted the negative value which is call signed number or two‟s complement number. Verilog is used as the language to design Booth‟s Multiplier Algorithm system. All the process will be running using Xilinx ISE 10.1 software which means to design the module and testbench module and the process simulation. Lastly, after the design is completed the system will implement on hardware which is FPGA board.

1.5 Thesis Overview

In this report, it was divided into five chapters which is introduction, literature review, methodology, result and discussion and lastly conclusion and recommendation. In chapter one, the project is about overview such as introduction to Booth‟s Algorithm, problem statement, objective and project scope.

In the literature review, all the past years project and research which is related to the project was discussed. After that, all the information and data gathered were compared to the Booth‟s Algorithm. Design the project using Field Programmable Gate Array to identify the functionality of this project.

For methodology, all the methods, hardware and software used in this project were verified. For this project, the Xilinx ISE 10.1 is used as software and Spartan 2 FPGA trainer is used as hardware.

In chapter four, all the results were discussed to justify any problem when developed the system. All the result of simulation must discussed detail and clearly. If the project is not functioning, discussed the problem and give a better solution. In last chapter is conclusion and recommendation that overall finding in this project is concluded. Give the recommendation for the future, what can this project do for the future. This recommendation can be used for references and also can be improve by anyone who wishes to develop this project.

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

In this chapter, all the literature review that is important to this project will be represent the literature review will include Booth Multiplier Algorithm (with procedure and example), VHDL and Xilinx Integrated Environment (ISE) 10.1 software. The detail of those will be discussed in this chapter.

2.2 Booth’s Algorithm

Table 2.1 show that the Booth Multiplier Algorithm Operation, which very important for this project. The algorithm rules give a procedure for multiplying binary integers in signed –2‟s complement representation. By follow this table, to design Booth Multiplier system make easier to understand the concept [2].

Table 2.1 Booth‟s Multiplier Algorithm Operation

A	**A-1**	**Operation**
0	0	Shift Right
0	1	A = A + M and Shift Right
1	0	A = A – M and Shift Right
1	1	Shift Right

2.3 Research of FPGA Implementation of Booth’s and Baugh-Wooley Multiplier Using Verilog

In the process of addition the multiple numbers of times is repeated. From the system, the number that is added is defined by multiplicand and the number of times it has to be added is given by multiplier [3]. The project of the multiplier must achieved the maximum speed in the multiplier hence, generation of partial product and adding if partial product must be optimized [3]. The multiplication perform on signed binary number and unsigned multiplication is perform on unsigned binary number is called a sign multiplication [3]. This project is to modified booth‟s algorithm in order to improve the performance which is high speed by reducing the product array multipliers [3].

Based on Figure 2.1; this is the process of booth‟s multiplier. In this block diagram, the input of multiplicand and multiplier is connecting to the control system. In multiplier the most significant bit is Xn which is the value can be added by 1 and the least significant bit is 0. The number of multiplicand must in two‟s complement or signed number. The two‟s complement happen when the value is negative. When this process is happening the value must inverted and adds to 1. Then, see the process of shifting in booth‟s bit. The process of shifting will shift to right until get the partial product. The product will save into control [4].

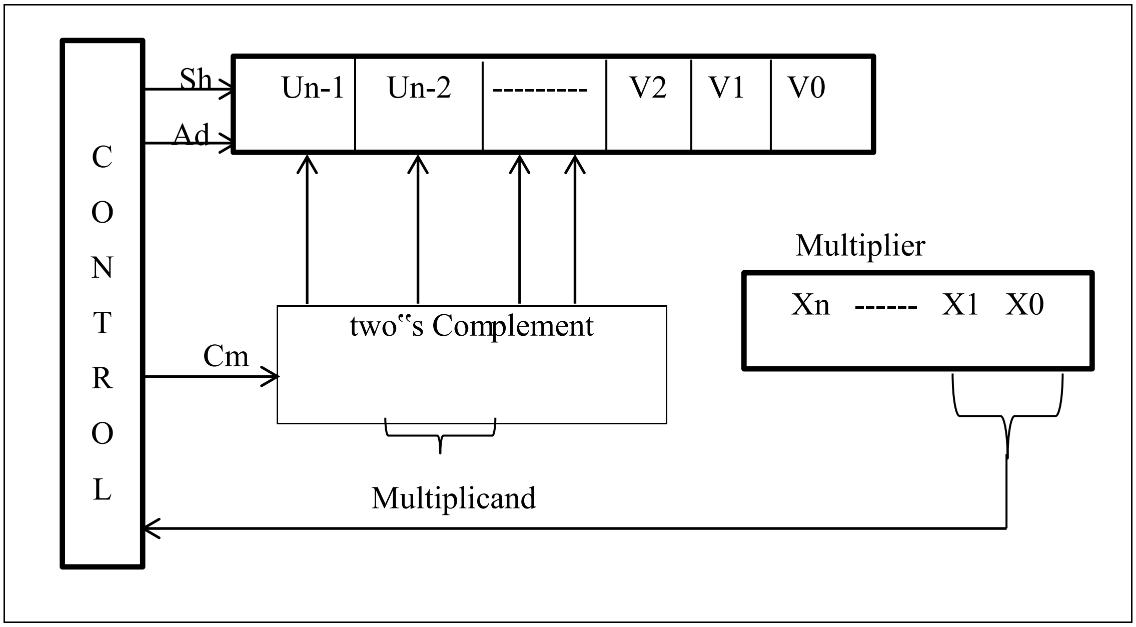

Figure 2.1 Booth‟s Multiplier Block Diagram

2.4 FPGA Implementation of an Adaptive Hearing Aid Algorithm using Booth's Wallace Multiplier

Hearing aids are one of many modems, portable, digital systems requiring power efficient design in order to give the life of the battery. Hearing aids are a typical example of a portable device. They include digital signal processing algorithms, which demands considerable computing power. Yet miniature pill sized batteries store to small amount of energy, limiting their lifetime [5]. Hearing impairment is often accompanied with reduced frequency selectivity which leads to a decreased speech intelligibility in noisy environments. One possibility to alleviate this efficiency is the spectral sharpening for speech enhancement based on adaptive filtering the important frequency contributions. for intelligibility in the speech are identified and accentuated [5]. This work discusses the power consumption in an FPGA implementation of the speech enhancement algorithm. It point out that power consumption can be reduce using Booth Wallace Multiplier [5].

2.4.1 Hearing Aid Architecture

To ease the computational burden, the real-time implementation of the hearing aid utilizes a spectral sharpening and noise reduction due to spectral sharpening design for the signal processing, which is illustrated in Figure 2.2, 2.3 respectively. The input signal comes in on the upper left side of the figure, is sampled at a rate of 8 kS/s, and is delivered to the high pass filter and the filtered signal is used for updating the filter coefficients [5].

Based on Figure 2.2, the output of the analysis filter is passed through synthesis filter and then to the speaker. The speech enhancement usually results from adaptively filtering the noise signals and subtracting from the primary input by using high pass filter. In the proto type implementation, the high pass filter with 6 taps, FIR filter was designed with cut off frequency 1k Hz.

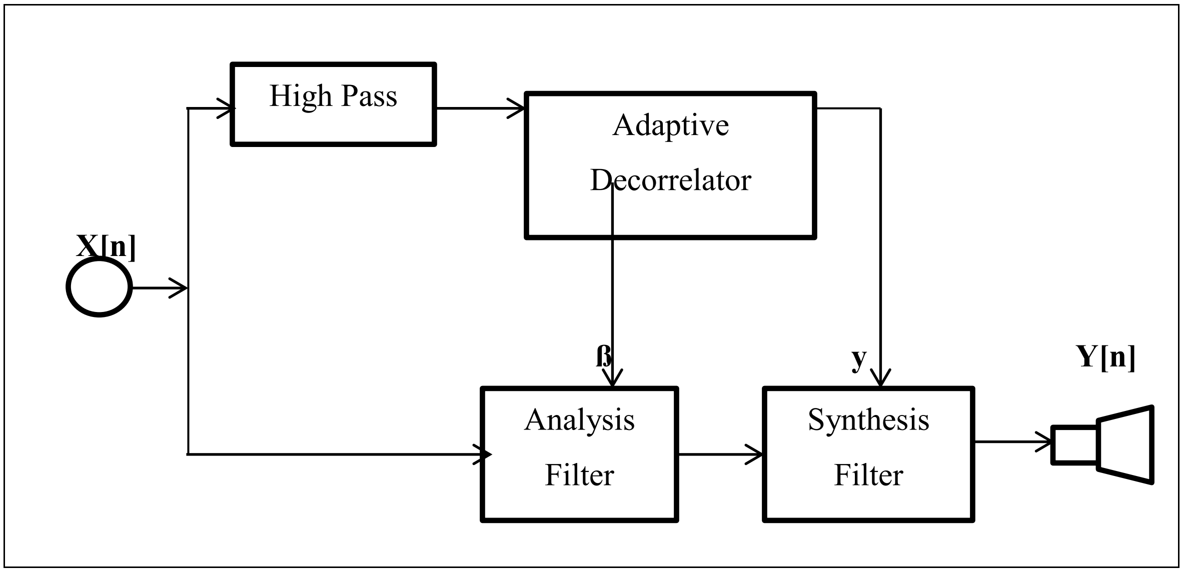

Figure 2.2 The Spectral Sharpening Filter for Speech Enhancement

Based on the Figure 2.3, the noise reduction can be reducing by using high pass filter. The adaptive decorrelator will process by using Laplace Transform to reduce the noise from speaker. Hardware multiplication is necessary in any system that contains Digital Signal Processing (DSP) functionalities.

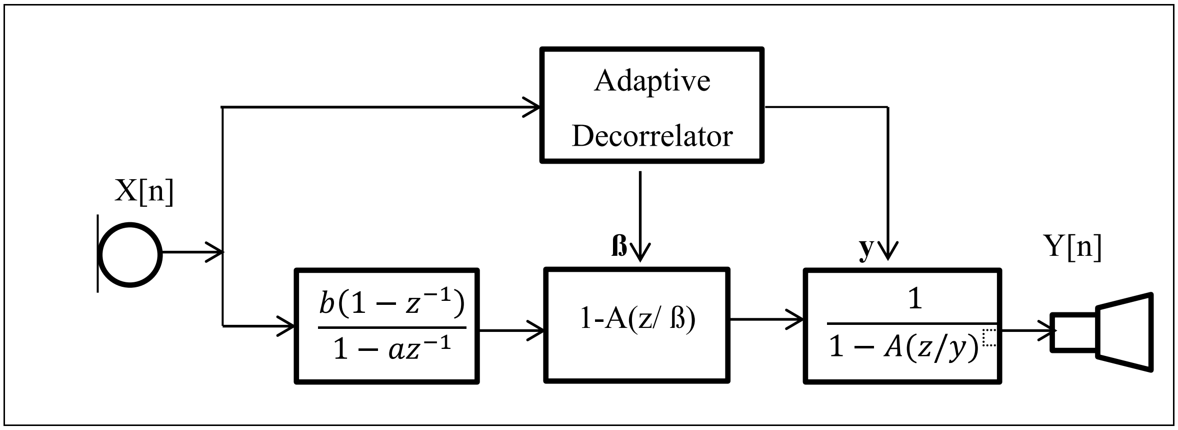

Figure 2.3 Spectral Sharpening for Noise Reduction

2.4.2 Multiplier Background

The shifts add Multiplier scheme is the most basic of unsigned integer multiplication algorithm. This algorithm uses addition and shift left operation to