ULTRA-THIN BODY SOI 22NM N-MOSFET
(THE EFFECT TiN GATE THICKNESS)

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A thesis submitted in partial fulfillment of the requirements for the award of the degree of Bachelor of Electronic Engineering (Computer Engineering)

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Special dedicated to my father, my beloved mother, brother, little sister and my fiancée.

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ABSTRACT

Currently, the demand of faster and smaller devices, need an attention to the researchers and semiconductor manufacturers make them putting a lot effort to face difficulties and challenges of improving on the performance of semiconductor devices. In other words, performance of short channel effects (SCE) in device, decreases the threshold voltage causes an, extra leakage current between the source and drain. The UTB comes to adoption of high-k/metal gate stack to improve the concept evolve to control the short channel effect with thin buried oxide (TBO). In addition, UTB SOI is very subject to the floating body effect and resulting in stability characteristic of the UTB SOI MOSFET. Technology Computer Aided Design (TCAD) tool from Silvaco's International® able to simulate the structure that has been designed in this project. Silvaco's DECKBUILD software used to design a structure of the MOSFET according to the steps in MOSFET fabrication process. Hence, Silvaco's ATLAS software used to obtain its characteristics. The analysis of the characteristics and results, such as transfer characteristics (Id-Vgs), sub-threshold curves (log Id-Vgs) and output characteristics (Id-Vd) were obtained to compare the drive current, leakage current, sub-threshold voltage and sub-threshold swing with titanium gate thickness for 5nm, 10nm, 15nm, 20nm, and 25nm for 22nm gate length. The 22nm UTBSOI carefully designed requirement of ITRS has been used as the reference. Results analyzed, give better performance in lower leakage current, high drain current and lower power consumption when the thickness of the titanium are increasing.

ABSTRAK

Pada masa ini, permintaan yang lebih cepat dan alat-alat yang lebih kecil, memerlukan perhatian para penyelidik dan pengeluar semikonduktor membuatkan mereka meletakkan usaha yang banyak untuk menghadapi masalah dan cabaran bagi meningkatkan prestasi peranti semikonduktor. Dalam erti kata lain, prestasi *short channel effects* (SCE) dalam peranti, mengurangkan *threshold voltage* menyebabkan, arus bocor bertambah di antara *source* dan *drain*. Kemunculan UTB datang bagi penggunaan *high-k* / *metal gate stack* untuk meningkatkan konsep evolusi bagi mengawal *short channel effects* dengan *Thin Body Oxide (TBO).* Di samping itu, UTB SOI adalah sangat bergantung kepada kesan *floating body* dan menyebabkan ciri-ciri kestabilan UTB SOI MOSFET. *Technology Computer Aided Design (TCAD)* perkakas daripada *International® Silvaco* yang dapat mensimulasikan struktur yang direkabentuk dalam projek ini. Perisian *DECKBUILD Silvaco* yang digunakan untuk merekabentuk struktur MOSFET mengikut langkah-langkah dalam proses fabrikasi MOSFET. Oleh itu, perisian *ATLAS Silvaco* yang digunakan untuk mendapatkan ciri-ciri MOSFET. Analisis ciri-ciri dan keputusan, seperti ciri-ciri pemindahan (Id-VGS) *sub-threshold curve* (log Id-VGS) dan ciri-ciri keluaran (Id-VD) telah diperolehi untuk membandingkan *drive current*, *leakage current*, *sub-threshold* voltan dan *sub-treshold swing* dengan ketebalan *gate* titanium bagi nilai 5nm, 10nm, 15nm, 20nm, dan 25nm untuk panjang *gate* 22nm. UTBSOI 22nm direka khas secara terperinci mengikut kehendak *ITRS* telah digunakan sebagai rujukan. Keputusan dianalisis, memberikan prestasi yang lebih baik dengan arus bocor lebih rendah, *drain current* yang tinggi serta penggunaan kuasa semasa yang rendah apabila ketebalan titanium semakin meningkat.

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MOSFET - Metal oxide semiconductor field effect transistor

SCE – Short channel effect

UTB – Ultra thin body

SOI – Silicon on insulator

SS – Sub threshold slope/swing

TBO – Thin buried oxide

VG – Voltage gate

Lg – Length gate

Tsi – Silicon thickness

CMOS – Complementary metal oxide semiconductor

Vth – Voltage Threshold

Ion – Drive Current

Ioff – Leakage Current

Tbox – Buried Oxide Thickness

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CHAPTER 1

INTRODUCTION

1.1 Introduction of Silicon On Insulator (SOI)

Silicon - On - Insulator (SOI) devices are a relatively new technology. Although the technology has been around since the 1960‟s, SOI devices are only recently becoming commercially viable, due to the expense associated with producing the devices. SOI devices are an advancement of standard MOSFET technology. The main difference between SOI and MOSFET technology is the inclusion of an insulating layer.

SOI devices are created from a thin layer of silicon placed on top of a layer of insulating. The purpose of this project is to design and analysis characteristic of Silicon - On - Insulator (SOI) Metal - Oxide - Semiconductor Field Effect Transistor (MOSFET) performance using semiconductor Technology Computer Aided Design (TCAD) tools requirement of the ITRS.

Semiconductor TCAD tools are computer programs which allow for the creation, fabrication, and simulation of semiconductor devices. These tools are used to design, semiconductor devices for various applications. Silicon - On - Insulator (SOI) device is a silicon-based device built upon an insulating substrate. Substrate materials can range from unusual materials such as ruby, diamond and sapphire, to common materials such as silicon dioxide. The SOI device design in this project was for an SOI MOSFET, using Silicon Dioxide for the insulator.

The structure of the device is very similar to that of a standard MOSFET device, but the presence of a thick layer of insulating material under the depletion region gives some changes of the device characteristics. During the course of this project, these programs were used to create simulations of the devices being worked on. These simulations provided an opportunity to study the effect of different device parameters on the overall device performance.

Throughout the year, the devices were simulated and gradually the performance of each one was improved, until an optimal device configuration was created for the particular applications. An SOI performance advantage over conventional bulk CMOS is mainly from lower average threshold-voltage due to transient floating-body (FB) operation and lower junction capacitance.

The partial depleted (PD) instead of fully depleted (FD) SOI has become the desirable choice for mainstream digital applications, due to the ease of manufacturing, better control of short channel effects, larger design window for the threshold voltage, and lower self heating effect [1]. The figure 1.1 shows the physical structure device of UTB SOI. Further study, to see the impact of different titanium gate thickness on the UTB SOI performance.

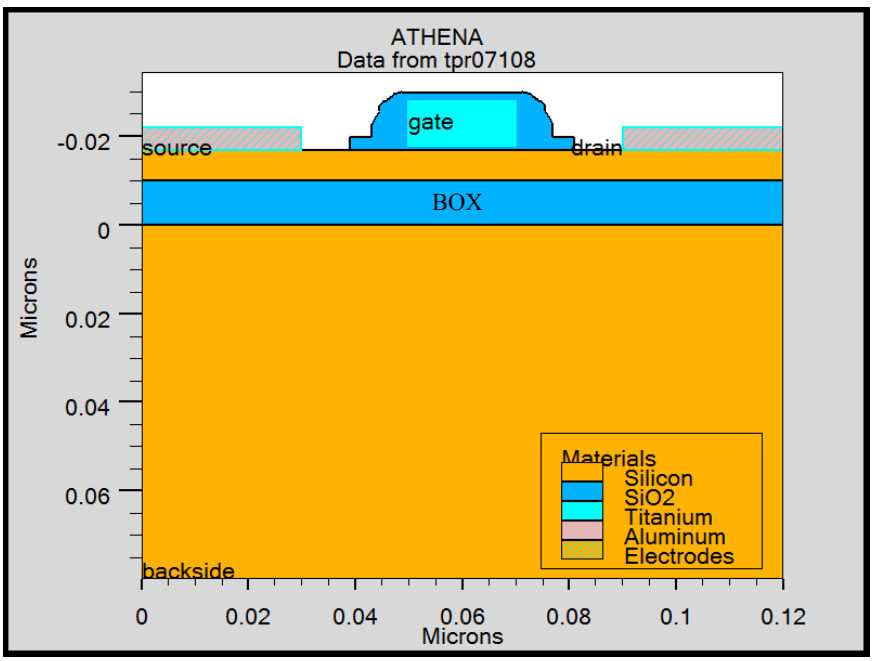

Figure 1.1: The physical structure of UTB SOI

1.2 Objective

The objectives of this project are:

1. To design Ultra-Thin Body SOI of the 22nm N - MOSFET.
2. To investigate the performance of 22nm N-MOSFET Ultra-Thin Body SOI including IV characteristic, leakage current, drive current, and subthreshold slope.
3. To compare the thickness of titanium (Ti) metal gate from 5nm, 10nm, 15nm, 20nm and 25nm at 22nm gate length.

1.3 Scope

i. Focus on the ultra-thin body SOI for 22nm N-MOSFET.
ii. Simulation tools using SILVACO to get the result including IV characteristic, leakage current, drive current, and the sub-threshold slope.

1.4 Problem Statement

The low switching energy of silicon on insulator technology still occur which degrades the performance. Meanwhile, the conventional fully depleted SOI MOSFETs have worse short-channel effect than bulk MOSFET and partially depleted SOI MOSFET. In words, short channel effects (SCE) decrease the threshold voltage, having extra leakage current between the source and drain degrade the performance of the device. The UTB utilizes metal gate may improve the performance ability to control the short channel effect with thin buried oxide (TBO).

The UTB SOI has many advantages which are it can improve transistor sub-threshold swing due to greatly improved the gate control, improve the channel mobility due to the reduced transverse electric field, reduce parasitic capacitance from the absence of depletion capacitance, leading to improve the speed; and reduce the power consumption.

The advantage used the SOI technology is reducing the SCE and improve performance. In ultra-thin body SOI (UTB SOI) with the adoption of high-k/metal technique are also being developed that acts on performance on of limitation of mobility. The usage UTB SOI can suppress SCE, scale gate length and also can reduce sub-threshold gate leakage current. In addition, UTB transistor does not rely on body doping to provide a potential barrier between the source and drain.

1.5 Thesis Guideline

In this thesis contains five chapters, Chapter 1- introduction of the research study, Chapter 2- literature review, Chapter 3- methodology, Chapter 4- result and discussion, and Chapter 5- Conclusion.

Chapter 1, the introduction of this project include the objective, scope, background of this project, and a problem statement.

Chapter 2, is presented the literature review consist of introducing to the scaling MOSFET theories using the ITRS demand, performance of the I-V characteristic, leakage current, short channel effect between source and drain, drive current and actual graph of sub-threshold slope.

Chapter 3 will be elaborate the design process simulation using SILVACO software whereby, Athena is used for writing the coding to build the structure of MOSFET and Atlas used for displaying the graph.

Chapter 4, discussion and analysis of the result, finding including an explanation of the problem occur when during the simulation. Investigate the result have been done in detail to optimize the performance the MOSFET.

Chapter 5 is the last chapter conclude the introduction, literature review, methodology, result, and discussion. It also contains part of my recommendation and ideas for the further research in related fields.

1.6 Conclusion

This chapter, present the background of this project to help the reader easily understand it. The problem statement discusses in this chapter can emphasis on the importance of this project. In addition, the objective, scope, and methodology already presented in easy to understand.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

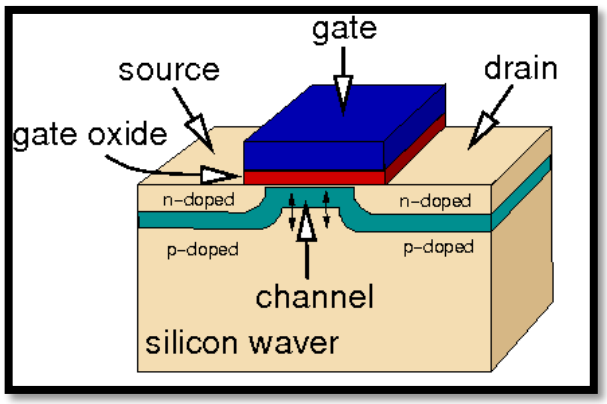

Figure 2.1: N- channel Mosfet (NMOS) Structure [2]

A MOSFET shows at figure 2.1 consists of an n- (p-) doped silicon substrate with two, highly p-(n-) doped contacts, source and drain. The channel region in between is covered by an insulator layer, the gate-oxide, which is in contact with the gate electrode. Without applying a voltage at the gate electrode, no current can flow from source to drain as the pn-junctions between each contact and the substrate act as two opposite diodes. [2]

When applying a positive (negative) voltage at the gate electrode, the channel region close to the gate oxide is 'inverted' from n-(p-) to p-(n-) doped and current can flow between source and drain. [2]

In addition, the central to the functionality is the thin insulating layer, the gate oxide. The gate oxide acts as the dielectric of a capacitor which attracts charge carriers into the channel region. Up to now, silicon dioxide (SIO2) has been used as a gate oxide. Two so far unparalleled electrical and structural properties of silicon's native oxide are commonly known as window glass are said to be one of the main reasons that silicon is today's semiconductor of choice. [2]

2.2 Bulk MOSFET/ Conventional MOSFET

The Metal-Oxide-Semiconductor has four terminal device which are drain (D), gate (G), source (S); and body (B) terminals. In addition, the channel region from drain and source, whereby they are connected to the inversion layer. The channel length (L) place between the source and drain channel, while the channel width (W) from in the direction normal to the channel length [3]. Below is the illustration of MOSFET structure.

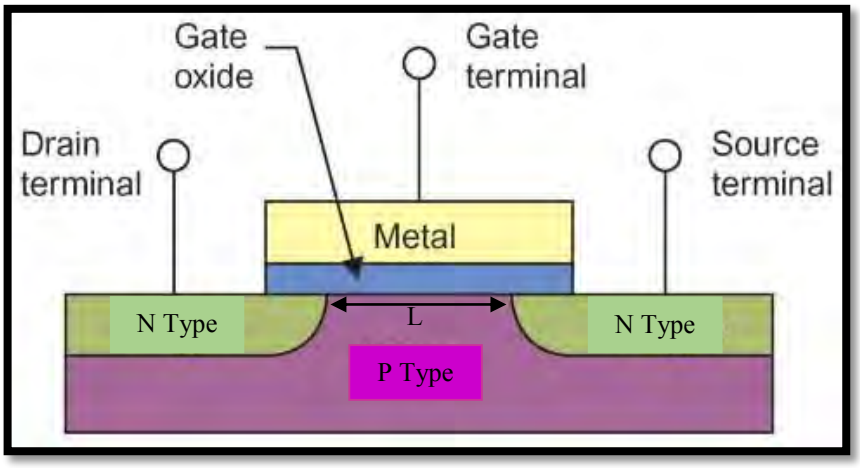

Figure 2.2: The P MOSFET structure [3]

In the depletion mode of MOSFET, to construct of n-channel mosfet there is two highly doped n regions are diffused into a p-type substrate and represent the source and drain [4].