GATE LEAKAGE IN LOW STANDBY POWER OF 18nm GATE LENGTH MOSFET

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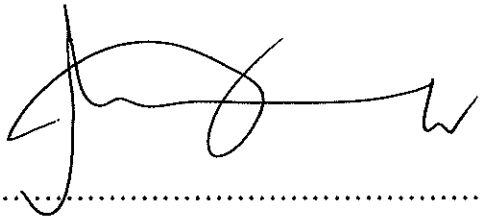

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DEDICATION

Special for the beloved parents and siblings who have a lot of support in order to complete this study may all appreciate the sacrifice you are rewarded by Allah SWT.

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ABSTRACT

The semiconductor devices are classified into three categories according to the performance which are high performance, low standby power and low operating power. Leakage current is a gradual loss of energy for charging capacitor and it happen to those categories of devices. Leakage power, due to the tunneling gate current, increases aggressively with the scaling of the insulator thickness. Low Standby Power (LSTP) devices are typically designed for low power applications that put strict limits on the gate current. This thesis present about design 18nm, 20nm and 30nm of gate length N-MOSFET and investigate the impact of different gate oxide materials on threshold voltage and drive current for similar materials with different gate length and for similar gate length with different material (polysilicon and titanium nitrate). This work was to explore because for a long time, the thickness of silicon dioxide reduces accordingly. This will reduce the performance of the device due to lead current leakage. In order to realize this project, it conducts by using Silvaco software which its tool are Anthena (to simulate device structure) and Atlas (to obtain the device characteristics). The results show titanium nitrate is the best material to use due to improve the performance devices. The higher value of the gate length will improve the current leakage.

ABSTRAK

Peranti semikonduktor diklasifikasikan kepada tiga kategori mengikut prestasi yang berprestasi tinggi, kuasa siap sedia rendah dan kuasa operasi yang rendah. Arus bocor adalah satu kehilangan beransur-ansur tenaga untuk mengecas kapasitor dan ia berlaku kepada semua kategori peranti. Kuasa kebocoran, disebabkan oleh arus terowong pagar, meningkatkan dengan agresif ukuran ketebalan penebat. Peranti Kuasa Siap Sedia Rendah (LSTP) biasanya direka untuk aplikasi kuasa rendah yang meletakkan had yang ketat ke atas arus pagar. Tesis ini sekarang mengenai 18nm reka bentuk, 20nm dan 30nm panjang pintu N-MOSFET serta menyiasat kesan bahan pagar oksida yang berbeza pada voltan ambang dan memandu semasa bagi bahan-bahan yang serupa dengan panjang yang berbeza dan pintu untuk pintu panjang sama dengan bahan yang berbeza (polisilikon dan titanium nitrat). Kerja ini diteroka kerana untuk masa yang lama, akan berlaku pengurangan pada ketebalan silikon dioksida. Ini akan mengurangkan prestasi peranti kerana kebocoran semasa memimpin. Bagi merealisasikan projek ini, ia menjalankan dengan menggunakan perisian Silvaco yang alat itu adalah Anthena (untuk simulasi struktur peranti) dan Atlas (untuk mendapatkan ciri-ciri peranti). Keputusan menunjukkan titanium nitrat adalah bahan yang terbaik untuk digunakan bagi meningkatkan prestasi peranti. Nilai panjang pintu yang lebih tinggi akan memperbaiki kebocoran semasa.

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CHAPTER 1

INTRODUCTION

Chapter 1 covers about the introduction part of this Final Year Project of Degree. It contains subchapter of objectives, problem statements, scopes of projects and project outline.

1.1 Introduction of Project

More than 30 years, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has continually been scaled down in size in channel length from two sub-micrometres and to sub-micrometers range following Moore's Law. The channel length of the MOSFET is reduced from 100nm to 45nm. The size reduction of the device makes great improvement to MOSFET operation. However, there are many effects when reducing the scale size of the MOSFET.

In MOSFET structure, it has 4 terminals; source (S), gate (G), drain (D), and body (B). In semiconductor, there are three categories according to performance, which are high performance, low standby power, and low operating power. Leakage current happens to all categories which are a gradual loss of energy for charging capacitor. It may reduce the performance of electronic product. Leakage current of MOSFET consists of three components called off-state sub threshold leakage current, gate direct tunneling leakage current and source/drain junction leakage current.

By adding high dielectric constant (k) oxides, it will reduce the leakage current and improve the performance of the MOSFET. High dielectric constant (k) oxides have some requirements which are good insulating properties, good thermal stability, capacitance performance, and high crystallization temperature. Table 1 shows several materials with its dielectric constant (k).

Table 1.1: Materials with different dielectric constants.

Material	Dielectric constant (k)	Conduction band offset (eV)
Al_2O_3	9	2.8
HfO_2	25	1.5
La_2O_3	30	2.3
SiO_2	3.9	3.0
Si_3N_4	7	2.0
Ta_2O_5	25	1.4
Y_2O_3	15	2.3
TiO_2	40	1.1
ZrO_2	25	1.4

1.2 Objective

The objectives of this project are**:**

1. To design 18nm, 20nm and 30nm of gate length N-MOSFET in Low Standby Power.
2. To investigate the impact of different gate oxide materials on threshold voltage and drive current for similar materials with different gate length.
3. To investigate the impact of different gate oxide materials on threshold voltage and drive current for similar gate length with different material.

1.3 Scope

This research is to review the characteristic of 18nm, 20nm and 30nm gate length N-MOSFET in Low Standby Power in the low performance device. Then, do some observation on 2 different materials of insulator which are titanium nitrate and polysilicon with similar gate length that conducted by Silvaco software which its tools is Athena (simulate the device structure) and Atlas (to obtain the devices characteristic). Furthermore, do the analysis of the result had been done to compare the MOSFET performance by the threshold voltage and drive current.

1.4 **Problem Statement**

Previously, MOSFET structures use silicon dioxide (SiO2) to avoid gate leakage. However, for a long time, the thickness of silicon dioxide (SiO2) reduced accordingly. This will reduce the performance of silicon dioxide (SiO2) and leakage current will increase in order to supply current from source to drain.

In addition, theoretically shorter gate length, will provide high density of current from drain to source. Thus, reducing of gate length from previous design is 30nm to 20nm and to 18nm was being designed. However, these changes will cause some disruption electrostatic force on the MOSFET. To handle these weaknesses, the best two materials were chosen to add on silicon dioxide (SiO2) in order to keep the performance.

1.5 Project Outline

The outline of this project is planning to ensure the flow of this research study is done properly. Besides that, this outline also can help the readers to fully understand the objective and the content of this thesis.

The report consists of five chapters which is Chapter 1 will discuss about the introduction of the project, which includes the objectives of the project, problem statements, scope of the project, and project outlines. The problem statement describes the problem faced by the performance of each topology and followed the discussion of the scope and significance of the project.

Chapter 2, presents the documentation of literature review, this chapter consist of the definition of a project, categories of leakage current, comparison about threshold voltage and drive current and also about dielectric materials.

Chapter 3 explaining the project flow from the starting until the end. In this chapter a briefly explain the procedures to design the MOSFET. It consists of the theoretical for the Silvaco software simulation including DEVBUILD and ATLAS.

Chapter 4 is the discussion stage where the result and the finding are presented. It consists of the explanation for the data and the problem occurred since the research begins and the update design to improve the finding result. Analysis from transfer curves and sub threshold curves also discussed in this chapter.

The final chapter is chapter 5 that explains about conclusion and recommendation for future work related to this project.

CHAPTER 2

LITERATURE REVIEW

This chapter presents an overview of the previous works on the related topic for the background study.

2.1 Introduction

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) defined as a very large integrated circuit (VLSI) block building with the area of applications. The MOSFET transition has four terminal devices called as Source (S), gate (G), drain (D) and body (B) terminals. However, two of the terminals are connected to each other (short circuit) internally to make three terminals appear in electrical diagram. In VLSI circuits, there are two types of MOSFET structure such as NMOSFET or PMOSFET.

According to the performance of semiconductor devices, ITRS classify them into three categories which are high performance, low standby power, and low operating power. Low operating power was used for low performance device and low cost consumer type application [8] [15]. Low standby power is usually used for low power consumption, actually to preserve battery life. Thus, the best solution to reduce the power dissipation is lowering the power supply voltage (VDD) [1].

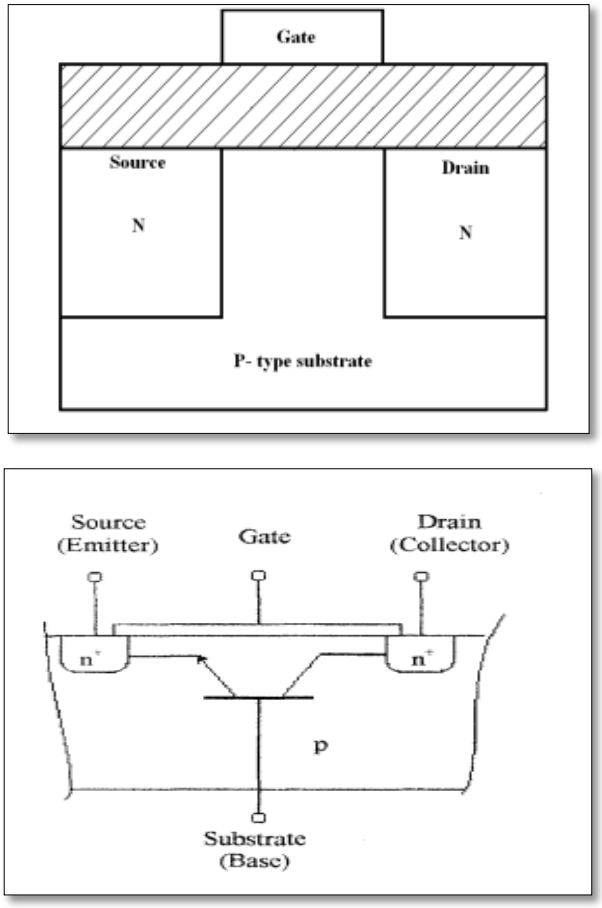

Figure 2.1: Structure of MOSFET [2] and the NPN transistor based on nMOSFET [13].