METAL GATE PROCESS REFINING USING GATE FIRST AND GATE LAST TECHNOLOGY FOR 22nm N-MOSFET

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This thesis is dedicated to

My family for their supports

and guide me throughout my academic career

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Bismillahirrahmanirrahim.

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ABSTRACT

This research has been done to improve the performance of 22nm n-MOSFET using two approaches which is gate-first and gate-last technology. Gate-first technology was initially developed by Sematech and the IBM-led Fishkill Alliance and found that it has flaws with their design. In gate-first technology, directly deposited gate has caused the gate damage due to the high temperature (over 1000°C) during the annealing process. To fix the flaws, gate-last technology has been proposed. Gate-last technology was introduced by Intel, implementing it in its 45nm technology. Gate-last technology overcomes the problem by depositing the dummy gate to withstand the high temperature throughout the annealing process then replace the gate with the real gate at the last process. Basically, metal gate is always pair up with high-k dielectric. Unfortunately, high-k dielectric is not defined by the simulation tools that we used. Thus, we use SiO_2 (silicon dioxide) as a dielectric constant for both processes. The metal gate used for this 22nm n-MOSFET is Titanium Nitrate (TiN). NMOS transistor was simulated using fabrication tool Silvaco ATHENA and the electrical characteristic was simulated using Silvaco ATLAS. The objective of this experiment is to design and compare the performance of 22nm n-MOSFET using gate-first and gate-last process. The results indicate that the gate-last process improves the performance of 22nm n-MOSFET in comparison with gate-first process. This is due to the undamaged metal gate during the annealing process.

ABSTRAK

Kajian ini telah dijalankan untuk menambah baik pencapaian bagi 22nm n-MOSFET mengunakan dua pendekatan, iaitu teknologi *gate-first* dan *gate-last.* Pada awalnya, teknologi *gate-first* telah dimulakan oleh Sematech dan IBM-led Fishkill Alliance dan didapati mempunyai kelemahan dalam reka bentuknya. Dalam teknologi *gate-first*, *metal gate* telah didepositkan secara langsung yang menyebabkan kerosakan *gate* kerana telah terdedah kepada suhu yang tinggi (melebihi 1000°C) semasa proses *annealing*. Untuk mengatasi kelemahan tersebut, teknologi *gate-last* telah dicadangkan. Teknologi *gate-last* telah diperkenalkan oleh Intel, yang mana telah dilaksanakan untuk teknologi 45nm. Teknologi *gate last* mengatasi masalah ini dengan mendepositkan *dummy gate* untuk menahan suhu yang tinggi semasa proses *annealing* kemudian menggantikannya dengan *metal gate* yang sebenar di akhir proses tersebut. Pada dasarnya, *metal gate* selalu digabungkan dengan pemalar dielektrik yang tinggi. Malangnya, pemalar dielektrik yang tinggi tidak ditakrifkan oleh alat simulasi yang digunakan. Oleh itu, SiO_2 (silicon dioksida) telah digunakan sebagai pemalar dielektrik untuk kedua-dua proses. *Metal gate* yang digunakan untuk 22nm n-MOSFET adalah Titanium Nitrat (TiN). NMOS transistor telah disimulasikan menggunakan alat fabrikasi Silvaco ATHENA dan ciri-ciri elektrik telah disimulasikan menggunakan Silvaco ATLAS. Objektif kajian ni adalah untuk mereka bentuk dan membandingkan pencapaian 22nm n-MOSFET yang menggunakan teknologi *gate-first* dan *gate-last.* Keputusan menunjukkan bahawa proses *gate-last* dapat meningkatkan pencapaian 22nm n-MOSFET jika dibanding dengan proses *gate-first*. Hal ini disebabkan oleh *metal gate* yang tidak rosak semasa proses *annealing*.

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MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
NMOS	N-channel Metal-Oxide-Semiconductor
FET	Field-Effect Transistor
ITRS	International Technology Roadmap for Semiconductors
EOT	Equivalent Oxide Thickness
RTA	Rapid Thermal Anneal
SiO_2	Silicon Dioxide
HfO_2	Hafnium Dioxide
HK/MG	High-k Metal Gate
TCAD	Technology Computer Aided Design
IL	Interfacial Layer
Vds	Source-Drain Voltage
Vg	Gate Voltage
Vth	Threshold Voltage
C	Capacitance
I	Current
V	Voltage

CHAPTER 1

INTRODUCTION

1.1 Project Introduction

MOSFET (metal-oxide semiconductor field-effect transistor) is a four terminal device with source (S), drain (D), gate (G), and body (B) terminals. The body or substrate of the MOSFET is often connected to the source terminal, whereby make it a three terminal device like another field-effect transistor (FET). The MOSFET is the most common transistor in both digital and analogue circuits.

The MOSFET is a special type of FET that works by electronically varying the width of a channel along which charge carriers (electrons or holes) flow. The charge carriers enter the channel at the source, and exit through the drain. The width of the channel is controlled by the voltage on an electrode called the gate, which is located physically between the source and the drain and is insulated from the channel by an

extremely thin layer of metal oxide. The MOSFET is useful for power amplifiers and also well suited to high-speed switching applications. Most integrated circuits (IC) contain nano MOSFETs and mostly used in electronic devices.

Several integration schemes are being considered with the two main approaches being “gate-last” and “gate-first”. The gate-last approach is considered a low-temperature process since the metal is not exposed to high temperatures [1]. The major advantage of this approach is that metals with known work functions can be integrated with a relatively simple process flow without exposure to a high thermal budget. In the gate-first integration flow, a standard transistor process is used.

The specification of the 22nm n-MOSFET has been designed according to the ITRS (International Technology Roadmap Semiconductors) 2011 requirements. Generally, this research is to measure the performance of 22nm n-MOSFET that has been carefully designed using Silvaco simulator. The results is measure by comparing the IV-Characteristic of the two processes regarding the drive current, leakage current, subthreshold slope and threshold voltage. MOSFET structure is designed using the Silvaco simulator ATHENA whereas the graph is plotted using Silvaco ATLAS.

1.2 Problem Statements

The MOSFET has continually been scaled down in size. Small MOSFETs exhibit higher leakage current and lower output resistance [1]. The difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance, it is necessary to redesign the circuit.

Since the scaling of the CMOS transistor has been the primary factor driving the improvements in microprocessor performance, choosing the best gate engineering technologies is required in order to maintain this rapid rate of improvement. One of the important parts is to design the devices in perfect gate technologies to improve its performance in nano scales devices [1].

Gate-first technology means that the metal gate is formed at early stage of fabrication process and the gate itself acts as a mask for the source and drain implantation. During the gate-first fabrication, the high temperature in the anneal step can cause the gate damage thus destroy the long-term integrity of the gate stack that will affect the performance of the MOSFET.

Gate-last technology is introduced to overcome this problem. Gate-last technology uses a sacrificial polysilicon instead of the actual gate to mask the implantation. After the high temperature source-drain annealing cycles, the dummy gate was removed and metal gate electrodes were deposited and anneal at lower temperature.

1.3 Objectives

The main objectives of this project are:

- To design the 22nm NMOSFET using gate-first and gate-last technology.
- To analyse the electrical characteristics of the devices regarding to drive current (Ion), leakage current (Ioff), subthreshold slope (SS), and threshold voltage (Vth).
- To compare the performance of 22nm NMOSFET using metal gate with gate-first and gate-last technology.

1.4 Scope of Project

The scopes of the project are as the following:

- Focusing on refining process of the metal gate (Titanium Nitrate) using gate-first and gate-last technology.
- The device will be designed and simulate for 22nm n-type MOSFET.
- Simulation tools using Silvaco TCAD software, including Athena for design the structure and Atlas to plot the graph.

1.5 Thesis Outline

The outline of this project is planned to ensure that the flow of this research study is presented properly. Besides that, this outline also can help the readers to fully understand the project research all about from the first chapter to the last chapter.

Chapter 1 includes the project introduction, problem statements, objectives, scope of this project and the thesis outline. Theory and literature review is discussed in chapter 2.

Chapter 2 discussed about the MOSFET and the differential in its electrical performances. This chapter also states the research on the fabrication process of the N-Type MOSFET using these two processes, gate-first and gate-last. Besides, MOSFET scaling and Equivalent Oxide Thickness (EOT) that is related to the device characteristic performance is also outlined. This chapter will be the knowledge source to gain the understanding about the gate process theories.

The methodology and software implementation of this project is thoroughly discussed in chapter 3. The software to complete this research is SILVACO TCAD and it has two parts which are ATHENA and ATLAS.

Chapter 4 elaborate the results and discussions produced by the simulation. It consists of the findings and explanations of the data and problems occurs along this research is conducted. The finding is presented in form of the designed structure and graph comparison.

Lastly, in chapter 5 conclusion and recommendations are outlined. In this chapter, it concludes the overall project and makes a suggestion for the future work regarding this study.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

This chapter review on fundamental and basic concepts of MOSFET, MOSFET operation, characteristics and its electrical performance. The objective of this research is to compare the performance of n-type MOSFET using two different technologies known as gate-first and gate-last technology. Therefore, this review has been highlighted on theories, processes of fabrication and specifications used related to this project through readings and research on previous study. Next, some explanation about EOT (Equivalent Oxide Thickness), mosfet scaling, fabrication process, and several electrical characteristics are thoroughly elaborated.

2.1 Introduction to the MOSFET

The metal-oxide-silicon field effect transistor (MOSFET) consists of four terminals, namely the source, gate, drain, and substrate (body). It is, in its very simplest form, a simple extension of the MOS capacitor, in which the gate electrode and the semiconductor channel constitute the parallel capacitor plates and the isolating oxide layer is equivalent to the dielectric material [2]. Although the MOSFET has a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals [3], the body (substrate) of the MOSFET is commonly connected to the source terminal, making it three terminal devices like other field-effect transistors. Since these two terminals are normally connected to each other internally, it caused them to be short-circuited. Thus, only three terminals appear in electrical diagrams as illustrated in Figure 2.1.

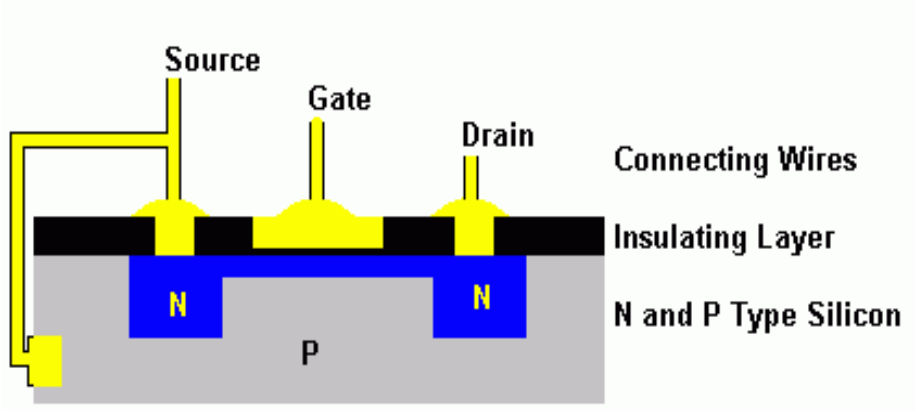

Figure 2.1: Source terminal short-circuit to the body (p-substrate) [6]

The drain and source terminals are connected to the heavily doped regions whereby the gate is connected on top of the oxide layer and the body terminal or substrate is connected to the intrinsic semiconductor [7]. The MOSFET is capable for voltage gain and signal power gain [7]. The inversion layer is formed between the source and drain terminal due to the flow of the carriers in it, the current flows in MOSFET are controlled by gate voltage. Thus it is known as a voltage controlled device.

N-type MOSFET is known by having n-channel region between source and drain. The source and drain is heavily doped n+ region (arsenic or phosphorus) with concentration of $10^{18}/cm^3$ and the substrate used is p-type substrate (Boron). The nMOS device is operated by setting a bias on the drain contact and using the gate voltage to control the flow of electrons from the source to the drain [2]. The current flows due to the flow of the negatively charged electrons. The gate voltage controls the electron concentration in the n-channel MOSFET is preferred over p-channel MOSFET as the mobility of electrons is higher than the holes. The basic structure of n-type MOSFET is shown in Figure 2.2.

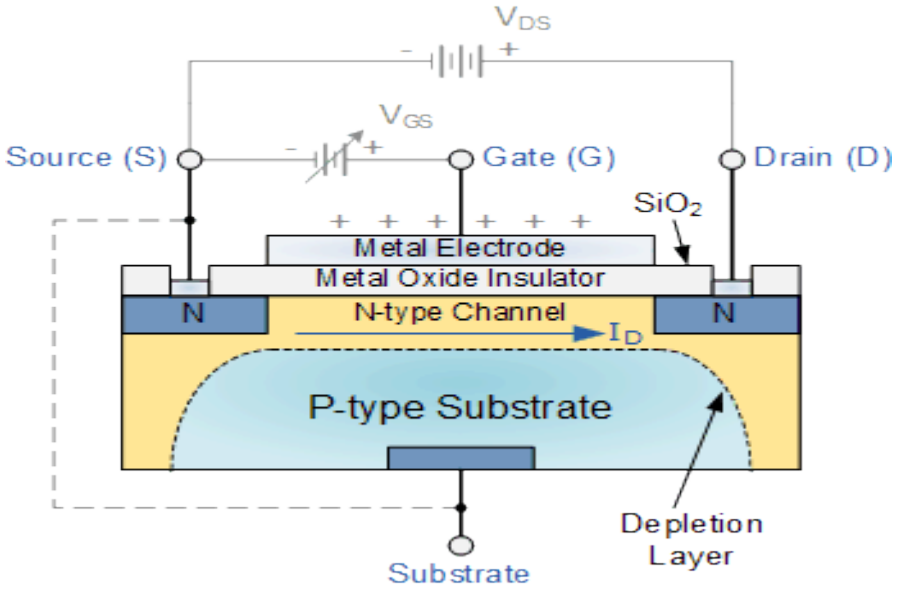

Figure 2.2: Basic n-Type MOSFET Structure [7]

2.1.1 Basic MOSFET operation

In the MOSFET, an inversion layer at the semiconductor – oxide interface acts as a conducting channel. For instance, in an n-channel MOSFET, the substrate is p-type silicon and the inversion charge consists of electrons that form a conducting channel between the n+ ohmic source and the drain contacts. At DC (direct current) conditions, the depletion regions and the neutral substrate provide isolation between devices fabricated on the same substrate.