# DEVELOPMENT ON 5GHz NEGATIVE FEEDBACK LOW NOISE AMPLIFIER

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UNIVERSTI TEKNIKAL MALAYSIA MELAKA FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER BORANG PENGESAHAN STATUS LAPORAN PROJEK SARJANA MUDA II				
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To my beloved family and supervisor

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### ABSTRACT

This project designs low noise amplifier (LNA) using negative feedback techniques for 5GHz. The LNA front end receiver is designed to operate at given frequency. The design process involved the use of design software's such as Advanced Design System (ADS) 2011. This project will use transistor from Avago Technologies (ATF-54143). Furthermore, this project presents the design of single stub elements at the input and output for impedance matching. This project also will analyse the performance of one stage and three stage of negative feedback low noise amplifier. To detect a weak signal, the receiving system must maintain a noise level that is lower than received signal. When using a low noise amplifier, noise is reducing by the gain by the amplifier while the noise of the amplifier is injected directly into the received signal. In this project, the design of microwave transistor amplifiers using the small signal S-parameters was studied to develop the LNA. S-parameter is a valuable aid both for collecting data for a transistor and them using data to predict the performance and design an amplifier circuit. The smith chart is an easy and practical tool used to designing matching circuits meanwhile the micro-strip line can perform the impedance conjugate matching. All the active component that use in this LNA is surface mount device (SMD) where it small in size and low cost. Finally, the hardware of this product was very compatible.

### ABSTRACT

Projek ini reka bentuk penguat bunyi yang rendah (jamax) menggunakan teknik maklum balas negatif untuk 5GHz. The jamax penerima akhir hadapan direka untuk beroperasi pada frekuensi yang diberikan. Proses reka bentuk melibatkan penggunaan perisian reka bentuk seperti Rekabentuk Sistem Lanjutan (ADS) 2011. Projek ini akan menggunakan transistor dari Avago Technologies (ATF-54143). Tambahan pula, projek ini membentangkan reka bentuk elemen puntung tunggal pada input dan output untuk impedans yang sepadan. Projek ini juga akan menganalisis prestasi satu peringkat dan tiga peringkat maklum balas negatif bunyi yang rendah penguat. Untuk mengesan isyarat yang lemah, sistem penerima mesti mengekalkan tahap bunyi bising yang lebih rendah daripada isyarat yang diterima. Apabila menggunakan penguat bunyi yang rendah, bunyi yang mengurangkan dengan keuntungan oleh penguat manakala bunyi penguat disuntik terus ke dalam isyarat yang diterima. Dalam projek ini, reka bentuk penguat gelombang mikro transistor menggunakan isyarat kecil S-parameter telah dikaji untuk membangunkan jamax itu. S-parameter adalah alat berharga kedua-dua untuk mengumpul data untuk transistor dan mereka menggunakan data untuk meramalkan prestasi dan reka bentuk litar penguat. Carta smith adalah alat mudah dan praktikal digunakan untuk mereka bentuk litar sepadan Sementara garis mikro jalur boleh melakukan pemadanan impedans konjugat. Semua komponen aktif yang digunakan dalam jamax ini adalah permukaan mount peranti (SMD) di mana ia bersaiz kecil dan kos rendah. Akhirnya, perkakasan produk ini sangat serasi.

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# LIST OF ABBREVIATION

ADS	-	Advance Design System
BFF	-	Band Pass Filter
BJT	-	Bipolar Junction Transistor
CAD	-	Computer Added Design
FCC	-	Federal Communication Commision
FET	-	field effect transistor
GaAs	-	Gallium Arsenide
GSM	-	Global system for Mobile Communication
IF	-	Intermediate frequency
ITU-T	-	International Telecommunication Union –
		Telecommunication Standardization
LNA	-	Low noise amplifier
NF	-	Noise Figure
RF	-	Radio frequency
SNR	-	Signal-to-noise ratio
S-parameter	-	Scattering Parameter
UWB	-	ultra-wideband

# LIST OF SYMBOL

- Zl Impedance load
- Zs impedance source
- C Capacitor
- L Inductor
- Z<sub>0</sub> characteristic impedance 500hm
- Y Admittance
- G Giga
- dB Decibel
- Mm millimeter
- Hz Hertz
- mA Miliampere
- $\Omega$  ohms
- V voltan
- nH nano henry
- uF micro Farad
- $\lambda$  Wavelength
- P pow

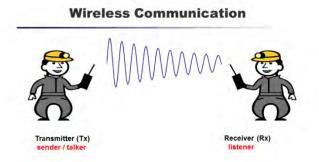
CHAPTER 1

# INTRODUCTION

This chapter presents the background of the project, problem statement, objectives, scope of work and thesis outline.

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### 1.1 Project Background



In communication system we have transmitter and receiver part which is transmitter is an electronic device which, with the aid of an antenna, produces radio waves. The transmitter itself generates a radio frequency alternating current, which is applied to the antenna. When excited by this alternating current, the antenna radiates radio waves. Whereas, receivers is an electronic device that receives radio waves and converts the information carried by them to a usable form. It is used with an antenna. The antenna intercepts radio waves (electromagnetic waves) and converts them to tiny alternating currents which are applied to the receiver, and the receiver extracts the desired information. Low noise amplifier located at front end of the radio-receiver circuit. It used to amplify possible very weak signal that captured by the antenna. The important parameter in LNA design is gain, noise figure, non-linearity and impedance matching. The design for LNA is based mainly upon the S-parameter of a transistor. For low noise, the amplifier needs to have a high amplification in its first stage. Therefore JFETs and HEMTs are often used. They are driven in a high-current regime, which is not energyefficient, but reduces the relative amount of shot noise. Input and output matching circuits for narrow-band circuits enhance the gain. Therefore, in this project propose to use FET LNA.

With the emergence of various communication standards, the need for low cost and reconfigurable/wideband receiver units is indispensable. The reconfigurable receivers usually employ inductors for tuning to a specific frequency band and, thus, occupy large area. In recent years, there has been a growing need for multiband and multimode transceivers for various wireless applications. This is due to multiple wireless standards for which various architectures addressing multi-band and multimode transceivers have been reported.

A basic rf front end typically consists of low noise amplifier image filter mixer for down conversion local oscillator and filter. The first stage the antenna and rf filter in the receiver chain is typically and LNA. Since every stage in the receiver chain adds noise in to the signal, very weak signals will be buried in this noise and be lost.

The main function of LNA is to provide high enough gain to overcome the noise of subs equal stage (mixer etc.), while adding as little noise as possible. At the same time it should be linear enough to handle strong interferers without introducing intermodulation distortion. The LNA is follow by the mixer that performs the down conversion to an intermediate frequency (IF) determine by the local oscillator. Due to the nature of the mixing process, the image problems occur. Several techniques to handle the image problem exist and will be discussed later in this chapter after the mixing filtering is required. Then, if necessary, another step of down conversion and filtering is made before the signal is simplified and ready for analogue-to digital conversion. The performance of receiver depends on the system design, circuit design and working environment. The acceptable level of noise and distortion varies with the application. Noise and distortion specify a lower limit on the usable signal -level at the output. For the output signal to be useful the signal power has to be larger than the noise power by an amount specify by the required signal-to-noise ratio (SNR). Including the distortion produced in the receiver, both noise and distortion should be at least the minimum specified signal- to-noise and distortion ratio (SNDR) below the signal power.

### **1.2 Problem Statement**

The signal will face interference when signal travels wirelessly and when the signal arrives at the receiver, it has some noise in the signal. For the receiver, that noise is not necessary because it will affect the information that was arrived by the signal. Because it is the unique requirements, using LNA at the RF front end of receiver is the best way to reduce the noise beside to ensure system efficiency and data accuracy. LNA is the simper receiver, space saving, excellent linearity, low current consumption and more efficient solution which allows the receiver chain variable gain. Signal amplification is the fundamental function in all communication system. Amplifiers in the receiving change that are closed to the antenna receive a weak electrical signal. Simultaneously strong interfering signal may be present. Hence, this LNA mainly determined the system noise figure and inter-modulation behaviour of the overall receiver. The common goes are therefore to minimise the system noise figure, provide enough gain with an efficient linearity.

Noise from the environment is avoidable, this sets, lower signal level that can be detected by a receiver. When noise at desired signal are applied to the input of a **-n**oiseless" network (an amplifier), both noise and signal power will be attenuated of amplifier by the same factor, does SNR at the input and output of the network similar. If the network is noisy, SNR out will be larger than SNR input. Since there additional noise, power at the output, does that produce by the network itself. Does, LNA is introduce at the front end of the receiver to minimise the problem. LNA is the special type of electronic amplifier use in wireless communication s system which applies very weak signal captured by an antenna. This is frequently used microwave system. When using LNA, noise is reduce with the gain by the amplifier while the noise of amplifier is injected directly into the received signal. LNA is usually used as the first stage amplifier for a receiving circuit. Since the signal from the antenna is very weak, the LNA amplifies the signal without contributing too much noise figured. This will improve overall noise figured, NF at the intermediate frequency, IF output.

### **1.3 Objective**

The objective of the project are to design a 5GHz low noise amplifier which provide enough gain, low noise figure, high linearity, great input and output matching with restraint of power consumption . Second objective of this project is to analyze the performance of a wideband low noise amplifier at 5GHz and incorporated with digital control based on electromagnetic (EM) simulations to determine S-Parameters, stability, linearity, efficiency, noise figure, bandwidth and gain.

#### 1.4 Scope of work

The scope of this project is to design the LNA for 5GHz. This project should be dividing to four parts which are:

- a) Calculate the stability, gain and noise figure.
- b) Simulate the LNA circuit by using advance design system (ADS)
- c) Parameter should be summarise and analysis such as the noise figure, power gain, voltage supply and stability performance. The comparison between calculation and simulation are analysed.
- d) The matching network is included in LNA design such as lumped element, quarter wave and stub.

### 1.5 Thesis outline

Generally, the report will consist of five chapter which are; chapter 1: Introduction, Chapter 2: Literature Review, Chapter 3: Methodology, Chapter 4: Results and analysis and Chapter 5: Conclusion and future network.

The first chapter is representing the introduction part. It is contain the project background, problem statement, objectives, scope of project, and discovered for the whole project.

The second chapter represented the literature review that involve in this project. The second chapter is about LNA. In this chapter also will give the information and theory about the LNA and how to design it.

The third chapter which is representing the methodology part will cover on the related methodologies applied in the project. The steps on design the single stage LNA starting from the selected transistor, all the calculation involve in order to design, obtain the simulation by using ADS software,.

The fourth chapter represents the result and analysis of the project. Here, the analysis of the result obtain will be discussed briefly. The result from the calculation, simulation and fabricated should be compared.

The last chapter should be conclusion and the future network for this project.

# CHAPTER 2

### LITERATURE REVIEW

This chapter discusses about general topologies in designing LNA. The S-parameter, DC biasing, matching network, and smith chart also will be elaborate through this chapter including the definition use in designing LNA.

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### 2.1 5GHz application

5 GHz bands basically under IEEE 802.11ac protocols. This is under list of WLAN and mostly sold under the trademark of Wi-Fi. The 802.11 workgroup currently documents use in five distinct frequency ranges which is 2.4 GHz, 3.6 GHz, 4.9 GHz, 5 GHz, and 5.9 GHz bands. The introduction of Wi-Fi is about two versions which are 802.11a and 802.11b. There is not much different for those two versions but not in term of price. 802.11b is more cheap compare to 802.11a so that consumer standard. 802.11b operate in 2.4GHz spectrum. These days, it's getting pretty crowded, and to help address the digital noise that comes with it, 5GHz Wi-Fi is making a comeback. The second latest version of Wi-Fi is in 2009 (802.11n) which cover both frequency 2.4GHz and 5GHz. 802.11ac (2.4 and 5GHz) 802.11ac was ratified in January 2014, but devices based on the draft specification were available for months prior. This standard brings the maximum data rates up to 1Gbps (almost double that of 802.11n). In most 802.11ac wireless access points, both 2.4GHz and 5GHz hardware is included, though most segregate the traffic from each onto its own network. 5GHz have some advantage of the reduced noise available. This will provide faster data rates, fewer disconnects, and a more enjoyable experience

#### 2.2 Topologies in design LNA

In communication networks, a topology is a usually schematic description of the arrangement of a network, including its nodes and connecting lines. There are two ways of defining network geometry: the physical topology and the logical (or signal) topology.

### 2.2.1 Common gate (CG)

 Input part for common gate is source terminal, output is for the drain and ground for gate or also known as -eommon". The analogous bipolar junction transistor circuit is the common-base amplifier. This technique can reduce noise and good isolation followed with some disadvantages which is Larger noise figure, lower bandwidth and poor linearity.

### 2.2.2 Cascode architecture

 Cascode is usually constructed from BJT or FET's transistors, with one operating as a common emitter or common source and the other as a common base or common gate. There is no direct coupling from the output to input and that make cascode improves input-output isolation (or reverse transmission). The superiority of these topologies is it can improve input output isolation, eliminate miller effect, and higher bandwidth. But the drawback is gain can be reducing due to insertion loss.

#### 2.2.3. Negative Feedback

 A negative feedback amplifier (or feedback amplifier) is an electronic amplifier that opposes the original signal by subtracts a fraction of its output from its input. The applied negative feedback increase the performance (gain stability, linearity, frequency response, step response) and reduces sensitivity to parameter variations due to manufacturing or environment. Many amplifiers and control systems use negative feedback because of the superiority.

### 2.3 Low Noise Amplifier (LNA)

Low noise amplifier only located at the receiver part in wireless communication system. It located at front end of the block diagram. Low noise amplifier is electronic device used to amplify a very weak signal that captured by antenna. Usually it located closed to the detection device to reduce losses in feedline.

An LNA is a key component which is placed at the front-end of a radio receiver circuit. Per Friis' formula, the overall noise figure (NF) of the receiver's frontend is dominated by the first few stages (or even the first stage only).

Using an LNA, the effect of noise from subsequent stages of the receive chain is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system. A good LNA has a low NF (e.g. 1 dB), a large enough gain (e.g. 20 dB) and should have large enough intermodulation and compression point (IP3 and P1dB). Further criteria are operating bandwidth, gain flatness, stability and input and output voltage standing wave ratio (VSWR).

For low noise, the amplifier needs to have a high amplification in its first stage. Therefore JFETs and HEMTs are often used. They are driven in a high-current regime, which is not energy-efficient, but reduces the relative amount of shot noise. Input and output matching circuits for narrow-band circuits enhance the gain .

### 2.3.1 LNA Application

The LNA is usually used as the first stage amplifier for a receiving signal from the antenna. Since the signal from the antenna is very weak, the LNA amplifies (Figure 2.0) the signal without contributing too much noise. This larger signal is then fix

to the mixer, which generally has higher noise figure. This will improve overall noise figure, NF at the intermediate frequency, IF output. If the power gain of the first stage is around 10 or more, the signal will sufficiently larger at the output of the first stage, so the additional noise contributed by the following amplifier stage or mixer will have a small degrading effect on the overall SNR, provide the noise contribution of the following stage is moderate. In the design of the first stage, the minimum noise figure requirement is more than maximum power gain or voltage standing wave ratio,VSWR.

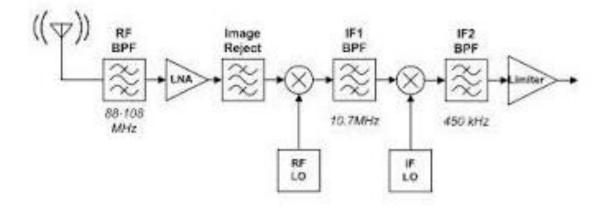


Figure 2.0: A Super-heterodyne Receiver with LNA

In contrast, the following architecture(Figure 2.0) suffers from lower sensitivity due to high noise figure of the mixer. Unless we can design a mixer that has very low noise and at the same time provide sufficient conversion gain, this architecture is generally avoided.

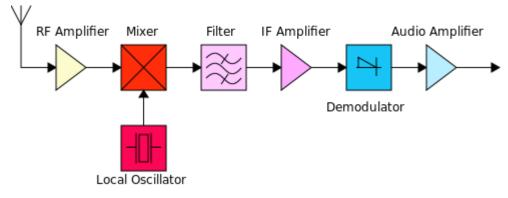


Figure 2.1: A Super-heterodyne Receiver without LNA

### 2.3.2 Scattering parameter (S-parameter)

Scattering parameters or S-parameters (the elements of a scattering matrix or Smatrix) describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals.

The parameters are useful for electrical engineering, electronics engineering, and communication systems design, and especially for microwave engineering.

The S-parameters are members of a family of similar parameters, other examples being: Y-parameters, Z-parameters, H-parameters, T-parameters or ABCD-parameters. They differ from these, in the sense that S-parameters do not use open or short circuit conditions to characterize a linear electrical network; instead, matched loads are used. These terminations are much easier to use at high signal frequencies than open-circuit and short-circuit terminations. Moreover, the quantities are measured in terms of power.

Many electrical properties of networks of components (inductors, capacitors, resistors) may be expressed using S-parameters, such as gain, return loss, voltage standing wave ratio (VSWR), and reflection coefficient and amplifier stability. The term 'scattering' is more common to optical engineering than RF engineering, referring to the

effect observed when a plane electromagnetic wave is incident on an obstruction or passes across dissimilar dielectric media. In the context of S-parameters, scattering refers to the way in which the traveling currents and voltages in a transmission line are affected when they meet a discontinuity caused by the insertion of a network into the transmission line. This is equivalent to the wave meeting impedance differing from the line's characteristic impedance.

Although applicable at any frequency, S-parameters are mostly used for networks operating at radio frequency (RF) and microwave frequencies where signal power and energy considerations are more easily quantified than currents and voltages. S-parameters change with the measurement frequency, so frequency must be specified for any Sparameter measurements stated, in addition to the characteristic impedance or system impedance.

S-parameters are readily represented in matrix form and obey the rules of matrix algebra.

### 2.3.3 Smith Chart

The Smith chart (Appendix B) basically a plot of all passive impedance in the reflection coefficient chart of unit radius. It also a graphical aid or nomogram designed for electrical and electronics engineers specializing in radio frequency (RF) engineering to assist in solving problems with transmission lines and matching circuits. Use of the Smith chart utility has grown steadily over the years and it is still widely used today, not only as a problem solving aid, but as a graphical demonstrator of how many RF parameters behave at one or more frequencies, an alternative to using tabular information. The Smith chart can be used to simultaneously display multiple parameters including impedances, admittances, reflection coefficients, Snn, scattering parameters, noise figure circles, constant gain contours and regions for unconditional stability, including mechanical

vibrations analysis. The Smith chart is most frequently used at or within the unity radius region. However, the remainder is still mathematically relevant, being used, for example, in oscillator design and stability analysis. Smith chart also very useful for solving transmission line problems. Although there are a number of other impedance and reflection coefficient charts that can be used for such problems

### 2.3.4 Matching Network

Impedance matching is often an important part of a larger design process for a microwave component or system. The basic idea of impedance matching is illustrated in Figure 2.2, which shows an impedance matching network placed between a load impedance and a transmission line. The matching network is ideally lossless, to avoid unnecessary loss of power, and is usually designed so that the impedance seen looking into the matching network is Z0. Then reflections will be eliminated on the transmission line to the left of the matching network, although there will usually be multiple reflections between the matching network and the load. This procedure is sometimes referred to as tuning. Impedance matching or tuning is important for the following reasons:

- Maximum power is delivered when the load is matched to the line (assuming the generator is matched), and power loss in the feed line is minimized.
- Impedance matching sensitive receiver components (antenna, low-noise amplifier, etc.) may improve the signal-to-noise ratio of the system.
- Impedance matching in a power distribution network (such as an antenna array feed network) may reduce amplitude and phase errors.

As long as the load impedance, ZL, has a positive real part, a matching network can always be found. Many choices are available, however, and we will discuss the design and performance of several types of practical matching networks. Factors that may be important in the selection of a particular matching network include the following:

- Complexity—As with most engineering solutions, the simplest design that satisfies the required specifications is generally preferable. A simpler matching network is usually cheaper, smaller, more reliable, and less lossy than a more complex design.
- Bandwidth—Any type of matching network can ideally give a perfect match (zero reflection) at a single frequency. In many applications, however, it is desirable to match a load over a band of frequencies. There are several ways of doing this, with, of course, a corresponding increase in complexity.
- Implementation—Depending on the type of transmission line or waveguide being used, one type of matching network may be preferable to another. For example, tuning stubs are much easier to implement in waveguide than are multisection quarter-wave transformers.
- Adjustability—In some applications the matching network may require adjustment to match a variable load impedance. Some types of matching networks are more amenable than others in this regard.

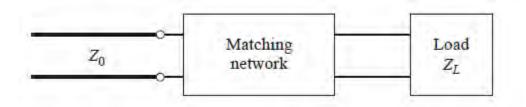


Figure 2.2: A lossless network matching arbitrary load impedance to a transmission line

### 2.3.4.1 Matching with lumped element

In impedance matching network, they are several types of matching network such as lumped element matching, quarter wave matching and stub matching. For lumped element, it contain LC component. The L-section uses two reactive elements to match arbitrary load impedance to transmission line. For L element they are two possible configurations will be illustrated in Figure 2.3. The smith chart is important part to design the matching network because from smith chart can determine the values of the component wants.

If the normalized load impedance, zL = ZL/Z0, is inside the 1 + jx circle on the Smith chart, then the circuit of Figure 2.4a should be used. If the normalized load impedance is outside the 1 + jx circle on the Smith chart, the circuit of Figure 2.4b should be used. The 1 + jx circle is the resistance circle on the impedance Smith chart for which r = 1.

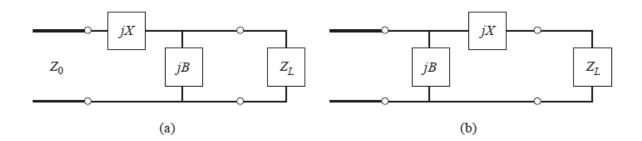


Figure 2.4: *L*-section matching networks. (a) Network for *zL* inside the 1 + jx circle. (b) Network for *zL* outside the 1 + jx circle.

In either of the configurations of Figure 2.4 the reactive elements may be either inductors or capacitors, depending on the load impedance. Thus, there are eight distinct possibilities for the matching circuit for various load impedances. If the frequency is low enough and/or the circuit size is small enough, actual lumped-element capacitors and

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inductors can be used. This may be feasible for frequencies up to about 1 GHz or so, although modern microwave integrated circuits may be small enough such that lumped elements can be used at higher frequencies as well. There is, however, a large range of frequencies and circuit sizes where lumped elements may not be realizable. This is a limitation of the *L*-section matching technique. We will first derive analytic expressions for the matching network elements of the two cases in Figure 2.4, and then illustrate an alternative design procedure using the Smith chart.

#### 2.3.4.2 Matching with Quarter wave

Quarter-wave transformer is a simple and useful circuit for matching a real load impedance to a transmission line. An additional feature of the quarter-wave transformer is that it can be extended to multisession designs in a methodical manner to provide broader bandwidth. If only a narrow band impedance match is required, a single-section transformer may suffice. However, multisession quarter-wave transformer designs can be synthesized to yield optimum matching characteristics over a desired frequency band. One drawback of the quarter-wave transformer is that it can only match a real load impedance. Complex load impedance can always be transformed into a real impedance, however, by using an appropriate length of transmission line between the load and the transformer, or an appropriate series or shunt reactive element. These techniques will usually alter the frequency dependence of the load, and this often has the effect of reducing the bandwidth of the match.

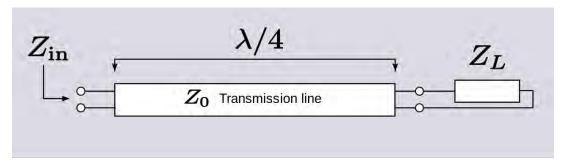


Figure 2.5: The quarter wave matchin

Formula for characteristic impedance of quarter wave:

$$Z_1 = \sqrt{Z_0 Z_L}$$

#### 2.3.4.3 Matching with single stub

The single stub matching is widely used to match any complex load to a transmission line. Stub consist a shorted or open segment of the line, also connected in parallel or in series with the line at appropriate distance from the load. Shorted are usually used because opened stubs may radiate from their opened ends. Shunt stubs are preferred for microstrip line or stripline, while series stubs are preferred for slot line or coplanar waveguide.

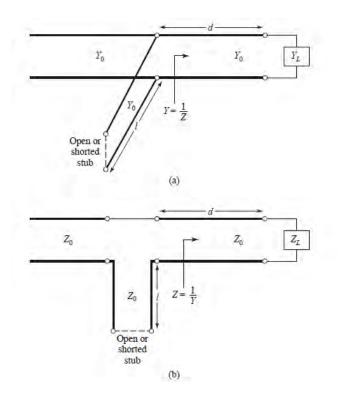


Figure 2.6: single stub tuning circuit. (a) shunt stub (b) series stub

The Smith chart of Figure 5.8 illustrates the basic operation of the double-stub tuner. As in the case of the single-stub tuner, two solutions are possible. The susceptance of the first stub, b1 (or b'1, for the second solution), moves the load admittance to y1 (or y'1). These points lie on the rotated 1 + jb circle; the amount of rotation is d wavelengths toward the load, where d is the electrical distance between the two stubs. Then transforming y1 (or y'1) toward the generator through a length d of line leaves us at the point y2 (or y'2), which must be on the 1 + jb circle.

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The second stub then adds a susceptance b2 (or b' 2), which brings us to the center of the chart and completes the match. Notice from Figure 5.8 that if the load admittance, yL, were inside the shaded region of the g0 + jb circle, no value of stub susceptance b1 could ever bring the load point to intersect the rotated 1 + jb circle. This shaded region thus forms a forbidden

range of load admittances that cannot be matched with this particular double-stub tuner.

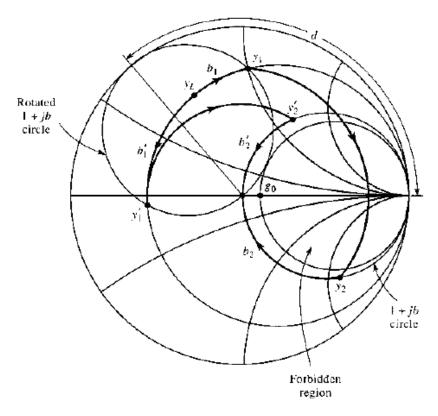


Figure 2.7: Smith chart diagram for the operation of a double-stub tuner

### 2.3.5 LNA parameters

This section introduces the important parameter used in the design theory of linear RF and microwave amplifier. Further, it develops some basic principle used in the analysis and design of such amplifier. However, below is definitions that can apply to a single stage linear amplifier.

### 2.3.5.1 Gain

Three type of power gain in terms of the S parameter of the two-port network and the reflection coefficient,  $\Gamma$ s and  $\Gamma$ L, of the source and load:

(a) Power gain = G = P load / P input is the ratio of power dissipated in the load ZL to the power delivered to the input of the two-port network. This gain independent of Zs, although some active circuits are strongly dependent on Zs.

$$G = \frac{|S_{21}|^2 \left(1 - |\Gamma_L|^2\right)}{\left(1 - |\Gamma_{\text{in}}|^2\right) |1 - S_{22}\Gamma_L|^2}$$
(2.1)

(b) Available Gain = GA = Pavn/Pavs is the ratio of the power available from the two port network available from the source. This assumes conjugate matching of both the source and load, and depends on Zs but not ZL.

$$G_{\mathcal{A}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_{\mathcal{S}}|^2\right)}{|1 - S_{11}\Gamma_{\mathcal{S}}|^2 \left(1 - |\Gamma_{\text{out}}|^2\right)}$$
(2.2)

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(c) Transducer Power Gain = GT = P load/ P avs is the ratio of the power delivered to the load to the power available from the source. This depends on the Zs and ZL.

$$G_T = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right) \left(1 - |\Gamma_L|^2\right)}{|1 - \Gamma_S \Gamma_{\rm in}|^2 |1 - S_{22} \Gamma_L|^2}$$
(2.3)

The operating gain design approach start from the desired load impedance and then the matches the resultant input impedance. The operating gain technique is recommended for linear-power amplifier, where the load is more important of the two terminations. Amplifier design this way have only one match port (input port). Since the output port is not matched, the maximum small-signal gain cannot get, but that is the price to get maximum absolute output power.

Operating power gain, derived from the transducer gain is:

$$Gp = \frac{\text{power delivered to the load}}{\text{power applied to the input of the two-port}}$$
(2.4)

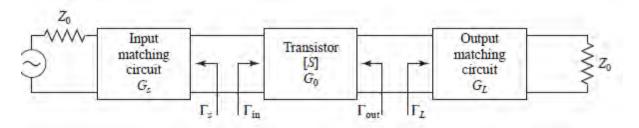


Figure 2.8: The general transistor amplifier circuit.

## 2.3.5.2 Stability and stability circle

In design LNA, need to consider the stability of transistor. The transistor was checking whether it is unconditionally stable or conditionally stable. The stability can define two types which are:

- (*a*) Unconditional stability: The network is unconditionally stable if  $|\Gamma in| < 1$  and  $|\Gamma out| < 1$  for all passive source and load impedances (i.e.,  $|\Gamma S| < 1$  and  $|\Gamma L| < 1$ ).
- (b) Conditional stability: The network is conditionally stable if  $|\Gamma in| < 1$  and  $|\Gamma out| < 1$  only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable

Following conditions that must be satisfied by  $\Gamma S$  and  $\Gamma L$  if the amplifier is to be unconditionally:

$$|\Gamma_{\rm in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1,$$
$$|\Gamma_{\rm out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1.$$

If the device is unilateral (S12 = 0), these conditions reduce to the simple results that |S11| < 1 and |S22| < 1 are sufficient for unconditional stability. For simpler test, the K – \_ test, where it can be shown that a device will be unconditionally stable if Rollet's condition and auxiliary condition

$$K = \frac{1 - |S11|2 - |S22|2 + |\Delta|2}{2|S12S21|} > 1$$
(2.7)  
$$|\Delta| = |S11S22 - S12S21| < 1$$
(2.8)

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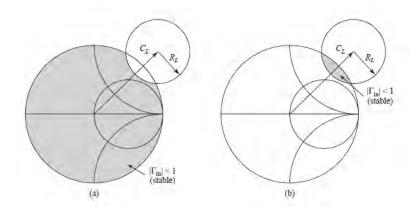


Figure 2.9: Output stability circles for a conditionally stable device. (a) |S11| < 1. (b) |S11| > 1. The output stability circle with a center:

$$C_{L} = \frac{\left(S_{22} - \Delta S_{11}^{*}\right)^{*}}{|S_{22}|^{2} - |\Delta|^{2}} \quad \text{(center)},$$
$$R_{L} = \left|\frac{S_{12}S_{21}}{|S_{22}|^{2} - |\Delta|^{2}}\right| \quad \text{(radius)}.$$

### 2.3.5.3 Noise parameter

The noise factor, F of a noisy two port is defines as the ratio between the available signal-to-noise power ratio at the input to the available signal to ratio at the output.

$$F = \frac{\frac{Sin}{Nin}}{\frac{Sout}{Nout}}$$

The noise factor of the two ports can also be expressed in terms of the source admittance Ys=Gs+jBs as

$$F=Fmin + \frac{Rn}{Rs} | Ys-Yopt |^2$$

When measuring noise, the noise factor is often represented in its logarithm from the noise figure,NF

$$NF = 10 \log F$$

## 2.2.5.4 Noise Circle

Noise circles refer to the contours of constant noise figure for two ports when plotted in the complex plane of the input admittance of the two ports. The minimum noise figure is represencymgented by a dot, while for any given noise figure higher than the minimum, a circle can be drawn. This procedure is adaptable in the source admittance notation as well as in the source reflection coefficient notation. Figure 2.10 shows the noise circle in the source reflection plane.

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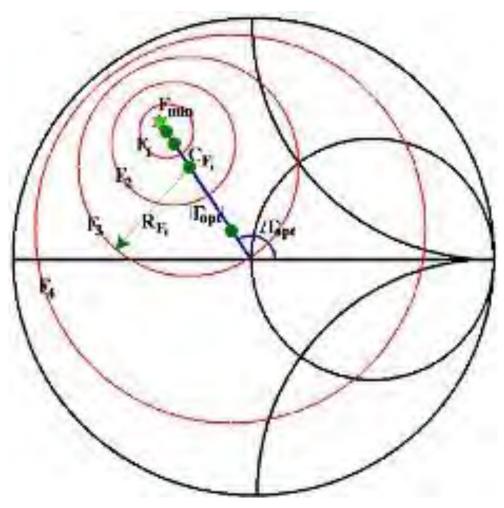


Figure 2.10: Noise circle

## 2.3.5.5 DC biasing network

Bias network is the least consideration factor in microwave transistor amplifier design. The purpose of the good DC bias design is to select the proper quiescent point and hold the quiescent point constant over variations in transistor parameter and temperature. The main purpose of the bias circuit is to maintain the collector current regardless of any drift in the DC current gain of the bipolar junction transistor. The S- parameter of a device are fixed and do not age so long as the correct bias current is maintained. A drop in bias current, over life, will cause the RF device gain and output power to fall. Below are the descriptions of the bias network in the project:

- a) A resistor bias network with a good results over moderate temperature changes was used instead of an active bias network because of its simplicity
- b) The DC biasing network for this project will not be integrated with the RF printed circuit board. At low frequency, a bypassed emitter resistors an important contributor to the quiescent-point stability. At microwave frequencies, the bypass capacitor, which is in parallel with the emitter resistor, can produce oscillations by making the input port unstable at some frequencies. Furthermore, an emitter resistor will degrade the noise performance of the amplifier. Therefore, in most microwave transistor amplifier, especially in the gigahertz region, the emitter lead of the transistor is grounded.

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# CHAPTER 3

# PROJECT METHODOLOGY

Methodology is the planning actions that are taken to complete the project. For this project, the methodology will focused in the design steps that will be taken in completing the project. The steps must be taken into account the objective of the project and plan according to the objective to make the project successful. The methodologies are needed to be plan carefully and to be following so that the project can be continuing smoothly without a hitch. The methodology is planned and illustrated in the form of flow chart. Figure 3.1 below show the methodology that is planned in completing the project:

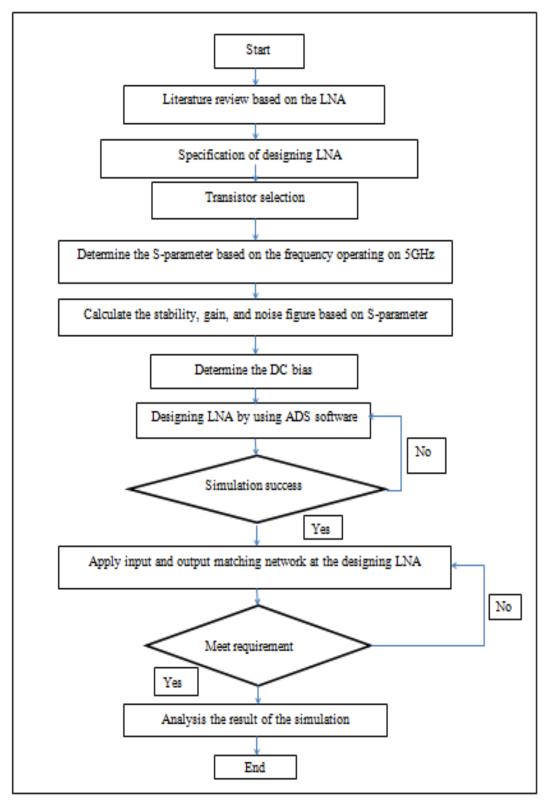


Figure 3.1 flow chart projects

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## 3.1 Introduction

Designing an LNA for lowest noise temperature requires knowing transistor noise parameters. Noise parameter can be obtain through a process that begins with measuring the S-parameter of a RF transistor and ends with using the circuit parameters of a FET model to calculate noise parameters. Since there is limitation to access a vector network analyser (VNA) to verify the S-parameter data on the manufacture data sheet, an assumption has to be made that all the data is accurate enough. But in this designing, we will not take transistor from datasheet. We will design the transistor instead of taking from datasheet.

The sensitivity of these receivers is often defined in terms of –noise temperature", which equivalent to noise figure. In the design of practical amplifier, a stability consideration is essential in additional to those for gain and noise. For low noise, design of impedance matching networks around the transistor which optimizes the transistor the best noise performance. The main steps are summarized as following:

Design of biasing networksDesign of impedance matching networks

The design process is quite challenging because it involve in the distributed resistance, inductance and capacitance in the matching network. The design specification for this project as shown as below:

-Frequency: 5 GHz -Gain : >4dB -Noise figure : <2.5dB

## 3.2 Design consideration

The following are the items that need to consider for design LNA. They are:

-Selection of the transistor
-S-parameter for 5Ghz frequency
-Stability of the transistor
-Gain (S-parameter)
-Noise figure (S-parameter)

## 3.2.1 Selection of the transistor

The FET transistor has been choosing to design LNA. The transistor is take from manufacture and available in market. But this project will design using FET because the advantages are high gain, high linearity performance, low noise figure, and others. This project wills ATF-54143. This transistor is manufacture by Avago Technologies which offer excellent high performance at economical price. The combination of good gain, good noise and low noise make FET ideal for this project. The data sheet can referred at Appendix A.

### 3.2.2 Simulation of s-parameter using ADS software

Since the transistor was selected, datasheet for ATF-54143 was determined. In datasheet ATF-54143, the S-parameter for frequency 5GHz did not show. Meanwhile, the ADS software is used to get s-parameter at frequency operating which is 5GHz.

# 3.2.3 Check the stability of the transistor

The stability of the transistor was checking based on Rollet's condition and Auxiliary condition,  $\Delta$ .

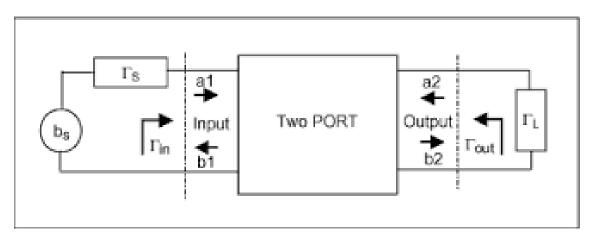
k>1

⊿<1

These two conditions are necessary and sufficient for unconditional stability, and are easily evaluated. In the project, the stability is consider unconditional stability because the device potentially stable and no oscillations will occur no matter what source and load reflection coefficient,  $\Gamma$ s and  $\Gamma$ L are presented.

Source and load reflection coefficient  $\Gamma$ in and  $\Gamma$ load respectively depend on load and source reflection coefficients as follows:

$$\begin{aligned} |\Gamma_{\rm in}| &= \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \\ |\Gamma_{\rm out}| &= \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1. \end{aligned}$$



The s-parameter is substitute into the equation (2.7) and (2.8) to find the value of K and  $\Delta$ 

### **3.2.4 Gain (S-parameter)**

S-parameters are valuable aid for collecting data for transistor and then using the data to predict performance and design the amplifier circuit. The values of s-parameter not only depend upon the properties of the transistor but also upon the source and load circuits used to measure them. This is because s-parameter values depend both upon the network and the characteristic impedance of the source and load used to measure it.

Several power gain equation appear in the literature which are equations (2.1), (2.2) and (2.3) are used through in the design of microwave amplifier.

### **3.2.5** Noise Figure

Noise figure, F of the two-port network is the ratio of signal-to-noise power ratio at the input to signal-to-noise ratio at the output. In other words, noise figure is a measure on how much a signal degrades as it passes through the two-port as a results of two-ports own noise. From the data sheet the minimum noise figure is 1db for frequency 900MHz. For frequency 5GHz the minimum noise figure still can get based on the calculation.

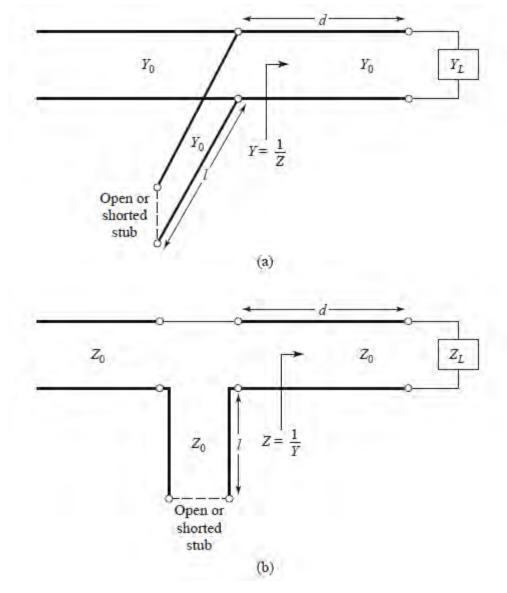
Noise figure also was calculated by using the equation 2.12 and 2.13 appeared in literature review.

### 3.3 Design of bias circuit

The necessary groundwork for designing an RF or microwave frequency amplifier has all been set. The first part of designing an amplifier is to find a circuit that will properly bias the RF transistor at the desired operating point but that will not interfere with the microwave operation of the circuit. By biasing the ATF-54143 according to the measured specification data sheet's Sparameter DC conditions, appropriate amplifier S-parameter can be achieved. For the ATF-54143, the performance of S-parameter over frequency (5GHz) is specified at Vce= 3V and Ic=60mA bias. DC voltage is 5 volt.

### 3.4 Design of matching network

A single frequency for low noise amplifier is going to be design at 5GHz. For that purpose, impedance matching networks which will allow that single band to pass and fulfill the requirement of the low noise amplifier parameters have to be design. This project used stubs as the matching networks. The impedance matching networks are designed for the frequency for which S-parameters of the ATF-54143 are available from the datasheet. The Vce= 3V and Ic=10mA for ATF-54143 are being selected due to low noise figure at these voltage. Matching is another important part need to consider in designing low noise amplifier. Miss matching makes the circuit low gain, high noise figure. In this project, single stub tuning being proposed as a matching of this project. Single-stub tuning circuit is often very convenient because the stub can be fabricated as part of the transmission line media of the circuit, and lumped elements are avoided. Shunt stubs are preferred for microstrip line or stripline, while series stubs are preferred for slot line or coplanar waveguide. In single-stub tuning the two adjustable parameters are the distance, d, from the load to the stub position, and the value of susceptance or reactance provided by the stub. For the shunt-stub case, the basic idea is to select d so that the admittance, Y, seen looking into the line at distance d from the load is of the form Y0 + jB. Then the stub susceptance is chosen as -j B, resulting in a matched condition. For the series-stub case, the distanced is selected so that the impedance, Z, seen looking into the line at a distance d from the load is of the form Z0 + j X. Then the stub reactance is chosen as -j X, resulting in a matched condition. Lastly, in this project we will use shunt stub matching network.



Single stub tuning circuit (a) shunt stub (b) series stub

CHAPTER 4

# **RESULT AND DISCUSSION**

This chapter describe about result and analysis that been carried out in this project. Simulation for this LNA is done by using Advance Design Systems. The results show simulation from our transistor such as noise figure, S-parameter and stability of the design.



# 4.1 Calculation

From data sheet of AVAGO Technologies (ATF-54143), the s-parameter is obtained from simulation as below:

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
3.000 GHz 3.100 GHz 3.200 GHz 3.200 GHz 3.400 GHz 3.500 GHz 3.500 GHz 3.600 GHz 3.700 GHz 4.000 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.200 GHz 4.500 GHz 4.500 GHz 4.500 GHz 5.100 GHz	$\begin{array}{c} 0.601 \ / \ 162.300 \\ 0.599 \ / \ 159.600 \\ 0.600 \ / \ 157.200 \\ 0.602 \ / \ 154.600 \\ 0.603 \ / \ 157.200 \\ 0.603 \ / \ 151.900 \\ 0.608 \ / \ 149.600 \\ 0.608 \ / \ 149.600 \\ 0.608 \ / \ 149.600 \\ 0.618 \ / \ 149.600 \\ 0.613 \ / \ 144.400 \\ 0.617 \ / \ 141.900 \\ 0.617 \ / \ 141.900 \\ 0.621 \ / \ 139.500 \\ 0.621 \ / \ 139.500 \\ 0.621 \ / \ 139.500 \\ 0.624 \ / \ 135.100 \\ 0.627 \ / \ 132.900 \\ 0.633 \ / \ 132.600 \\ 0.637 \ / \ 128.300 \\ 0.642 \ / \ 128.600 \\ 0.650 \ / \ 121.200 \\ 0.656 \ / \ 117.400 \\ 0.656 \ / \ 115.500 \\ 0.659 \ / \ 113.900 \end{array}$	0.078 / 26.500 0.080 / 25.600 0.081 / 24.800 0.083 / 24.100 0.085 / 23.100 0.086 / 22.200 0.090 / 20.200 0.091 / 19.100 0.093 / 18.100 0.094 / 17.100 0.095 / 16.100 0.095 / 16.100 0.095 / 15.100 0.095 / 15.100 0.098 / 14.100 0.099 / 13.200 0.101 / 12.100 0.102 / 11.000 0.103 / 9.900 0.105 / 8.900 0.107 / 6.800 0.108 / 5.800	5.098 / 51.000 4.948 / 48.900 4.800 / 46.900 4.671 / 44.900 4.543 / 42.800 4.419 / 40.800 4.304 / 38.800 4.192 / 36.700 4.089 / 34.800 3.896 / 30.800 3.799 / 28.900 3.712 / 27.000 3.628 / 25.000 3.545 / 23.100 3.466 / 21.200 3.392 / 19.200 3.319 / 17.300 3.250 / 15.400 3.161 / 15.300 3.114 / 11.700	$\begin{array}{c} 0.106 / -146.500 \\ 0.102 / -150.400 \\ 0.099 / -154.900 \\ 0.096 / -159.600 \\ 0.095 / -164.400 \\ 0.094 / -170.100 \\ 0.093 / -175.400 \\ 0.094 / 179.800 \\ 0.094 / 174.500 \\ 0.094 / 174.500 \\ 0.096 / 176.200 \\ 0.099 / 165.200 \\ 0.102 / 160.600 \\ 0.106 / 156.500 \\ 0.110 / 152.500 \\ 0.110 / 152.500 \\ 0.110 / 152.500 \\ 0.1119 / 145.400 \\ 0.124 / 142.600 \\ 0.129 / 139.600 \\ 0.134 / 136.500 \\ 0.136 / 154.400 \\ 0.142 / 131.500 \\ 0.146 / 129.300 \\ \end{array}$
5.200 GHz 5.300 GHz 5.400 GHz 5.500 GHz 5.600 GHz 5.700 GHz 5.800 GHz	0.663 / 112.100 0.668 / 110.200 0.673 / 108.200 0.673 / 106.200 0.678 / 103.700 0.680 / 102.100 0.677 / 100.700	0.109 / 4.900 0.111 / 3.900 0.112 / 2.800 0.113 / 1.700 0.114 / 0.500 0.115 / -0.600 0.116 / -1.500	2.988 / 8.100 2.927 / 6.300 2.871 / 4.500 2.818 / 2.700 2.766 / 0.700 2.712 / -1.000 2.665 / -2.700	0.150 / 127.100 0.153 / 125.200 0.157 / 123.600 0.161 / 122.000 0.164 / 120.400 0.168 / 118.600 0.171 / 116.700

Table 4.0 : S- parameter as 5Ghz

$$\begin{aligned} \Delta &= |S11S22 - S12S21| \\ &= |(0.656 < 115.5)(0.142 < 131.5) - (3.114 < 11.7)(0.107 < 6.8) \\ &= 0.401 \\ K &= \frac{1 - |s11|^2 - |s22|^2 + \Delta^2}{2|S12S21|} \\ &= \frac{1 - |0.656|^2 - |0.142|^2 + |0.401|^2}{2|3.114 < 11.7)(0.107 < 6.8)} \\ &= \frac{0.710301}{2(0.333198)} \\ &= 1.0665 \\ Z_0 &= ZL = Zs = 50\Omega \end{aligned}$$

$$\Gamma s = \frac{Zs - Z_0}{Zs + Z_0} = 0 , \Gamma L = 0$$
  

$$\Gamma in = S11 + \frac{S12 \ S21 \ \Gamma L}{1 - S22\Gamma L}$$
  

$$= S11$$
  

$$= 0.656 < 115.5^{\circ}$$
  

$$\Gamma out = S22 + \frac{S12 \ S21 \ \Gamma s}{1 - S11\Gamma s}$$
  

$$= S22$$
  

$$= 0.142 < 131.5^{\circ}$$
  
Power gain, G  

$$= \frac{|S21|^2(1 - |\Gamma L|^2)}{(4 - |\Gamma L|^2)}$$

 $\frac{|(1-|\Gamma L|^2)|1-S22\Gamma L|}{|(1-|\Gamma L|^2)|1-S22\Gamma L|}$ =  $\frac{|(3.114)|^2(1-0)}{(1-|0.656|^2)|1-0|}$ = 17.022=  $10\log 17.022$ = 12.31 dB

Available power gain

 $= \frac{|S21|^2(1-|\Gamma L|^2)}{(1-|\Gamma L|^2)|1-S22\Gamma L|}$  $= \frac{|3.114|^2(1-|0|^2)}{(1-|0.142|^2)|1-0|}$ = 9.897

=10log 9.897

= 9.9548 dB

Transducer Power Gain, GT

```
= \frac{|S21|^{2}(1-|\Gamma s|^{2})(1-|\Gamma L|^{2})}{(|1-S22\Gamma L|^{2})|1-\Gamma in\Gamma s|^{2}}= |3.114|^{2}= 9.696= 10 \log 9.696= 9.866 \text{ dB}
```

# 4.2 Simulation

Before designing any low noise amplifier (LNA) every designer has to check the stability of the device chosen for design. Manually, the calculations are very long but it is much quicker to simulate in any circuit simulating tool, for this ADS simulator was used to check the stability of the device and it was found that the selected ATF 54143 is potentially stable to the desired frequency at 5 GHz. To stabilize at frequency range between 4 GHz to 6 GHz. The Figure 20 and Table 3 show the stability at 5GHz frequencies.

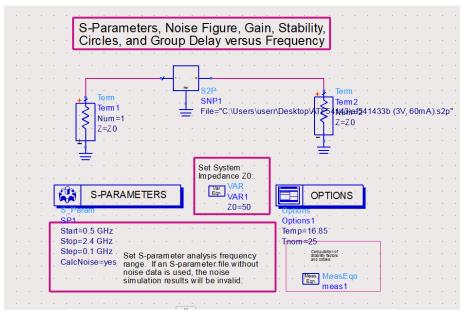


Figure 4.1: step in ADS to get the simulation result

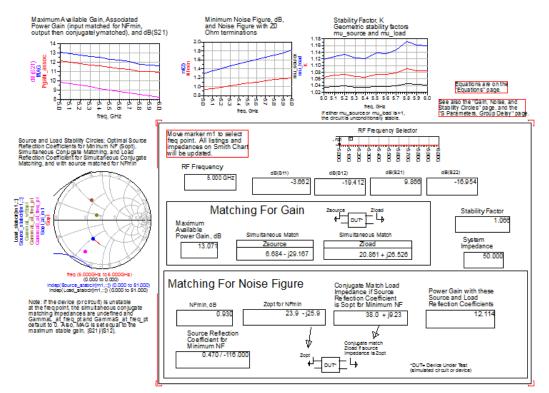
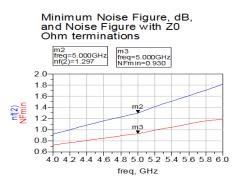
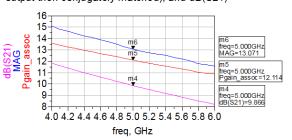


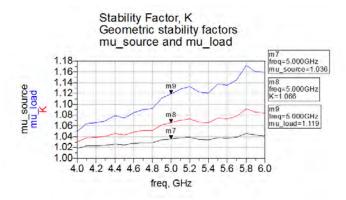
Figure 4.2: result of simulation in ADS



Maximum Available Gain, Associated Power Gain (input matched for NFmin, output then conjugately matched), and dB(S21)



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Parameter	Simulation	Calculation
Stability, K	1.066	1.0665
Power gain, Gp	12.114db	12.31db
Available gain, GA	13.071db	9.9548db
Transducer power gain, gt	9.866db	9.866db

Table 4.3: comparison between simulation and calculation result

# 4.3 Negative feedback LNA and biasing

The technique for this LNA is using negative feedback amplifier. Below is the designing of circuit into ADS. It consists of active element such as Resistor (270ohm) and inductor (10nH). The simulation result show that low noise figure, stability k>1, high gain but bad return loss. Return loss can be fixed by design input and output matching network.

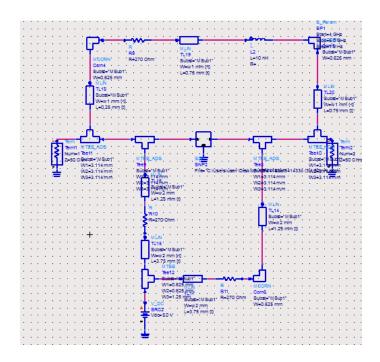


Figure 4.4: schematic diagram of negative feedback and biasing only

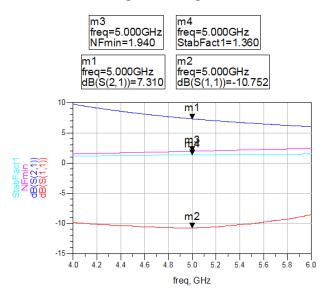


Figure 4.5: result simulation of schematic 1<sup>st</sup> stage LNA

## 4.4 Matching Network

In designing the LNA, the RF input matching is almost the main part. Although it is the way to obtain the higher gain and better input return loss while to achieve the low noise figure an LNA design. Filter actually exists before the LNA have a poor input return loss, thus will affect the performance of the systems. Therefore, the goal for the input matching is to achieve good return loss and noise figure while maintaining acceptable gain. In this matching we decide to use single stub matching than lumped element. So this type of design will directly into microstrip line.

By using the ADS simulation we get the input matching by get the value of 5GHz frequency in source impedance (Zopt) required which achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt. For best noise match (match for lowest noise figure but not best S11 return loss), need to match to Zopt.

Simulation based on input single stub matching:-

AUG Passive Cit	rcuit DesignGuide		-					
File Tools	View							
rs 🥨	<b>95</b> 🖂 🗙  -	骨 ━ 飞 =	Ĩ					
Garrene berten	Current Schematic SmartComponent (matching [ain_lib:matching:schematic]: 29 (DA_SSMatch1							
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schematic			esign, Simulation, Optimiza	tion, Display				
Overview	Design Assistant	Simulation Assistant	Optimization Assistant	Display Assistant				
<ol> <li>Place a the too</li> <li>Place a SmartC</li> <li>Select</li> <li>Design</li> <li>Set Sm The "A</li> <li>Simulat</li> </ol>	<ol> <li>Passive Circuit DesignGuide: SmartComponent Overview</li> <li>Place a SmartComponent from one of the "Passive Circuit" palettes (accessible from the toolbar buttons or "view" menu above).</li> <li>Place an appropriate substrate ("MSUB" or "MLSUBSTRATE") if required for selected SmartComponent (accessible from "Passive Circuit" palettes).</li> <li>Select the SmartComponent from the "SmartComponent" list above.</li> <li>Design SmartComponent from the "Design Assistant" tab.</li> <li>Set SmartComponent simulation frequencies from the "Simulation Assistant" tab. The "Automatically Display Results" option controls automatic launching of display following simulation.</li> </ol>							
8. If the p								
9. Re-sim	ulate SmartComponer	nt from the "Simulation A	ssistant" tab.					

43

MSub	•
MSUB	DA_SSSMatch1_matching
MSub1	DA SSSMatch1
H=1.6 mm	Subst="MSub1"
Er=4.4	F=5 GHz
Mur=1	Zin=50 Ohm
Cond=1.0E+50	Zload=(23.9-j*25.9) Ohm
Hu=1.0e+033	Zstub=50 Ohm
T=0.035 mm	Zline=50 Ohm
TanD=0.019	Delta=0 mm
Rough=0 mm	a a second as a second as
Bbase=	
Dpeaks=	

irrent Sche			SmartComponent	
atching [aii	n_lib:matching:schema	atic]: 35 🔹	DA_SSMatch1	
irrent Desig	n		SmartComponent Capability	
chematic			Design, Simulation, Optimiza	tion, Display
Overview	Design Assistant	Simulation Assistant	Optimization Assistant	Display Assistant.
Designing S	d SmartComponent De imartComponent gress	⊧sign		100%
Designing S	martComponent	esign Design All	Help	
	martComponent		Help	

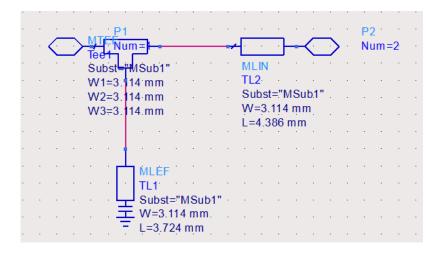


Figure 4.6: input matching

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Simulation based on output single stub matching:-

Same step like input single stub. We using design guide to generate the matching. The different is on the Zin and Zload data. Below is the information for output matching.

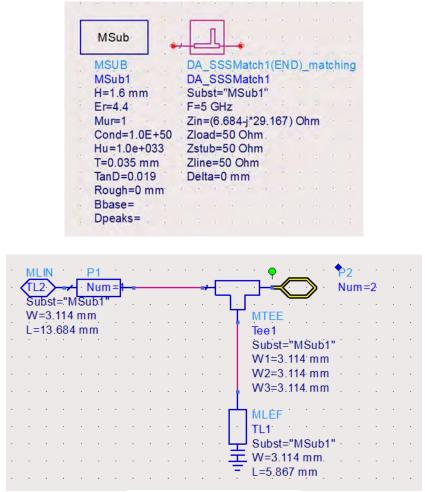


Figure 4.7 output matching

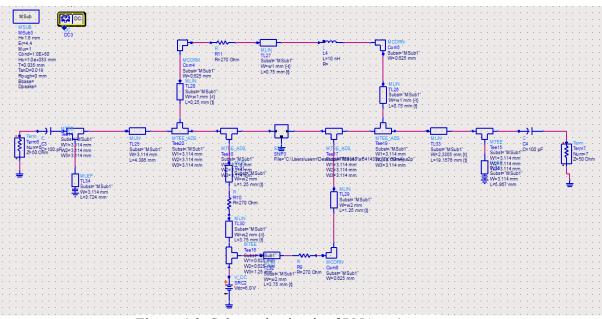


Figure 4.8: Schematic circuit of LNA at 1 stage

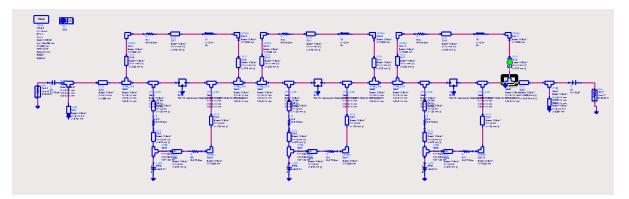
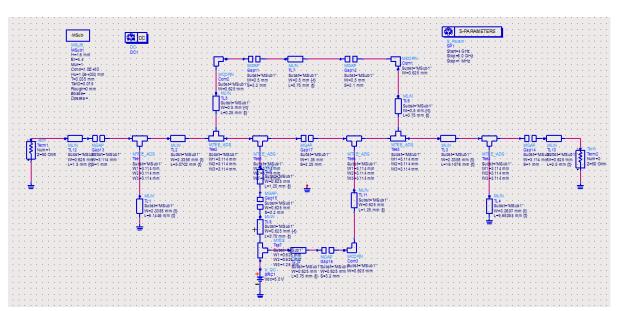


Figure 4.9: Schematic circuit of LNA at 3 stage

## 4.5 **Optimization**

The result shows that after matching and optimization. The optimization process well done when the matching network match with 50ohm. The optimization process tune by the parameter of input matching network which for magnitude S11 and magnitude for S22. This magnitude refers as reflection coefficient.

Then, after matching network being constructed in a microstrip line, it is built in electrical transmission line which can be fabricated using printed circuit board technology. At the end at the input impedance we adjusting the value and determine it by tuning the component such as MLIN, MTEE and etc.



# 4.5.1 1<sup>st</sup> stage schematic simulation result

Figure 4.10: schematic diagram of 1<sup>st</sup> stage LNA

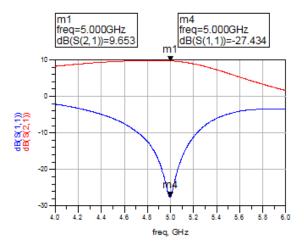


Figure 4.11: simulation result of gain and return loss 1stage LNA

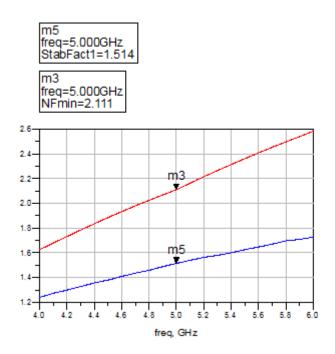
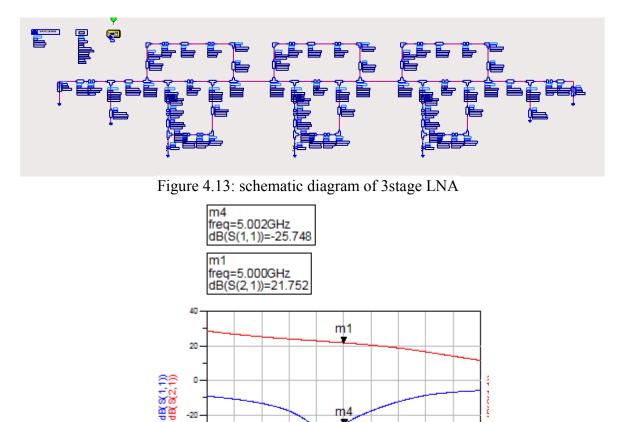


Figure 4.12: simulation result of noise figure and stability factor 1stage LNA



# 4.5.2 3<sup>rd</sup> stage schematic simulation result

-40

-60

4.0

4.2

Figure 4.14: simulation result of gain and return loss of 3stage LNA

4.8 5.0 5.2

freq, GHz

4.4 4.6

5.8

6.0

5.6

5.4

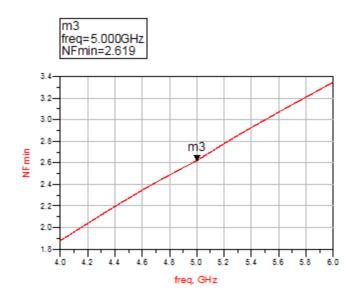


Figure 4.15: simulation result of noise figure 3stage LNA

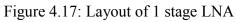
Parameter	1 <sup>st</sup> stage	3 <sup>rd</sup> stage
Gain (S2,1)	9.653dB	21.752dB
Return loss (S1,1)	-27.434dB	-25.748dB
NF min	2.111	2.619

Table 4.16: Comparison table between 1<sup>st</sup> stage and 3<sup>rd</sup> stage negative feedback LNA schematic

The value that were obtained is an optimized value, based on the table the value of S21 on 3-stage cascade single stage amplifier is more stable than 1-stage. More gain is occur when cascade the 1-stage but the return loss and noise figure is lower than 1-stage result. But both stage follows design specification that mention before in chapter 3. So, both stage are accepted to proceed next step to layout simulation. In schematic simulation, most of the circuit is ideal circuit where usually we can get higher result compare to layout result.



4.5.3 1<sup>st</sup> stage layout simulation result:



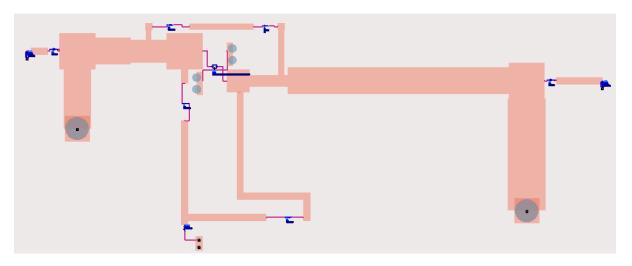


Figure 4.18: Import layout of 1 stage LNA

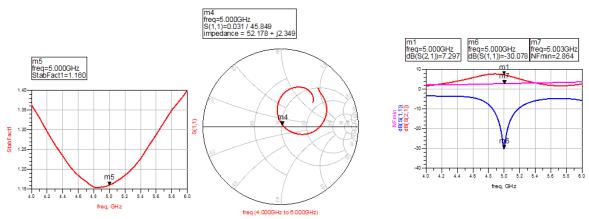


Figure 4.19: result of simulation 1<sup>st</sup> stage layout

# 4.5.4 3<sup>rd</sup> stage layout simulation result:

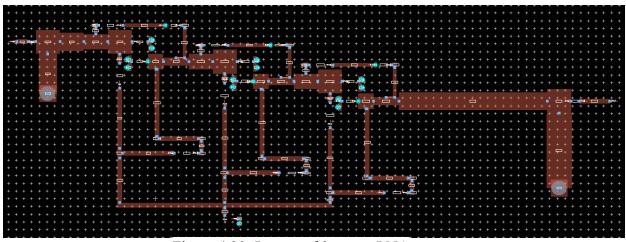


Figure 4.20: Layout of 3 stages LNA

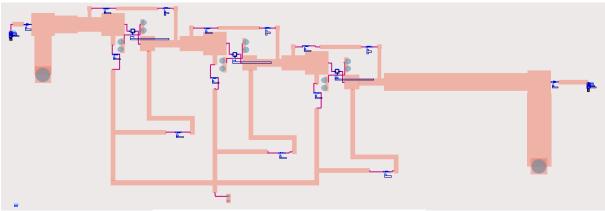


Figure 4.21: Import layout of 3 stage LNA

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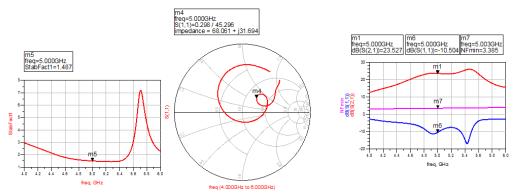


Figure 4.22: result of simulation 3stage layout LNA

parameter	1 <sup>st</sup> stage	3 <sup>rd</sup> stage
Gain (S2,1)	7.297dB	23.527dB
Return loss (S1,1)	-30.078dB	-10.504dB
NF min	2.864	3.385
Impedance matching	52.178+j2.349	68.061+j31.694
Stability factor	1.160	1.487

Table 4.23: Comparison table between 1<sup>st</sup> stage and 3<sup>rd</sup> stage negative feedback LNA layout

Before, we already simulate and tuning to make the best result in 4.4.1 and 4.4.2. Now, in layout simulation there will be varying of result because of some factor. In layout we need to consider every part of the circuit because from layout we will fabricate the LNA. Usually people will add some of the microstrip line (MLIN,MCORN & MTEE) to fulfil the design because in the schematic is not ideal and not possible to fabricate with the design. From schematic, we will generate the layout. Then we will adjust the layout follow the schematic drawing. The gap is already determined from the schematic drawing. In amplifier case, we have active component to be consider. Because of that, the gap is exist in order to place the component after fabricated the layout. Usually, other than amplifier design they can simulate the layout and get the momentum result. But, in LNA we need to import the layout to the schematic and place the active component from the palette. After complete the circuit, the result can be done by simulate like usual.

From the observation above, we can see that the 3-stage LNA result 3x higher in gain compared to 1-stage but the return loss shows drawback. The noise figure also quite higher compare to schematic simulation.1-stage LNA circuit shows a good impedance matching than 3-stage because nearest to 50ohm. Both LNA shows a stable circuit where the K>1.

## 4.6 Fabrication and Measurement

The file from ADS software is taken to Coral Draw software con figure for milling and fabrication process. After checking all dimensions and final adjustment, the fabrication was done by using machine provided in PSM laboratory in FKEKK UTeM. After milling and drilling and plating processes, the LNA is completed by adding the test port SMA connectors for measurements. The dimensions of fabricated LNA are 6x3cm for 1-stage and 8x3 cm for 3-stage. After fabrication process, the LNA is measure by using Agilent Network Analyzer.

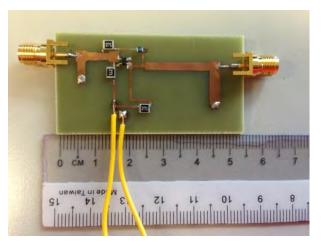


Figure 4.24: Fabricated 1-stage LNA

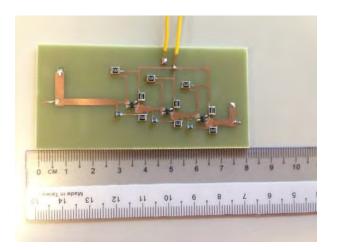


Figure 4.25: Fabricated 3-stage LNA

In order to test the device low noise amplifier which are using Agilent Network Analyzer to determine the S-Parameter. To testing the device should be the voltage input is given 5VDC to protect the design of the LNA excessive current draw due to layout circuit. Before use the analyzer, calibration must be done.

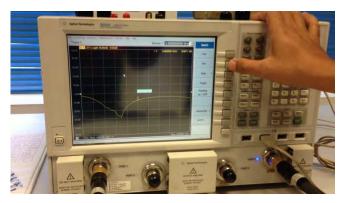


Figure 4.26: The measurement of the LNA performance using Network Analyzer

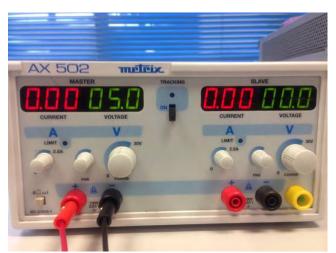


Figure 4.27: Voltage Input 5V DC for biasing circuit



Figure 4.28: The S-parameter measurement results for 1stage



Figure 4.29: The S-parameter measurement results for 3stage

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## 4.7 Debugging and Final LNA Measurement

Initial result showed that the return loss needs improvement (Fig.) Main reason appeared that the LNA was not well grounded on the side edges in the beginning, vias were not well filled with conducting paste. Moreover, we deal with the SMD component which very small in size. The normal soldering tools is not suitable for SMD type. Maybe human error while solder causes the measurement to be different from simulation.

As we can see there is no gain in the measurement. After meeting with supervisor, I have found the mistake of my soldering. The FET may be short because of the debugging while soldering. I am using iron clamps to hold the FET but not covering my hand. So my body becomes electrostatic static discharge make the component short.

In the design, via diameters are modelled die to the smallest vertical linewidth as in 0.7mm. Then, all the shunt linewidths came with a via at the end. During the milling process, there has to be ground holes as vias at the ground parts of the LNA. The smallest pin of the drilling tools roughly around 0.7mm so all the vias and ground holes are milled with that pin to make the diameters as exactly 0.7mm. That can cause some performance errors in measurement. A tuning would help improve the performance.

# CHAPTER 5

## CONCLUSION

# 5.1 Conclusion and Future Network

As a conclusion 5GHz frequency formally is unique in that, in all cases, the authorized unlicensed spectrum spans several GHz which in cover for WLAN application. Furthermore, it's a new spectrum that been used to avoid a crowd in 2.4GHz spectrum.

In order to design LNA, the transistor that are using is ATF-54143 which is commonly cover from 450MHz till 6GHz. This transistor has good features in Avago Technologies. From the simulation, the parameter that have been target is achieved which is noise figure less than 2.5dB, gain more than 4dB and return loss is less than -10dB. The simulation is at 5GHz.

For input output matching determine by using Zopt to get the best noise figure. Then, using microstrip line tools determine the layout for the LNA. This LNA project is using a feedback method which can increase the amplification. The feedback reduce distortion in the amplifier elements and also provides outstanding performance for 5GHz frequency.

For the future works, the design must compare with other type of method to designing the low noise amplifier such as balanced method. In addition, use several methods for matching and analyse which is better matching. Then, choose the best performance and fabricate it.

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# APPENDIX A

# ATF-54143

Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package

Data Sheet

### Dectiption

Nage: Tachnologini: ATF 64142 st a bigh dynamic ramps, true minu, 5 (MdM) Account in a 4 (sad. SC 70 (SCF 042) surface mount plants peckage:

This combination of high gain, high levanity and fow noise makes the ATE-54140 ideal for unlider PCS been stations. WWO's and other optients in the 832 MHz to 8 GHz hispannay range.

### Surface Mount Package 507-543



**Fin Connections and Package Marking** 

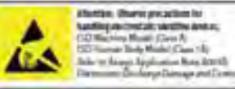


Sec.

Top Years Parkage meeting provides committed, and all with series

14"-Same Data 14" - Gam palls American

Antonio i pedeca.



#### Teatures

- High Enuirity partornamia
- Enhancement Mode Technology77
- Low second dyars
- Explain uniformity in penduat specifications
- + BTE micron gale width
- Low cost surface meant study plants: package 30<sup>o</sup> s 61 (4 load SC 70<sup>o</sup>
- Tape and Risk packaging option evaluates
- Last fear option analable.

### Specifications

- 3 Gitz IV. AdmA (1yp.)
- 36.2 dline bulgsak (Pf sector emiscope)
- 31.4 dBm output power at 1 dB gas comprise
- · hi filmealipre
- MLA-dill associated gen

### Applications

- Low major amplifies for califiliar PCS have stations.
- LNA for IM.AN, WLL/RLL and MMCN applications
- Constal purpose discrete E PEEMI for other ultra low resea application

 Jonanna versk schedug report port Vg. Involucleaning the number for regime part veltage successful with transmission by the second brand.

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Avago

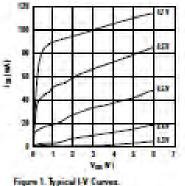
Sec.

ATE-54143	Absolute I	Vaximum	Ratings <sup>[1]</sup>

Symbol	Parzmeter	Units	Abseluto Maximum
Vos	Drain - Source Voltage [7]	V	5
Vcz	Gata - Source Voltage <sup>[2]</sup>	V.	5101
Voza	Gate Drain Voltage [2]	v	-5 to 1
los	Drain Current <sup>(2)</sup>	mA	120
Pala	Total Power Dissipation(7)	mW	725
Pinmax, (ON mode)	RF Input Power (Vids-3V, Ids-60mA)	dBm	20 [3]
Pinmas (OFF mode)	RF Input Power (Vd=0, Ids=0A)	dBm	20
1 <sub>25</sub>	Gate Source Current	mA	215
T <sub>CH</sub>	Channel Temperature	Ϋ́C	150
Tsats	Storage Temperature	1	-65 to 150
Bje	Thermal Resistance (4)	"CAW	162

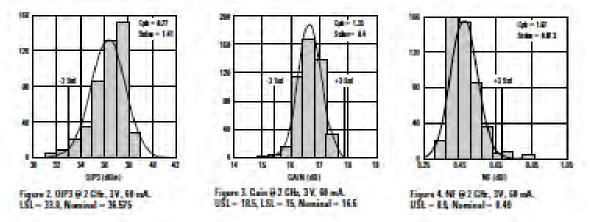
Notes:

- Operation of this device in excess of any one of these parameters may cause permanent damage.
- 2. Anomen DC quiescent conditions.
- 3. Source lead temperature is 25°C. Denote 6.2 mW\*C for Tt > 35°C.
- Thermal resistance measured using 150°C Liquid Crystal Measurement method.
- The device can handle +30 dBm RF input Power provided ligg in firmled to 2 mA. Igg at Prag drive Intel is bias circuit dependent. See application section for additional information.





### Product Consistency Distribution Charts 16, 7]



Notence

- Distribution data sample size is 450 samples takes from 9 different waters. Future waters also and to this product may have nominal values anywhere between the upper and lower limits.
- Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a makenable match based on production test oppipment. Circuit losses have been de-embedded from actual measurements.

### ATF-54143 Electrical Specifications

TA = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameter and Test (	ondition		Units	Min.	Typ.[2]	Max.
Vqs	Operational Gate Voltage Threshold Voltage		Vds = 3V, kds = 60 mA	Ŷ	0.4	0.50	0.75
Vth			Threshold Voltage Vds = 3V, lds = 4 m/	Vds - 3V, kds - 4 mA	V	0.18	0.38
idss.	Saturated Drain Current		Vds = 3V, Vgs = OV	μA	-	1	5
Gm	Transconductance		Vds = 3V, gm = Aktss/AVgs; AVgs = 0.75-0.7 = 0.05V	mmho	230	410	560
igas.	Gate Leakage Curre	at	Vgd – Vgs – -3V	μA		-	200
NF	Note Figure <sup>[1]</sup>	f = 2 GHz f = 900 MHz	Vds = 3V, lds = 60 mA Vds = 3V, lds = 60 mA	dB dB	-	0.5 0.3	0.9
64	Associated Gain <sup>[1]</sup>	f = 2 GHz f = 900 MHz	Vds = 3V, lds = 60 mA Vds = 3V, lds = 60 mA	dB dB	15	16.6 23.4	18.5
CIP3	Output 3rd Order Intercept Point <sup>(1)</sup>	f = 2 GHz f = 900 MHz	Vds = 3V, lds = 60 mA Vds = 3V, lds = 60 mA	dBm dBm	33	36.2 35.5	-
PldB	1dB Compressed Output Power <sup>[1]</sup>	f = 2 GHz f = 900 MHz	Vds = 3V, lds = 60 mA Vds = 3V, lds = 60 mA	dBm dBm	_	20.4 18.4	-
		and the second	and the second				

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1. Measurements obtained using production set board described in Figure 5.

2. Typical values measured from a sample size of 450 parts from 9 wafers.

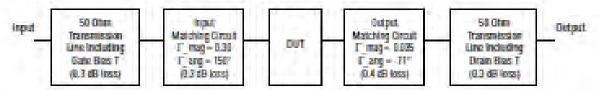


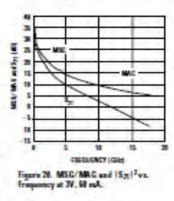
Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Associated Gain, P1dE, and OIP3 measurements. This circuit represents a trade-off between an optimal noise match and associated impedance matching diruit losses. Circuit issues have been de-embedded from actual measurements.

Freq.	5	in.		Sm		St		S21	1	NSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	48
0,1	0.99	-18.9	28.84	27,66	167.6	0.01	80.0	0.54	-14.0	34.42
0.5	0,81	-80.8	26.04	20.05	128.0	0.03	52.4	0.40	-58.8	28,25
0.9	0.71	-117.9	22.93	14.01	106.2	0.04	41.8	0.79	-83.8	25.44
1.0	0.69	-124.4	22.24	12.94	102.2	0.05	40.4	0.27	-88,5	24.13
1.5	0.64	-149.8	19.40	9.34	86.1	0.05	36.1	0.21	-105.2	22.71
1.9	0.62	-164.9	17.66	7.64	75.6	0.06	33.8	0.17	-1147	21.05
2.0	0.62	-168.3	17.28	7.31	73.3	0.06	33.3	0.17	-117.0	20,86
2.5	0,60	176.2	15.58	6.03	61.8	0.07	30.1	0.13	-129.7	19.34
3.0	0,60	162.3	14.15	5.10	51.0	80.0	26.5	0.11	-146.5	18.04
4.0	0.62	137.1	11.81	3,90	30.8	0.09	17.1	0.10	165,2	14.87
5.0	0,66	115.5	9.87	3.11	11.7	0.11	6.B	0.14	131.5	13.27
6.0	0.69	97.2	8.77	2.58	-6.4	0.12	-3.9	0.18	112.4	11.72
7.0	0.70	80.2	6.85	2.20	-24.0	0.13	-15.8	0.20	94.3	10.22
8.0	0.72	67.2	5.58	1.90	-41.8	0.14	-28.0	0.23	70.1	9.02
9.0	0.76	45.0	4.40	1.66	-59.9	0.15	-39.6	0.29	50.6	8.38
10.0	0.83	28.4	3.06	1.42	-78.7	0.15	-55.1	0.38	36.8	8.71
11.0	0.85	13.9	1.60	1.20	-95.8	0.15	-68.6	0.46	24,4	7.55
12.0	0.88	-0.2	0.43	1.05	-111.1	0.15	-80.9	0.51	11.3	7.55
13.0	0.89	-14.6	-0.65	0.93	-128.0	0.15	-949	0.55	-52	6.70
14.0	0.88	-30.6	-1.98	0.80	-146.1	0.14	-109.3	0.61	-20,8	5.01
15.0	0.88	-45.0	-3.67	0.66	-162.7	0.13	-122.9	0.66	-35.0	3.73
16.0	0.88	-54.5	-5.37	0.54	-176.6	0.12	-133.7	0.70	-45.8	2.54
17.0	0.88	-67.5	-6.83	0.46	171.9	0.12	-143.2	0.73	-56.1	1.57
18.0	0.92	-73.4	-8.01	0.40	157.9	0.11	-156.3	0.76	-68.4	7.72

ATF-54143 Typical Scattering Parameters, Vos = 3V, Ios = 60 mA

### Typical Noise Parameters, Vos = 3V, los = 60 mA

Freq	Fair	Fopt	Fapt	R <sub>av'so</sub>	6.
GHz	dB	Mag.	Ang.	200	dB
0.5	0.15	0.34	42.3	0.04	28,50
0.9	0.20	0.37	62.8	0.04	24.18
1.0	0.22	0.37	67.6	0.04	23,47
1.9	0.42	0.27	116.3	0.04	18,67
2.0	0.45	0.27	120,1	0.04	18,29
2,4	0.52	0.26	145.B	0.04	16.65
3.0	0.59	0.29	178.0	0.05	15.56
3.9	0.70	0.36	-145.4	0.05	13.53
5.0	0.93	0.47	-116.0	0.10	12.13
5.8	1.16	0.52	-98.9	0.18	11.10
6.0	1.19	0.55	-96.5	0.20	10.95
7.0	1.26	0.60	-77.1	0.37	9.73
8.0	1.63	0.62	-56.1	0.62	8.56
9.0	1.69	0.70	-38.5	0.95	7.97
10.0	1.73	0.79	-21.5	1.45	736



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 Fmin values at 2 GHz and higher are based on measurements while the Fmins below 2 GHz have been extrapolated. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.

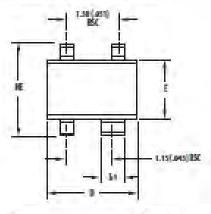
S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumine carries. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameters via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

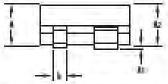
7

### **Ordering Information**

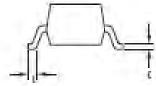
Part Number	No. of Devices	Container
ATF-54149-TRIG	3000	7" Roal
ATT-5414G-TR2G	10000	13'Beat
ATF-54143-BLKG	100	antistatic bag

## **Package Dimensions** Outline 43 (50%-343/5C70 4 lead)

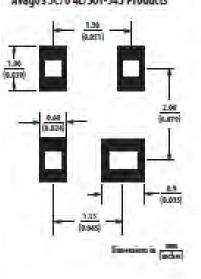




SIMBOL	OIMEKSIONS (mm)	
	MIN.	MAX.
6	1.15	1.35
	1.45	2.25
HE .	1.80	2,40
1	0.00	1.10
42	9.56	1.00
41	90.09	0,10
	0.15	0.40
1	0.55	0.70
. 4	0.01	0.20
	6.16	2.46



**Recommended PCB Pad Layout for** Avago's SC70 4L/SOT-343 Products



STE:

- 1. All dimension are in mo
- 2. Supervises are inclusive of old b
- 1.5 AND AND BRANCH na Al
- 4. All specifications comply to BAUSC20. 5. The straining up for model and facing do fertin
- 1. In a facing up for an in: reverse tab
- 5. Package metace to be mirror finish.