

# UNIVERSITI TEKNIKAL MALAYSIA MELAKA DEVELOPMENT OF AUTOMATIC LOAD-SHEDDING STRATEGY FOR STAND-ALONE PHOTOVOLTAIC SYSTEM

## MASHITAH BINTI MOHD FARITH

**Bachelor of Electrical Engineering** 

(Power Electronic And Drives)

**June 2014** 

" I hereby declare that I have read through this report entitle "Development Of Automatic Load-Shedding Strategy For Stand-Alone Photovoltaic System" and found that it has comply the partial fulfillment for awarding the degree of Bachelor of Electrical Engineering (Power Electronic and Drive) "



# DEVELOPMENT OF AUTOMATIC LOAD-SHEDDING STRATEGY FOR STAND-ALONE PHOTOVOLTAIC SYSTEM



Faculty of Electrical Engineering UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2013/2014

I declare that this report entitle "Development Of Automatic Load-Shedding Strategy For Stand-Alone Photovoltaic System" is the result of my own research except as cited I the reference. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : ...... Name : Miss Mashitah Binti Mohd Farith Date : ...... اونيون سيني نيڪنيڪل مليسيا ملاك UNIVERSITI TEKNIKAL MALAYSIA MELAKA

#### ACKNOWLEDGEMENT

Alhamdulillah, many thanks to Allah, with His permission I complete my PSM2 successfully. Thanks to Allah for blessing me and for ease my way to complete this report. I would like to express the deepest appreciation to my supervisor, Mr. Mohamad Na'im bin Mohd Nasir for guiding, supervising and advising me along the completion of this report.

I would like to express my deepest gratitude to both my beloved father and mother who raised me well with loves and support. Thank you for giving me support, advise and also money to complete this report. One day, your kindness will be repay.

Last but not least, thank you to all my friend for giving me important information in completing the report. The supports from all of you are so unforgettable. Great thanks to all.



## ABSTRACT

Nowadays, the use of solar energy are extremely developed and delivered worldwide. This project presents the development of automatic load-shedding strategy for stand-alone photovoltaic system. The design of this project shows the characteristics of solar energy and operation of load-shedding strategy. The main objective of this project is to implement the load-shedding strategy as an emergency controller for stand-alone photovoltaic system. To achieve the objective, research of basic understanding related to this project is very important to understand more about the characteristics of each element in this project. The circuit of the load-shedding system is designed in the SoftCad Eagle PCB Design software. The algorithm controlling the load-shedding scheme is developed in the Arduino IDE. Then, the coding programmed is burn in the microcontroller board and installed with the hardware. Output of this project can support the DC loads and load-shedding strategy scheme is performed based on the designed algorithm.

, ahun

**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

### ABSTRAK

Pada masa kini, penggunaan tenaga solar adalah sangat maju dan tersebar di seluruh dunia. Projek ini membentangkan pembangunan strategi catuan beban secara automatik untuk sistem photovoltaic bersendirian. Reka bentuk projek ini menunjukkan ciri-ciri tenaga solar dan operasi strategi catuan beban. Objektif utama projek ini adalah untuk melaksanakan strategi catuan beban sebagai pengawal kecemasan untuk sistem photovoltaic bersendirian. Untuk mencapai matlamat tersebut , penyelidikan pemahaman asas yang berkaitan dengan projek ini adalah sangat penting untuk memahami lebih lanjut mengenai ciri-ciri bagi setiap elemen dalam projek ini. Litar sistem catuan beban telah direka dalam perisian SoftCad Eagle PCB Design. Algoritma mengawal skim catuan itu diprogramkan dalam perisian IDE Arduino . Kemudian, pengekodan yang diprogramkan telah dimuat turun ke dalam papan pengawal mikro dan dipasang dengan perkakasan. Pengeluaran projek ini boleh menyokong beban DC dan skim strategi catuan beban dilakukan berdasarkan algoritma yang direka.

بۆمرسىتى تېكىنىكل مليسيا ملا

**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

## TABLE OF CONTENT

CHAPTER	TITLE			PAGE
	ACKN	OWLEDGEMENT		i
	ABST	ACT		ii
	TABL	OF CONTENT		iv
	LIST (	F TABLES		vi
	LIST (	F FIGURES		vii
	LIST	<b>F ABBREVIATIONS</b>		viii
	LIST (	F APPENDICES		ix
		AK		
1	INTRO	DUCTION		1
	F 1.1	Project Background		1
	·***************	Problem Statement		2
	1.3	Objectives		3
	سها ملاك	Scope of Research	اوىيۇم سىتى تىھ	3
_	1.5	Report Outlines		4
L	JNIVERSI	TEKNIKAL M	ALAYSIA MELAKA	
2	LITEF	ATURE REVIEW		5
	2.1	Introduction		5
	2.2	Photovoltaic System		5
		2.2.1 Definition		5
		2.2.2 Configuration		6
		2.2.3 Operation		8
	2.3	Stand-alone Photovoltai	ic System	10
		2.3.1 Definition		10
		2.3.2 Configurations		11
	2.4	Load-shedding Strategy	7	12

		2.4.1 Definition	12
		2.4.2 Load-shedding Techniques	13
	2.5	Microgrid Islanded System	18
		2.5.1 Definition	18
3	DESIG	SN METHODOLOGY	20
	3.1	Project Methodology	20
	3.2	Circuit Components and Design	23
	3.3	Arduino Hardware and Programming	28
4	RESU	LTS AND DISCUSSION	32
	MA4AYS	Introduction	32
	4.2	Multiple AC-DC Power Adaptor Test Results	32
	4.3	Solar Panel Test Results	36
	۲	4.3.1 Experiment 1 (Morning Session)	36
	II.S.	4.3.2 Experiment 2 (Afternoon Session)	38
	& JAINO	4.3.3 Experiment 3 (Evening Session)	41
	4.4	Combination of Multiple AC-DC Power Adaptor and Solar	
	سیا مالاک	Panel Test Results	43
5	UNIVERSI	LUSION AND RECOMMENDATION	48
	5.1	Conclusion	48
	5.2	Recommendation	49
REFERENC	ES		50
APPENDICE	ES		54

## LIST OF TABLES

TABLE	TITLE	PAGE
4.1	Multiple AC-DC Power Adaptor Test Results	33
4.2	PV Supply Experiment 1 Results	37
4.3	PV Supply Experiment 2 Results	39
4.4	PV Supply Experiment 3 Results	41

4.5 Combination of Multiple AC-DC Power Adaptor and PV Supply Test Results 44



**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

# LIST OF FIGURES

FIGURE	TITLE	PAGE
2.1	Solar Cell Structure And Energy Band	7
2.2	Basic Construction Of PV Systems	9
2.3	Basic Structure of Semiconductors	10
2.4	Stand-Alone PV System With DC And AC Loads	12
2.5	Frequency Response Model	15
2.6	Example of Q-V Nose Curve	16
2.7	Example of P-V Nose Curve	17
2.8	Microgrid Architecture, Comprising MS, Loads and Control Device	19
3.1	Project Methodology	22
3.2	Block Diagram of the System	23
3.3	Schematic Diagram of the System	25
3.4	PCB Layout of the System	27
3.5	Arduino Uno Microcontroller Board	29
3.6	Flow Chart of Load-Shedding Operation	31
4.1	Graph of Multiple AC-DC Power Adaptor Test Results	34
4.2	Graph of PV Supply Experiment 1 Results	38
4.3	Graph of PV Supply Experiment 2 Results	40
44	Graph of PV Supply Experiment 3 Results	42
4.5	Graph of Combination of Multiple AC-DC Power Adaptor and	
	PV Supply Test Results	45
4.6	Result of No Load was Shed Condition	46
4.7	Result of One Load was Shed Condition	46
4.8	Result of Two Loads were Shed Condition	47
4.9	Result of Three Loads were Shed Condition	47

# LIST OF ABBREVIATIONS

PV	-	Photovoltaic
PCB	-	Printed Circuit Board
DC	-	Direct Current
AC	-	Alternating Current
Si	-	Silicon
V	-	Volt
А	-	Ampere
W	- the	Watt
MOSFET	KINI	Metal Oxide Semiconductor Field-Effect Transistor
LED	E .	Light Emitting Diode
SRAM	I-I-S	Static Random Access Memory
EEPROM	- 43	Electrically Eraseable Programmable Read-Only Memory
I <sub>SENSE</sub>	2101	Sensed Current
V <sub>SENSE</sub>		Sensed Voltage
$V_{in}$	UNIV	Input Voltage

# LIST OF APPENDICES

APPENDIX	TITLE	PAGE
А	Gantt Chart	54
В	Arduino Coding	55
C	Data Sheet	58



**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

### **CHAPTER 1**

#### **INTRODUCTION**

## 1.1 Project Background

The level of demand for electricity is very high as it is human necessities of life either during day time or night. Most of human daily routines such as work, economy, livelihood, healthcare and leisure depend on a constant power supply. Thus, even a temporary power failure can cause chaos, financial loss, and possible loss of life. There are several unexpected causes of power failure such as natural causes like weather, short circuit, components broken and others. However, in this modern day life, a lot of precaution steps are designed and implemented on the grid system to overcome the power failure. The islanded microgrid operation is one of the methods to keep certain places to receive power supply. This operation is supported by load-shedding scheduling which keeping the power system stability by turn off some of the loads. For this project, the application of load-shedding strategy for islanded microgrid system during power outages is implemented in a small scope where photovoltaic (PV) technology is used as a power supply. PV systems are low maintenance, provide a cleaner, environmentally friendly alternative, and very reliable source of power. It is often used as a back-up for the grid system or operates independently without grid connection. Successful stand-alone systems generally take advantage of a combination of techniques and technologies to generate reliable power, reduce costs, and minimize in convenience. Therefore, this stand-alone PV system will supply several loads and to keep the system balance, load-shedding strategy will be implemented in this system.

## **1.2 Problem Statement**

As the demand of electricity has increase throughout the decade, the failure of power system will affect the daily routines. Therefore, the methods to overcome power outages are developed and delivered worldwide such as the usage of solar energy, wind energy and biofuels energy as a back-up system. However, another issue has come out, there is a rising interest on their impacts on power system operation and control as they have low reliability and flexibility. For this project, a PV stand-alone system is installed to supply several loads. At a certain time, power generated by the PV might be low than the power consumed by the loads due to the variation of irradiances level. At this moment, the power consumed by the loads will not be at rated value and make the power demand higher than power supply. Therefore, the load-shedding strategy is applied to the system to give the maximum power to the loads. The algorithms for the load-shedding will be determined based on the load demand and acceptable power range from PV. The number of load to be shed is important to ensure the stability of energy conservation.

# **UNIVERSITI TEKNIKAL MALAYSIA MELAKA**

## 1.3 Objectives

The aims of this project are as follow:

- 1. To design automatic load-shedding strategy for stand-alone photovoltaic system.
- 2. To develop the algorithms to control the load-shedding operation.
- 3. To study the energy conservation between load and supply under variation of conditions.

## **1.4** Scope of Research

This project primarily focuses on three parts; which are the type of PV system, the strategy for load-shedding and type of load. In this project, the system designed is stand-alone PV system without connection of energy storage. Other than this type of PV system is not included in this project. This project performs only on the implementation of hardware. The circuit of hardware is designed by using SoftCad Eagle PCB Design software while the programming is developed by using Arduino IDE. The algorithms developed for load-shedding will be determined based on the load demand and the acceptable power range from PV. Furthermore, this project use number of lighting as a DC loads. This project will not cover the AC loads. This project is implemented as a prototype of load-shedding strategy for islanded microgrid operation after power failure is covered.

## 1.5 Report Outlines

- 1. Chapter 1 An introductory of the project consisting of the project problem statement, objectives, and scope.
- Chapter 2 Collection of theories that can be formulated and implemented in the project. Reviews of literatures from various sources that can be related to the project research and development.
- Chapter 3 Description of design methodology for the project development and progress.
- 4. **Chapter 4** Results of the project progress is described and the analysis of the results are discussed.
- Chapter 5 The conclusion and recommendation on the final stages of the project development.

## **CHAPTER 2**

## LITERATURE REVIEW

## 2.1 Introduction

MALAYS

Review related to this project are really important to have more understanding on research subject. Therefore, literature review from various sources of information such as technical report, books and journals for related topics are referred. In this chapter, the theory or basic principle of elements covered in this project are discussed. This includes fundamental characteristics, their functions, advantages and many more. For this project, the element or system developed are stand-alone photovoltaic system and load-shedding strategy.

## 2.2 Photovoltaic System

## 2.2.1 Definition

Genuinely, PV entail the process regarding the conversion of the radiant energy from the sun (solar energy) directly into the electricity [1]. Since the solar energy is the most abundant energy source on the planet, photovoltaic system can be classified as a vital technology that needs to be explored extensively in order to preserve our planet. PV sources can provide power supply to from the small electronics to homes and large commercial businesses. PV systems consist of various type of configuration such as grid connected PV system, direct PV system, stand-alone PV system and hybrid system [2].

## 2.2.2 Configurations

A PV cell is normally consists of a semiconductor diode whose p-n junction is exposed to light. Nowadays, most of PV which are more than 90% of them, are manufactured from Si modules constructed from small 4-12 inch crystalline or multicrystalline wafers [3]. Basically photovoltaic cell is made from several types of semiconductor such as monocrystalline and polycrystalline silicon cells. Silicon PV cells are composed of a thin layer of bulk Si or a thin Si film connected to electric terminals. One of the sides of the Si layer is doped to form p-n junction. A thin metallic grid is placed on the Sun-facing surface of the semiconductor [4].

The traditional Si solar cell is a homo junction device. It might have a p-type base with an acceptor (typically boron or aluminum) and a diffused n-type window/emitter layer (typically phosphorus). The Fermi level of the n-type side will be near the conduction (valence) band edge so that donor-released electrons will diffuse into the p-type side to occupy lower energy states there, until the exposed space charge (ionized donors in the n-type region, and ionized acceptors in the p-type) produces a field large enough to prevent further diffusion. To produce a back surface field (BSF) for hole collection and rejects the electrons, a very heavily doped region is used at the back contact. Figure 2.1 indicates the typical construction of the semiconductor part of a Si cell.



Figure 2.1: The Diagram Of Solar Cell Structure And Energy Band [3]

Most of the PV panels are covered with an aluminum frame around the edge, with the size about 600 mm wide, 1200 mm tall and 25 mm thick. These panels are combined together to form a PV array. The crytalline-type panel are the most efficient which operates at about 25% efficiency by maintaining the cool temperature. These type of panels are created from crystalline silicon cells which covered by a grid of wire to aid the electrical energy flow to the terminals. Besides that, there are cheaper PV panels compare to crystalline panels called thin film technologies panels. Material like amorphous silicon can be applied as a film without the need for a glass covering such as glass or plastic. However, the efficiency of thin film technologies panel is about 10% which is much lower than crystalline [5].

Some of PV systems need an inverter and batteries as one of the equipments, depend on the system requirement. The inverters are used to convert the DC value of

PV panels to AC value for AC system. The batteries are mostly needed for stand-alone PV systems which the place is not provided with connection to the electricity grid. These batteries keep the electrical power as a back-up when the PV panels cannot manage to supply adequate electricity. The grid connected systems need a metering system to calculate the amounts of electricity comes from the grid and also from the PV.

## 2.2.3 Operation

MALAYSIA

PV generates electricity by converting it directly from solar radiation through an electronic process that occurs in certain types of material called semiconductor. Solar energy release the electrons in these materials and can be induced to travel through an electric circuit which then powering electronic devices or supply electricity to the grid [6].



Figure 2.2: Basic Construction Of PV Systems [8]

The photons energy from the sun strike and ionize the semiconductor material causing the electrons have high energy to break free of their atomic bonds. Then, the electrons are forcely move in one direction which create a flow of electric current [7]. The layers are placed within the cell opposite charges to prevent the negatively charged electron return to positively the positively charged holes. However, the electrons can move back to the positively charged holes by flowing through the external circuit, thus causing the electricity to flow [8].

The 'p' and 'n' types of semiconductor which are similar to 'positive' and 'negative' because of their plenty of holes or electrons are sandwiched together [9]. When the p-type and n-type semiconductors are joined together, the extra electrons in the n-type material move to the p-type, and the holes thereby empty during this process move to the n-type. These two semiconductors act as a battery since there is flow of hole and electron, thus creates an electric field at the surface where they clash (junction). Figure 2.1 illustrates the detail of electron and hole at n-layer and p-layer.



Figure 2.3: Basic Structure of Semiconductors [9]

The rate of electric carriers generation depends on the flux of incident light and the capacity of absorption of the semiconductor. The capacity of absorption depends mainly on the semiconductor band gap, on the reflectance of the cell surface (that depends on the shape and treatment of the surface), on the intrinsic concentration of carriers of the semiconductor, on the electronic mobility, on the recombination rate, on the temperature, and on several other several factors [4].

## 2.3 Stand-alone PV System

## 2.3.1 Definition

Stand-alone PV systems is designed to operates independently, not involving with electricity grid connection [10]. These system can be powered by PV generator alone or combine with utility source as an additional source such as wind and engine-generator and these system are called PV-hybrid system. PV system is designed either to supply the AC load or DC load or both with the aids of appropriate components [11].

Stand-alone PV system is used worldwide and it is the most popular system compare to other PV system. Stand-alone PV system mostly installed to a totally mains-isolated application as the energy provided is enough to power the application [12]. The installation of stand-alone PV system is not only popular in the town area, besides that it is also popular in the remote rural area [13]. Especially the remote locations where the connection to the electricity grid is either not possible or expensive. They are most cost effective when electricity requirements are relatively low. Stand alone systems include a battery bank, inverter, battery charger and a fuel generator set [5].

## 2.3.2 Configurations

Designing the stand-alone PV system configurations needs a confirmation of which components to connect in the system. The components used depend on the type of the loads (AC or DC load, heavy or light), load requirement (critical oc noncritical, reliability, cost), and its geographical location [14]. The additional equipments as a balance of the system and safely transmit the electricity to the load.

The main component in the system is PV array. It will convert the solar energy into electricity. As the energy generation and consumption do not generally coincide, energy storage is required in most stand-alone systems [15]. The solar energy generated during daylight is not fixed, it change depends on the intensity of the sunlight. Energy need to be stored to ensure the stability of the system. Charge controller is important as it consist of DC/DC converter that will take optimum power from PV array and adjust it to the charge voltage of the battery. Inverter is needed when the type of load is AC load. Since the output power drive from PV is in DC, thus inverter converts the DC power to AC power to feed the AC load.



Figure 2.4: Stand-Alone PV System With DC And AC Loads [16]

#### 2.4.1 Definition

Energy efficiency has become an issue debates where several factors may disrupt the effiency of the system such as deregulation of electrical energy distribution, the increasing price of electricity, and the implementation of rolling blackouts [17]. These factors affect the stability of the whole power system. For example when a sudden large industrial load is switched on, it will disrupt the grid system and the system become unstable. Particularly, the differences between the generated power and the load demand caused by disturbance which reduces the generation capacity of the system, thus affect the frequency of the system. The voltages become unstable when the power system unable to meet the reactive power demands of the loads [18].

The stability of the system need to be control where the load-shedding strategy can be an emergency control operation. The load-shedding strategy is designed to curtail the system load during emergency situation to control the stability of the system [19]. The loads are curtailed until the available generation could supply the remain loads. Load-shedding strategy balances the real and reactive power supply and the load demand in the system to prevent from the excessive frequency or voltage decline.

The location bus for the load-shedding will be determined based on the load importance, cost, and distance to the contingency location. The acceptable algorithms are developed based on the number of LS steps, amount of load that should be shed in each step, the delay between the stages, and the location of shed load.

#### 2.4.2 Load-shedding Techniques

An automatic load-shedding for power system using different schemes such as under frequency, under voltage and combinations of the two can be employed to avoid frequency or voltage collapse during a significant imbalance between generation and load [19]. These types of load-shedding methods are very dependant on offline studies of the system's dynamic performance and only consider the greatest probable imbalance between generation and load. These methods have to coordinated with the protections of the generating units, shunt capacitors and other automatic actions that occur in the system during frequency and voltage variations.

## 2.4.2.1 Under Frequency Load-shedding Scheme

The under frequency load-shedding scheme uses relays detecting the system's frequency [20]. These are design to operate on the instantaneous frequency value where they trip when the frequency drops below the set point of the relay. The shedding operation is accomplished in the systems distribution or transmission stations where major load feeders can be controlled by tripping of the circuit breakers (CB) automatically. Different settings can be apply in these load-shedding schemes.

Multiple stages can be use in the scheme [19]. The substation loads are prioritised and grouped according to the importance of the load. The relays can be set to control one or more groups of loads and when there is a frequency drop these can be disconnect sequentially where the group with the highest probability being disconnected the last. Each group disconnected should contribute to the system rate of change of frequency decline. If the load to be disconnected is small compared to the overall imbalance then the contribution will be insignificant and would cause further problems to the systems frequency decline.

Another setting usual for this type of scheme is the time delay [21]. The time may can be required and used usually to avoid any frequency transient dips that could arise in the system. The time delay also avoids unnecessary load shedding by allowing the load or frequency controls in the system to respond to the frequency deviation. However load shedding performed with long time delays should be set appropriately as it will make the system more vulnerable to system stability if eventually load shedding is required. This method will work adequate in a situation where the system frequency decline is slow.



Figure 2.5: Frequency Response Model [19]

## 2.4.2.2 Under Voltage Load-shedding Scheme

Under voltage load-shedding method has been successfully deployed in transmission systems to protect them from voltage collapse [22]. System studies are required to determine which systems are potential candidates for suitable the under voltage load shedding method. This method is most useful in slow decaying systems where the under voltage load shedding relay time relays can coordinated accordingly and operate to alleviate the system from overload conditions and low voltages.

Voltage collapse can be studied using steady state simulations for the identified areas using a power flow analysis. System planning engineers conduct numerous studies using P-V and Q-V as well as other analytical methods to determine the amount of load required to be shed to preserve voltage stability under different disturbances



Figure 2.6: Example of Q-V Nose Curve [22]



Figure 2.7: Example of P-V Nose Curve [23]

There limitation associated with proper application of under voltage load shedding is the location of its application to where the relaying may be appropriately applied. If it is placed on a distribution line the effects of auto tap changers mask a system overload condition from the relay, or alternatively a line switching operation or the startup of a large industrial plant on one feeder could fool the relay. The relay would not be appropriate at locations directly adjacent to generation powerful enough to control bus voltages even during severe overloads. The relay is best applied to locations with fairly stiff voltages under all normal conditions, so a low voltage condition will reliably indicate a severe overload condition, as may be assumed to be the case at large substations associated with bulk power transmission lines and therefore this method cannot be effectively applied in islanded distribution networks where distribution generation unit power and load demand varies.

#### 2.5 Microgrid Islanded System

ALAYSIA

#### 2.5.1 Definition

Microgrid is an low voltage (LV) network for examples a small urban area, a shopping center, or industrial park, which the loads and several small modular generation systems are connected to it. Microgrid provides both power and heat to local loads, combine heat and power (CHP) to the system [25]. Besides that, the small modular generation systems can be referred to systems such as photovoltaic (PV), fuel cells, microturbines (MT), small wind turbines (WT) and storage devices (Fly wheels, super capacitors, batteries, and so on), which are lead to a new energy system paradigm [26].

There are two different operating conditions of Microgrid system. The first one is the Normal Interconnected Mode where the Microgrid is connected to a main MV network, either being supplied by it or injecting some amount of power into the main system [25, 26]. The second one is the Emergency Mode where the Microgrid operates autonomously, in a similar way to physical islands, when the disconnection from the upstream MV network occurs due to planned or unplanned events for examples, maintenance actions or faults in the MV network, respectively. Figure 2.8 illustrates the Microgrid system.

Microgrid can operates either in grid connected or islanded operation mode. In the Microgrid management, it requires the balance between supply and demand of power. The Microgrid exchanges power to an interconnected grid to meet the balance during the grid-interconnected mode. On the contrary, during islanded mode, the microgrid should meet the balance using the decrease in generation or load shedding [27].



Figure 2.8: Microgrid Architecture, Comprising MS, Loads and Control Device



**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

## **CHAPTER 3**

### **DESIGN METHODOLOGY**

## 3.1 Project Methodology

MALAYSI.

This section will discuss on the methods considered to complete this project successfully. The first, most important step is literature review and research on related previous projects, knowledges and informations from the various of information such as journals, technical reports and books. Chapter 2, literature review is important to gain more informations about PV and load-shedding strategy as aids to complete this project. Figure 3.1 shows the flow chart of project methodology.

After gaining a lot of informations related to the project, the circuit and PCB layout for hardware is designed by using CadSoft Eagle PCB Design Software. Then the hardware is setup with two inputs, the first one is multiple AC-DC power adaptor as an utility supply, and the second one is solar panel as a PV supply. After finish setup, the connection will be test for the functional of the system.

The algorithms for controlling the loads which depends on the supply is developed in the Arduino IDE. These algorithms will decide which loads will on depends on the acceptable power range of the supply. This coding must be suitable and can work well when implemented with the hardware.



**Figure 3.1: Project Methodology** 

After the implementation of the coding with the hardware, both will be tested and troubleshoot to ensure either the combination of both hardware and coding fulfill the all the specification of the project and achieve its objectives or fail. When the test is success all the relevant results needed are recorded and discussed. The conclusion of whole project is briefly explained.

## 3.2 Circuit Components and Design



Figure 3.2: Block Diagram of the System

For the whole system, Figure 3.2 briefly illustrates the block diagram of the system. This project is using two supplies, utility supply and PV supply but only one is used at one time. The utility supply is represented by multiple AC-DC power adaptor with rating of 3-12V DC output voltages and 1200mA loading current. The PV supply is from the solar panel with rating of 30W, 18V. Both supplies are connected to a relay where the adaptor is connected to the normally open of relay contactor and PV supply is energized and normally open contact become close therefore, the loads are supplied by the adaptor. Otherwise, PV supply is used to supply the loads if adaptor is off.

A current sensor, ACS712 is connected in series with both supplies to measure the value of currents. Instead of that, voltage divider with resistor value of  $15k\Omega$  and  $4.7k\Omega$  is used to measure the value of voltage supply. Arduino will received both input values from the sensors and calculate the input power. This input power will be used to determined the number of loads to be shed. The coding programmed in the Arduino are based on the algorithms of input power range and will be compared with power demand by the loads. Arduino will execute the program to control the switching devices by deciding which one will be on and which one will be shed.

The switching devices used are p-channel MOSFETs which are activated by transistors. When Arduino gives high input voltage to transistor, the transistor will give low signal to the p-channel MOSFET and activate it. Therefore, the load connected to that MOSFET will be on. The main advantages of using p-channel is circuit simplification in medium and low power applications. Arduino will decide which switching device will either on or off.

Four bulbs with rating 6.3V, 3W are used as loads. These bulbs will be light up when the switching devices are activated. By connecting the adaptor which gives 12V voltage supply, all bulbs will be on. However, when PV supply is on, there will be different number of bulbs that are on. The number of bulbs light up or shed depends on the acceptable power range delivered by the PV source.



## **UNIVERSITITE KNIKAL MALAYSIA MELAKA** Figure 3.3 shows the schematic diagram for the hardware designed in the

SoftCad Eagle PCB Design Software. In the figure, the supplies connections are at the bottom left of the corner which connected with the relay. The NA-10 multiple AC-DC power adaptor manufactured by WINSTAR® is used to supply 12V to the loads. Otherwise, if the power adaptor is not functioning, the solar panel will be the power supply. Maximum voltage that can be accepted by this hardware is 20V. The relay used is K1 G5L and the diode 1N4004 is used to protect the system from coil spike when the relay opens. When voltage is applied to a coil it creates a magnetic field. When the voltage is removed the magnetic field collapses and creates a reverse polarity voltage and can be many times the value of the original applied voltage. This creates a transient voltage pulse that can damage other components in the circuit that

are not rated for this polarity or the higher voltage created, things like semiconductors and caps have a maximum voltage limit and breakdown if exceeded. Having a reversed a reversed biased diode across the coil allows the diode to conduct for reverse polarity voltages and creates a short circuit across the coil that allows the pulse to be dissipated in the resistance of the coil wiring.

The ACS712 is a current sensor used to measure the current from the supply. This current sensor is supplied by the 5V from the Arduino board. LED1 is the indicator for the supply, when supply is on the LED1 will on and the color is red. 5V from the Arduino board will supply the LED1. Resistor 1k $\Omega$  is for the protection. At the top left of the schematic diagram is the Arduino Uno. Uno will received the voltage and current from the supply and gives signal to the outputs based on the coding inside the Arduino. 15k $\Omega$  and 4.7k $\Omega$  is the voltage divider to measure the voltage. The the Arduino. 15k $\Omega$  and 4.7k $\Omega$  is the voltage divider to measure the voltage. The the Arduino National SV to ensure it gives less than 5V to Arduino.

The transistor BC548 and the p-channel MOSFET IRF9540 are the switching devices use to on and off the loads. The resistors are used for biasing. The last connection is the load where four bulbs 6.3Vdc, 3W are used. Figure 3.4 shows the PCB layout of the circuit design.



Figure 3.4: PCB Layout of the System
The boards are made from glass reinforced plastic with copper tracks in the place of wires. Components are fixed in position by drilling holes through the board, locating the components and then soldering them in place. The copper tracks link the components together forming a circuit.

The schematic diagram was first converted into a layout of components pin pads, then traces were routed to provide the required interconnections. Pre-printed nonreproducing mylar grids paper assisted in layout, and rub-on dry transfers of common arrangements of circuit elements helped standardize the layout. Traces between devices were made with self-adhesive tape. The finished layout "artwork" was then photographically reproduced on the resist layers of the blank coated copper-clad boards.

### 3.3 Arduino Hardware and Programming

In the designing stages, several condition in order to design an automatic loadshedding strategy for stand-alone PV system are considered. The characteristics of PV used such as type of PV, power generated by PV and total power consumed by the load are important to set the algorithms for the system. The method for the load-shedding are determined based on the acceptable power range from PV and load demand. Figure 3.5 illustrates the flow of load-shedding operation. The power from the PV is sense and delivered to the Arduino to compare the power of PV,  $P_{PV}$  and power of load demand,  $P_L$  by using developed algorithms.

The Arduino Uno, shown in Figure 3.5 is chosen as the microcontroller board in this project due to its easy to use benefit. The Arduino is open-source, which means hardware is reasonably priced and development software is free. With the Arduino board, programs can be written and interface circuits can be created to read switches and other sensors, and to control motors and lights with very little effort. Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators.

The Arduino Uno can accept input voltage from 6V to 20V, however, the recommended input voltage range is from 7V to 12V. Users must be reminded that if the external supply source supplied to the Arduino Uno is higher than 12V the board may be suffer from overheating problems. There are pins on the board that can provide output voltage of 5V and 3.3V. The processor provides 32 kilobytes of flash memory, 2 kilobytes of internal SRAM and 1 kilobyte of EEPROM. This microcontroller board provides 14 digital pins that can be used as an input or output. They operate at 5 volts. The Uno has 6 analog inputs, labeled A0 through A5, each of which provide 10 bits of resolution (1024 different values).

## MALAYSIA

The Arduino Uno will be combined with the PCB board of the hardware so that the output data from the Arduino can be sent to the switching devices of the hardware. The analog inputs of Arduino Uno are  $I_{SENSE}$  from the current sensor ACS712 at A0 and  $V_{SENSE}$  from voltage divider at A1. The supply for Arduino is 9V from the adapter at V<sub>in</sub> while 5V from the board is supplied to current sensor ACS712 and LED supply indicator. Four digital pins are used as ouputs to connect with the switching devices that control each load.

# **UNIVERSITI TEKNIKAL MALAYSIA MELAKA**



Figure 3.5: Arduino Uno Microcontroller Board

The software used to program the Arduino microcontroller is called Arduino IDE which is available for download from the official Arduino website. Arduino IDE version 1.0.5 is used to write the Arduino codes used in this project. Figure 3.6 shows the flow chart of Arduino programming. When Arduino microcontroller is powered up, it will first read the values from analog inputs where the inputs are current and voltage either from adaptor supply or PV supply. The read values will then be used to calculate the total power draw from the supply by using their respective conversion equation and algorithms.

Rating power for each bulb is 3W which makes the total power for four bulbs are 12W. 12W or more is needed to give maximum power to four bulbs. When there is supply from adaptor, which is 12V, the power supply from adaptor is sufficient enough to support all loads. Thus, all four bulbs will light up when there is supply from adaptor. However, when the adaptor is turned off solar panel will supply all the loads. Because of the power from solar panel is not constant, the load will be shed based on the power range of solar panel.

When the PV supply power more than 12W, all bulbs will be light up. While when the power sensed from PV supply is less than 12W but more than 9W, only three bulb will be light up. Likewise, when the power sensed from PV supply is less than 9W but more than 6W only two bulbs will be light up. When the power sensed from PV supply is less than 6W but more than 3W only one bulb will be light up. When the power sensed from PV supply is too small, no bulb will be light up. Every time the load-shedding operation is done, there will be 5 second delay before the process start over again. Arduino will calculate the power again and do the shedding. This process is repeated until the power supply is off. The full Arduino codes are shown in Appendix.



Figure 3.6: Flow Chart of Load-Shedding Operation

## **CHAPTER 4**

### **RESULTS AND DISCUSSION**

# 4.1 Introduction

MALAYS

This section discusses the results of calibration test results of load-shedding startegy operation using power adaptor and solar panel as power supplies. More importantly, the load-shedding operation is implemented in order to ensure each bulb lighted up in maximum power. Additionally, the full integration of the whole project and screenshots of the project are shown. The load-shedding operation is done in order to give the balance between supply and demand of power.

# 4.2 Multiple AC-DC Power Adaptor Test Results

Previous projects and research are more focus on larger system applied on a grid. However, this project is just a prototype of the control strategies for microgrids islanded operation in a smaller scope, only to show the operation of load-shedding strategy. Therefore, two supplies are used which the power adaptor is used to represent

the system during the normal condition and the PV supply is used to represent the condition during islanded operation when power failure occur.

Power adaptor will give 12V to the system which has sufficient power to accommodate all four loads. The power supplied by the adaptor is depends on the load and the rating for current is 1.2A. Moreover, all bulbs will light up during power adaptor consumption. Nevertheless, in order to make better understanding about the load-shedding strategy, the multiple AC-DC power adaptor is varies in several values, 4.5V, 6V, 7.5V, 9V, and 12V. In the meantime, the value of power also fluctuate consequently affect the loads. The results of this test is represented in Table 4.1, while Figure 4.1 shows the results of loads and power in form of a graph.

X				
F	Voltage (V)	Current (A)	Power (W)	Number of Lighted Bulb
1	7.71	1.93	14.88	4
	7.73	1.96	15.13	4
	7.85	1.96	15.37	4
-	7.85	2.01	15.78	اويوم ميني بيه
	5.99	1.77	10.62	
	5.24	1.56	8.17	ATOK I
	5.22	1.53	8	2
	5.26	1.56	8.2	2
	6.55	1.8	11.77	3
	6.52	1.8	11.73	3
	4.75	0.77	3.65	1
	7.69	2.01	15.45	4
	7.67	2.01	15.41	4
	6.59	1.82	12.02	4
	6.55	1.77	11.6	3

 Table 4.1: Table of Multiple AC-DC Power Adaptor Test Results

MALAYSIA



Figure 4.1: Graph of Multiple AC-DC Power Adaptor Test Results

Based from the results in Figure 4.1, there were changes in the number of lighted bulb linearly towards the changes in the value of power sensed from the supply. When the power is greater more loads can be on, while decrease in power will also decrease the numbers of bulbs light up. The highest power sensed by Arduino is 15.78W which is sufficient enough to light up the four loads. While, the lowest power draws from the supply is 3.65W which can light up only one load.

When the voltage of the supply is maintained in 12V, the power will be more than 12W and thus the power is sufficient to maintain light up four bulbs with maximum power. However, when the voltage is decrease to value of 7.5V, the number of bulbs light up also decreased correspond to the decline in value of power to below than 12W. The same thing happened when the voltage is further decrease to smallest value. This operation worked according to the coding programmed in the Arduino.

The advantage of using the multiple AC-DC power adaptor rating 1200mA, DC 3-12V, is the stability of the power produced by the adaptor. This power adaptor has sufficient power to support all four loads. Common adaptors rating below than 800mA are not stable and sufficient enough to support all four loads. Moreover, the adjustable

voltage range make it easier to test the hardware for observing the load-shedding operation.

Each electronic product must have come with its own drawbacks. Although the supply is set to 12V, 9V, 7.5V, 6V and 4.5V, from the Table 4.1 it can be seen that the higher voltage from the supply is 7.85V which is slightly smaller than the value set (12V) because voltage drop happened when connected to the load of the system. As no electronic products are ideal in the real world, different results will be obtained for other set values, where the values might be slightly smaller or larger from the set values. Therefore, the voltages and currents were sensed ten times and only average values are taken for power calculation as programmed in the Arduino.

Besides that, the power adaptor will be overheated if use it in a long period. The power losses of the adaptor will affect the power supply to the bulbs. During overheated period, the power supplied by the adaptor is unstable. The power draw from the overheated adaptor might be smallest from the normal condition. In normal condition, the 12V supply should give sufficient power to all four bulbs. Nevertheless, because of the power losses due to overheated, the power has become smaller and not enough to supply all bulbs. Therefore, the test should be conducted in normal condition in a short period to prevent overheated.

# **UNIVERSITI TEKNIKAL MALAYSIA MELAKA**

## 4.3 Solar Panel Test Results

The load-shedding stategy operation is tested again by using solar panel as a power supply. PV systems are low maintenance, provide a cleaner, environmentally friendly alternative, and very reliable source of power. However, the power instability of the PV system can affect the performance of the load. Therefore, load-shedding strategy is an efficient control strategy that can minimize the number of loads depends on the available power supply. To illustrates the influences of irradiant and temperature on the performance of the solar panel, the tests were executed with different session.

# 4.3.1 Experiment 1 (Morning Session)

LA

The test was conducted in the morning at 9 a.m. where the wheather is moderate. The power draw from the solar panel is constantly small. The results of this test is represented in Table 4.2, while Figure 4.2 shows the results of loads and power in the form of a graph.

Table 4	.2: Table of H	V Supply E	xperiment 1 Results
Voltage (V)	Current (A)	Power (W)	Number of Lighted Bulb
4.32	0.88	3.78	1
4.34	0.93	4.02	1
4.66	_1.3	6.05	اويية م فيت ت
4.48**	1.06	4.75	
UNIV4.32RSI	TU.77	<b>KA</b> 3.321AI	AYSIA NELAKA
4.48	1.06	4.75	1
4.95	1.46	7.2	2
5.54	1.72	9.53	3
4.58	1.3	5.94	1
4.42	1.09	4.80	1
5.17	1.69	8.76	2
4.75	0.77	3.65	1
5.36	1.69	9.07	3
4.44	1.03	4.59	1
4.32	0.77	3.32	1



Figure 4.2: Graph of PV Supply Experiment 1 Results

Figure 4.2 shows the changes in the number of lighted bulb linearly with the changes in the value of power sensed from the PV supply. From the graph, the powers mostly are small results in the most number of lighted bulb is one only. The maximum number of lighted bulb are three loads which were occured twice. The highest power sensed by Arduino is 9.53W which is sufficient to light up only three loads. While, the lowest power draws from the supply is 3.32W which can light up only one load. The performance of the solar panel is low at this moment as the irradiance of the sun is low at the very moment. It is hardly to produce power more than 9W which can light up three loads not to mention four loads. Thus, more loads need to be shed and from the graph mostly two and three loads are shed because of the deficiency of power.

# 4.3.2 Experiment 2 (Afternoon Session)

The test was conducted in the afternoon at 12.30 p.m. where the wheather is sunny. The power draw from the solar panel is slightly higher than in the morning. The results of this test is represented in Table 4.3, while Figure 4.3 shows the results of loads and power in the form of a graph.

	Voltage (V)	Current (A)	Power (W)	Number of Lighted Bulb
	4.93	1.59	7.82	2
N.	4.89	1.56	7.63	2
TEK	5.32	1.72	9.14	3
1	5.2	1.64	8.52	2
	4.99	1.51	7.53	2
	5.28	1.72	9.07	3
-	5.26	1.67	8.76	اوىيۇم 2يىتى ئىچ
	5.54**	1.72	9.53	3
U	<b>N</b>  \5.62 <b>\S</b>	TI.72	<b>KA</b> 9.67 <b> A</b>	AYSIA BIELAKA
	4.97	1.48	7.36	2
	4.32	0.77	3.32	1
	5.38	1.64	8.82	2
	5.3	1.72	9.11	3
	5.07	1.46	7.38	2
	4.32	0.77	3.32	1

 Table 4.3: Table of PV Supply Experiment 2 Results



Figure 4.3: Graph of PV Supply Experiment 2 Results

The above graph shows the number of lighted bulb and the power generated by PV supply during the sunny afternoon. The correlation between power generated by the PV supply and the number of lighted bulb can be analyzed from the graph. When the power is rised, the number of lighted bulb also increase. During afternoon, the power of PV can reach up to more than 9W because of the high irradiance since it was sunny. Therefore, from the graph it can be seen that the most number of lighted bulb is two and three. This supports the theory that higher irradiances give higher efficiency to the PV supply. When the power is greater more loads can be on, while decrease in power will also decrease the numbers of bulbs light up. The highest power sensed by Arduino is 9.67W which is sufficient to light up the three loads. While, the lowest power draws from the supply is 3.32W which can light up only one load. However, the circumstances where the number of lighted bulb is one, occured twice only. Most of the bulbs light up are about two and three often.

# 4.3.3 Experiment 3 (Evening Session)

The test was conducted in the evening at 5.30 p.m. where the wheather is partly cloudy. The power draw from the solar panel is slightly lower than in the afternoon. The results of this test is represented in Table 4.4, while Figure 4.4 shows the results of loads and power in the form of a graph.

	Voltage (V)	Current (A)	Power (W)	Number of Lighted Bulb
	4.66	1.56	7.28	2
N	4.32	0.88	3.78	1
TEK	4.30	0.80	3.42	1
1	4.79	1.46	6.97	2
	5.03	1.75	8.78	2
	4.85	1.51	7.31	2
-	4.46	1.06	4.73	اوىيۇر پلىتى ئىچ
	5.01**	1.69	8.48	
U	5.99 <b>.</b> 5	TI T1.77 NI	<b>KA10.62 A</b>	AYSIA BIELAKA
	4.34	0.93	4.02	1
	4.62	1.48	6.85	2
	4.34	0.88	3.79	1
	4.93	1.69	8.34	2
	4.87	1.72	9.04	3
	4.87	1.61	7.86	2

Table 4.4: Table of PV Supply Experiment 3 Results



Figure 4.4: Graph of PV Supply Experiment 3 Results

From the graph in Figure 4.4, it can be seen that the average power generated by the supply is in the range of 6.85W to 8.78W where the number of lighted bulb is mostly two. The correlation between power generated by the PV supply and the number of lighted bulb can be analyzed from the graph. The highest power sensed by Arduino is 10.62W which is sufficient to light up the three loads. While, the lowest power draws from the supply is 3.42W which can light up only one load. During the test is conducted, the wheather was partly cloudy. The power is not constant and mostly the power generated can only light up one to two loads. Three loads were rarely light up which occur twice only. The performance of the PV in the evening slightly similar to the prformance of the PV during morning. However, the power generated in the evening is slightly higher than that in the morning. Therefore the number of load shed in the evening is less than in the morning. The variation of power might be influenced by the irradiance and the temperature at the moment. This experiment was conducted using both supplies, power adaptor and PV supply. The experiment is conducted to observe the operation of the system when the power adaptor gave sufficient supply to the loads, however suddenly the power adaptor was off and the PV took over to supply the loads. At this moment, the power from PV might not be sufficient to support the loads, thus the load-shedding strategy operation was executed. Table 4.5 and Figure 4.5 show the result of the system during the usage of power adaptor and PV supply. The operation of load-shedding strategy also can be observed from the table and the graph.

N.	MA		
Voltage (V)	Current (A)	Power (W)	Number of Lighted Bulb
7.61	1.93	14.69	4
7.63	1.90	14.52	4
7.71	1.93	14.88	4
7.73	1.96	15.13	4
7,14	1.93	13.78	اويىۋىرىلىت تىغ
4.89**	1.56	7.63	
UNI\4.66 SI	1.56	<b>KA</b> 7.28 <b>A</b>	AYSIA PELAKA
4.40	1.19	5.24	1
5.32	1.69	9.00	3
5.2	1.64	8.52	2
4.99	1.51	7.53	2
5.26	1.72	9.04	3
4.48	1.46	6.52	2
4.38	1.06	4.64	1
4.62	1.59	7.34	2

 Table 4.5: Table of Combination of Multiple AC-DC Power Adaptor and PV Supply Test

 Results

MALAYSIA

38



Figure 4.5: Graph of Combination of Multiple AC-DC Power Adaptor and PV Supply

**Test Results** 

From the graph in Figure 4.5, it can be seen that from the first data up the fifth data, the loads were supplied by the power adaptor. During that time, the number of lighted bulb is four since the power generated from power adaptor is sufficient to support all four loads. The maximum power generated by the adaptor was 15.13W while the minimum power generated was 13.78W which is still can supply the four loads. Suddenly the number of lighted bulb is decreased to two because at this moment, the power adaptor is turned off and at the same time the PV supply is turned on and supply the loads. The graph shows the variation in number of bulb lighted up that occurred because of the values of power generated by the PV supply are not constant. The values of power are depend on the irradiances and the temperature of the surrounding at that moment. From the graph, when the value of power is drop to 4.64W which is the lower power, the three bulb were shed and only one bulb is lighted up. The maximum number of bulbs than can be lighted up is up to three only with the highest power of 9.04W. The load-shedding strategy operation is continue because the power generated keep increasing and decreasing. The performance of the PV supply is less efficient than power adaptor since the maximum loads that PV supply can supports

are up until three loads. Figure 4.6, 4.7, 4.8, and 4.9 show the hardware test results where no load was shed, one load was shed, two loads were shed, and three loads were shed are shown respectively.



Figure 4.7: Result of One Load was Shed Condition



Figure 4.8: Result of Two Loads were Shed Condition



Figure 4.8: Result of Three Loads were Shed Condition

#### **CHAPTER 5**

#### **CONCLUSION AND RECOMMENDATION**

# 5.1 Conclusions

MALAYS

An automatic load-shedding strategy for stand-alone photovoltaic system was designed using the SoftCad Eagle PCB Design Software for schematic design and PCB layout of the hardware prototype. All the components were set up and the hardware was constructed and tested successfully. The test results show the loads been shed when the power is smaller than the load demands. The load-shedding strategy operation was executed based on the algorithms programmed in the Arduino IDE. The algorithms were developed to control the load-shedding operation by using power parameters. The supplies used are multiple AC-DC power adaptor and solar panel which have different performances. The performance of the PV supply is less efficient than power adaptor since the maximum number of bulb that can be lighted up by the PV was three. While the power adaptor can light up all four loads. Solar panel has different power generated within different time, morning, afternoon and evening. Furthermore, the performance of solar was affected by the irradiances of the sun and the surrounding temperatures. The higher value of temperature gives lower efficiency of the PV systems. However, the irradiant is the factor that would make the PV system more efficient where the higher the value of irradiant, the higher the efficiency of the PV systems. During islanding, the power balance between supply and demand was match at the moment. The results show that the proposed load-shedding scheme can regulate the power supply and the load demand very well. In addition, these results indicate that the load-shedding strategy can contribute to improve the control capability.

## 5.2 **Recommendations**

When using one solar panel, all bulbs might not be lighted up with maximum power. This is because the power generated from one solar panel is small. Therefore, to make the system more efficient, two or more solar panel can be used and combined either in parallel or in series to yield better performance.

This system can be installed not just for power failure condition only but might be design for the normal used during daylight to save energy used from the utility. Utility bills also can be saved from the high cost bills by implement this system in the house and improve the performance for daily use during daylight only.

# **UNIVERSITI TEKNIKAL MALAYSIA MELAKA**

To differentiate between the importance and non-importance load to be shed, the priority of load can be implemented in this system. The load-shedding strategy will be operates on the least important load to the most important load.

#### REFERENCES

- [1] Inc., N. Z. (July 2003). An Introduction To Photovoltaics.
- [2] S. Sopitpan, P. C. (2000). PV Systems With/Without Grid Back-up for Housing Applications. *IEEE Explore*.
- [3] Compaan, A. (n.d.). *Photovoltaics: Clean Electricity for the 21st Century*. Retrieved October 2013, from APS Physics: http://www.aps.org/publications/apsnews/200504/forefronts.cfm
- [4] Marcelo Gradella Villalva, J. R. (2009). Modelling and Circuit-Based Simulation of Photovoltaic Arrays. *IEEE Xplore*.
- [5] Council, A. C. (n.d.). Photovoltaic (PV) Systems. Adelaide City Council Green Building Fact Sheets.
- [6] Solar Energy Industry Association. (n.d.). Solar Technology. Retrieved October 2013, from SEIA: http://www.seia.org/policy/solar-technology/photovoltaic-solar-electric
- [7] Association, S. E. (n.d.). *Solar Photovoltaic Technology*. Retrieved October 2013, from SEIA.
- [8] Renewable Energy Systems Ltd. (2000-2013). How Does It Work? Retrieved October 2013, from PV Systems: <u>http://www.pvsystems.com/about-solar-pv/how-does-it-work.aspx</u>
- [9] Program, U. D. (n.d.). *How A Photovoltaic Cell Works*. Retrieved October 2013, from About.com Inventors: http://inventors.about.com/library/inventors/blsolar3.htm
- [10] Anca D. Hansen, P. S. (December 2000). Models for a Stand-Alone PV System.

- [11] Florida, I. o. (2007). *Types of PV Systems*. Retrieved October 2013, from Florida Solar Energy Center: http://www.fsec.ucf.edu/en/consumer/solar\_electricity/basics/types\_of\_pv.htm
- [12] Luis Castaner, Santiago Silvestre. (March 7, 2003). Standalone PV Systems. In S. S.
   Luis Castaner, *Modelling Photovoltaic Systems Using Pspice* (pp. 180-182). Chichester West Sussex: John Wiley & Sons Ltd.
- [13] Mota, J. A. (2013). A High-Performance Stand-Alone Solar PV Power System for LED Lighting. *ISRN Renewable Energy*.
- [14] Solanki, C. S. (July, 2011). Introduction to Solar PV Systems. In Solar Photovoltaics: Fundamentals, Technologies and Applications (pp. 391-394). New Delhi: Asoke K. Ghosh, PHI Learning Private Limited.
- [15] Society, G. E. (2008). Planning and Designing Stand-alone Systems. In *Planning & Installing Photovoltaic Systems* (pp. 29-39). UK, USA: Earthscan.
- [16] Florida, I. o. (2007). Types of PV Systems. Retrieved October 2013, from Florida Solar Energy Center: <u>http://www.fsec.ucf.edu/en/consumer/solar\_electricity/basics/types\_of\_pv.htm</u>
- [17] Granderson, A. M. (September 2005). Intelligent Commercial Lighting: Demand-Responsive . UCEI, University of California Energy Institute .
- [18] Joshi, P. M. (December 2007). LOAD SHEDDING ALGORITHM USING VOLTAGE AND FREQUENCY DATA.
- [19] H. Bevrani, A. G. (2010). Power System Load Shedding: Key Issues and New Perspectives. *World Academy of Science, Engineering and Technology 41*.
- [20] J.A. Laghari, H. M. (2012). An Intelligent Under Frequency Load Shedding . IEEE Explore .
- [21] LIMITED, T. N. (2012). Automatic Under-Frequency Load Shedding (AUFLS).

- [22] (UVLSTF)\*, U. L. (JULY 1999). UNDERVOLTAGE LOAD SHEDDING GUIDELINES. Western Systems Coordinating Council.
- [23] Mozina, C. (n.d.). UNDERVOLTAGE LOAD SHEDDING. *Beckwith Electric Co., Inc.*
- [24] Stephan Koch, S. C. (2010). Mitigation of cascading failures by real-time controlled islanding. *IREP Symposium*.
- [25] J. A. Pecas Lopes, Senior Member, IEEE, C. L. Moreira, and A. G. Madureira. (2006). Defining Control Strategies for MicroGrrids Islanded Operation. IEEE.
- [26] M. Kohansal, M. J. Sanjari, G. B. Gharehpetian. (n.d.). A novel approach to frequency control in an islanded microgrid by load shedding scheduling. IEEE.
- [27] Jong-Yul Kim, Member, IEEE, Jin-Hong Jeon, Member, IEEE, Seul-Ki Kim, Member, IEEE, Changhee Cho, Member, IEEE, June Ho Park, Hak-Man Kim, Member, IEEE, and Kee-Young Nam. (2010). Cooperative Control Strategy of Energy Storage System and Microsources for Stabilizing the Microgrid during Islanded Operation. IEEE.

**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

# APPENDIX A

# **Gantt Chart**

Activities of project	Fina	al Year	Projec	t 1 (201	13)	Final Year Project 2			
ALAYSIA							(20	<b>)14</b> )	
Stat Mint	Sept	Oct	Nov	Dec	Jan	Feb	Mar	Apr	Mei
Literature Review									
PV analysis by Matlab				Ь					
Circuit design and simulation									
Analysis and result	Š		2.	ىينى	ۇكرىم	اوي			
Report writing	KNIKA		ALAY	SIA	MEL	AKA			

### **APPENDIX B**

# **Arduino Coding**

const byte is n = 0; const byte vsn = 1; const byte ld1 = 7; const byte ld2 = 8; LAYS const byte ld3 = 9; const byte 1d4 = 10; float current = 0.0; float voltage = 0.0; float power = 0.0;unsigned int current\_d = 0; //digital value for current sensor unsigned int voltage\_d = 0; //digital value for voltage sensor\* **ΔΕ ΜΔΙ** SIA MEL void setup () { pinMode (ld1, OUTPUT); //set output port pinMode (ld2, OUTPUT); pinMode (ld3, OUTPUT); pinMode (ld4, OUTPUT); digitalWrite (ld1,0); digitalWrite (ld2,0); digitalWrite (ld3,0); digitalWrite (ld4,0); pinMode (isn, INPUT);

```
pinMode (vsn, INPUT);
Serial.begin (9600);
delay (100);
}
void loop() {
test_load ( );
if (power <= 3)
{
 digitalWrite (ld1,0);
 digitalWrite (ld2,0);
 digitalWrite (ld3,0);
 digitalWrite (ld4,0);
 Serial.print ("No Load On -- ");
 }
if (power>3 && power<=6)
{
 digitalWrite (ld1,1);
 digitalWrite (ld2,0);
                                   KNIKAL MALAYSIA MEL
 digitalWrite (ld3,0);
 digitalWrite (ld4,0);
 Serial.print ("1 Load On -- ");
 }
else if (power>6 && power<=9)
{
 digitalWrite (ld1,1);
 digitalWrite (ld2,1);
 digitalWrite (ld3,0);
```

```
digitalWrite (ld4,0);
 Serial.print ("2 Load On -- ");
 }
else if (power>9 && power<=12)
 {
 digitalWrite (ld1,1);
 digitalWrite (ld2,1);
 digitalWrite (ld3,1);
 digitalWrite (ld4,0);
 Serial.print ("3 Load On -- ");
                 MALAYS
 }
else if (power>12)
 {
 digitalWrite (ld1,1);
 digitalWrite (ld2,1);
 digitalWrite (ld3,1);
 digitalWrite (ld4,1);
 Serial.print ("4 Load On --
                                    (NIKAL MAL
                            "):
                                                            SIA MFI
}
delay(5000);
}
void sensor_read ( ) {
 int voltage_t=0;
 int current_t=0;
 for (int i=0;i<10;++i) //count total for 10 cycle
 {
  voltage_t = voltage_t + analogRead (vsn);
```

```
current_t = current_t + analogRead (isn);
```

delay (50);

```
}
```

voltage\_d = voltage\_t/10; //count average voltage

```
current_d = current_t/10; //count average current
```

```
voltage = voltage_d * 0.00488; //convert to volt
```

```
voltage = voltage * 4.1914;
```

```
current = (current_d * 0.00488)-2.527; //sensitivity 185mv/A ACS712
```

current = current/0.185;

```
power = voltage * current;
```

Serial.print ("Volt:");

```
Serial.print (voltage);
```



Serial.print (", Power: ");

Serial.print (power);

Serial.println (" ");



```
UNIVERSITI TEKNIKAL MALAYSIA MELAK
```

```
void test_load ( )
```

```
{
```

}

```
Serial.print ("Load All On -- ");
```

```
digitalWrite (ld1, HIGH);
```

digitalWrite (ld2, HIGH); // turn the LED on (HIGH is the voltage level)

```
digitalWrite (ld3, HIGH); // turn the LED on (HIGH is the voltage level)
```

```
digitalWrite (ld4, HIGH); // turn the LED on (HIGH is the voltage level)
```

delay (1000); sensor\_read ( );

# **APPENDIX C**

- 1. Data Sheet of Current Sensor ACS712
- 2. Data Sheet of MOSFET IRF9540
- 3. Data Sheet of Transistor BC548





Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

# **Features and Benefits**

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at  $T_A = 25^{\circ}C$
- Small footprint, low-profile SOIC8 package
- $1.2 \text{ m}\Omega$  internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 66 to 185 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis

Approximate Scale 1:1

Ratiometric output from supply voltage



# Description

The Allegro<sup>™</sup> ACS712 provides economical and precise solutions for AC or DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope ( $\geq V_{IOUT(Q)}$ ) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 m $\Omega$  typical, providing low power loss. The thickness of the copper conductor allows survival of

# **Typical Application**

Continued on the next page...



Application 1. The ACS712 outputs an analog signal, V<sub>OUT</sub>. that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I<sub>P</sub>, within the range specified. C<sub>F</sub> is recommended for noise management, with values that depend on the application.

#### **Description (continued)**

the device at up to  $5 \times$  overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS712 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS712 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

#### **Selection Guide**

Part Number	Packing*	Т <sub>А</sub> (°С)	Optimized Range, I <sub>P</sub> (A)	Sensitivity, Sens (Typ) (mV/A)
ACS712ELCTR-05B-T	Tape and reel, 3000 pieces/reel	-40 to 85	±5	185
ACS712ELCTR-20A-T	Tape and reel, 3000 pieces/reel	-40 to 85	±20	100
ACS712ELCTR-30A-T	Tape and reel, 3000 pieces/reel	-40 to 85	±30	66

\*Contact Allegro for additional packing options.

# Absolute Maximum Ratings

Absolute Maximum Ratings	in.			
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V <sub>CC</sub>		8	V
Reverse Supply Voltage	V <sub>RCC</sub>		-0.1	V
Output Voltage	V <sub>IOUT</sub>		8	V
Reverse Output Voltage	V <sub>RIOUT</sub>		-0.1	V
Output Current Source	I <sub>IOUT(Source)</sub>		- 3	mA
Output Current Sink	I <sub>IOUT(Sink)</sub>		10	mA
Overcurrent Transient Tolerance	l <sub>P</sub>	1 pulse, 100 ms	•100	А
Nominal Operating Ambient Temperature	LINTALO,	Range E	-40 to 85	°C
Maximum Junction Temperature	T <sub>J</sub> (max)		165	°C
Storage Temperature	T <sub>stg</sub>		-65 to 170	°C
UNIVE	RSITTE	KNIKAL MALAYSIA ME	LAKA	

#### **Isolation Characteristics**

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage*	V <sub>ISO</sub>	Agency type-tested for 60 seconds per UL standard 60950-1, 1st Edition	2100	VAC
Working Voltage for Basic Isolation	V <sub>WFSI</sub>	For basic (single) isolation per UL standard 60950-1, 1st Edition	354	VDC or V <sub>pk</sub>
Working Voltage for Reinforced Isolation	V <sub>WFRI</sub>	For reinforced (double) isolation per UL standard 60950-1, 1st Edition	184	VDC or V <sub>pk</sub>

\* Allegro does not conduct 60-second testing. It is done only during the UL certification process.

Parameter	Specification
	CAN/CSA-C22.2 No. 60950-1-03
Fire and Electric Shock	UL 60950-1:2003
	EN 60950-1:2001



Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor





#### **Terminal List Table**

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP-	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal



# ACS712

# Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

#### COMMON OPERATING CHARACTERISTICS<sup>1</sup> over full range of T<sub>A</sub>, C<sub>F</sub> = 1 nF, and V<sub>CC</sub> = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
ELECTRICAL CHARACTERIS	TICS					
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, output open	_	10	13	mA
Output Capacitance Load	CLOAD	VIOUT to GND	-	-	10	nF
Output Resistive Load	R <sub>LOAD</sub>	VIOUT to GND	4.7	-	-	kΩ
Primary Conductor Resistance	R <sub>PRIMARY</sub>	T <sub>A</sub> = 25°C	-	1.2	-	mΩ
Rise Time	t <sub>r</sub>	$I_P = I_P(max), T_A = 25^{\circ}C, C_{OUT} = open$	-	3.5	-	μs
Frequency Bandwidth	f	$-3 \text{ dB}, \text{T}_{\text{A}} = 25^{\circ}\text{C}; \text{I}_{\text{P}} \text{ is 10 A peak-to-peak}$	_	80	-	kHz
Nonlinearity	E <sub>LIN</sub>	Over full range of I <sub>P</sub>	_	1.5	-	%
Symmetry	E <sub>SYM</sub>	Over full range of I <sub>P</sub>	98	100	102	%
Zero Current Output Voltage	V <sub>IOUT(Q)</sub>	Bidirectional; I <sub>P</sub> = 0 A, T <sub>A</sub> = 25°C	_	V <sub>CC</sub> × 0.5	_	V
Power-On Time	P tPO	Output reaches 90% of steady-state level, $T_J$ =25°C, 20 A present on leadframe	_	35	-	μs
Magnetic Coupling <sup>2</sup>		AX	-	12	-	G/A
Internal Filter Resistance <sup>3</sup>	R <sub>F(INT)</sub>	×		1.7		kΩ

<sup>1</sup>Device may be operated at higher primary current levels,  $I_P$ , and ambient,  $T_A$ , and internal leadframe temperatures,  $T_A$ , provided that the Maximum Junction Temperature,  $T_J(max)$ , is not exceeded.

<sup>2</sup>1G = 0.1 mT.

<sup>3</sup>R<sub>F(INT)</sub> forms an RC circuit via the FILTER pin.

# COMMON THERMAL CHARACTERISTICS<sup>1</sup> EKNIKAL MALAYSIA MELAKA

			Min.	Тур.	Max.	Units
Operating Internal Leadframe Temperature	T <sub>A</sub>	E range	-40	_	85	°C
					Value	Units
Junction-to-Lead Thermal Resistance <sup>2</sup> R <sub>0JL</sub> Mounted on the Allegro ASEK 712 evaluation board					5	°C/W
Junction-to-Ambient Thermal Resistance R <sub>0JA</sub> Mounted on the Allegro 85-0322 evaluation board, includes the power con- sumed by the board						°C/W

<sup>1</sup>Additional thermal information is available on the Allegro website.

<sup>2</sup>The Allegro evaluation board has 1500 mm<sup>2</sup> of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.



#### **x05B PERFORMANCE CHARACTERISTICS1** $T_A = -40^{\circ}C$ to 85°C, $C_F = 1 \text{ nF}$ , and $V_{CC} = 5 \text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Optimized Accuracy Range	l <sub>P</sub>		-5	-	5	A
Sensitivity	Sens	Over full range of I <sub>P,</sub> T <sub>A</sub> = 25°C	180	185	190	mV/A
Noise	V <sub>NOISE(PP)</sub>	Peak-to-peak, $T_A = 25^{\circ}$ C, 185 mV/A programmed Sensitivity, C <sub>F</sub> = 47 nF, C <sub>OUT</sub> = open, 2 kHz bandwidth	_	21	_	mV
Zero Current Output Slope	$\Delta V_{OUT(Q)}$	$T_A = -40^{\circ}C$ to $25^{\circ}C$	—	-0.26	_	mV/°C
		T <sub>A</sub> = 25°C to 150°C	-	-0.08	-	mV/°C
Sensitivity Slope	ASons	$T_A = -40^{\circ}C$ to 25°C	-	0.054	-	mV/A/°C
		T <sub>A</sub> = 25°C to 150°C	-	-0.008	-	mV/A/°C
Total Output Error <sup>2</sup>	E <sub>TOT</sub>	$I_P = \pm 5 \text{ A}, T_A = 25^{\circ}\text{C}$	-	±1.5	-	%

<sup>1</sup>Device may be operated at higher primary current levels, I<sub>P</sub>, and ambient temperatures, T<sub>A</sub>, provided that the Maximum Junction Temperature, T<sub>J(max)</sub>, is not exceeded.

<sup>2</sup>Percentage of  $I_{P}$ , with  $I_{P} = 5 A$ . Output filtered.

#### x20A PERFORMANCE CHARACTERISTICS<sup>1</sup> T<sub>A</sub> = -40°C to 85°C, C<sub>F</sub> = 1 nF, and V<sub>CC</sub> = 5 V, unless otherwise specified

Characteristic	X	Symbol	S Test Conditions	Min.	Тур.	Max.	Units
Optimized Accuracy Range	-	I <sub>P</sub>		-20	-	20	A
Sensitivity	_	Sens	Over full range of I <sub>P</sub> , T <sub>A</sub> = 25°C	96	100	104	mV/A
Noise	1.	V <sub>NOISE(PP)</sub>	Peak-to-peak, $T_A = 25^{\circ}$ C, 100 mV/A programmed Sensitivity, C <sub>F</sub> = 47 nF, C <sub>OUT</sub> = open, 2 kHz bandwidth	-	11	_	mV
Zero Current Output Slope		ΔV <sub>OUT(Q</sub> )	$T_A = -40^{\circ}C$ to 25°C	-	-0.34	-	mV/°C
			T <sub>A</sub> = 25°C to 150°C	_	-0.07	-	mV/°C
Sensitivity Slope	6	ASens	$T_A = -40^{\circ}C$ to 25°C	_	0.017	-	mV/A/°C
		Adens	$T_A = 25^{\circ}C$ to $150^{\circ}C$	4	-0.004	-	mV/A/°C
Total Output Error <sup>2</sup>		E <sub>TOT</sub> •	$I_{P} = \pm 20 \text{ A}, T_{A} = 25^{\circ}\text{C}$		±1.5	-	%

<sup>1</sup>Device may be operated at higher primary current levels, I<sub>P</sub>, and ambient temperatures, T<sub>A</sub>, provided that the Maximum Junction Temperature,

 $T_{J}$ (max), is not exceeded. <sup>2</sup>Percentage of  $I_{P}$ , with  $I_{P}$  = 20 A. Output filtered.

#### **x30A PERFORMANCE CHARACTERISTICS**<sup>1</sup> $T_A = -40^{\circ}$ C to 85°C, $C_F = 1$ nF, and $V_{CC} = 5$ V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Optimized Accuracy Range	l <sub>P</sub>		-30	-	30	A
Sensitivity	Sens	Over full range of I <sub>P</sub> , T <sub>A</sub> = 25°C	63	66	69	mV/A
Noise	V <sub>NOISE(PP)</sub>	Peak-to-peak, $T_A = 25^{\circ}$ C, 66 mV/A programmed Sensitivity, C <sub>F</sub> = 47 nF, C <sub>OUT</sub> = open, 2 kHz bandwidth	_	7	_	mV
Zero Current Output Slope	$\Delta V_{OUT(Q)}$	$T_A = -40^{\circ}C$ to 25°C	-	-0.35	-	mV/°C
		T <sub>A</sub> = 25°C to 150°C	_	-0.08	-	mV/°C
Sensitivity Slope	ASons	$T_A = -40^{\circ}C$ to 25°C	-	0.007	-	mV/A/°C
		T <sub>A</sub> = 25°C to 150°C	-	-0.002	-	mV/A/°C
Total Output Error <sup>2</sup>	E <sub>TOT</sub>	$I_{P} = \pm 30 \text{ A}, T_{A} = 25^{\circ}\text{C}$	-	±1.5	-	%

<sup>1</sup>Device may be operated at higher primary current levels,  $I_{p}$ , and ambient temperatures,  $T_{A}$ , provided that the Maximum Junction Temperature,  $T_{I}(max)$ , is not exceeded.

<sup>2</sup>Percentage of  $I_{P}$ , with  $I_{P}$  = 30 A. Output filtered.



# **ACS712**

# Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor



Characteristic Performance



# ACS712

# Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

Characteristic Performance  $I_P = 20 \text{ A}$ , unless otherwise specified





Allegro MicroSystems, LLC 115 Northeast Cutoff Worcester, Massachusetts 01615-0036 U.S.A. 1.508.853.5000; www.allegromicro.com
# Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor



Characteristic Performance I<sub>P</sub> = 30 A, unless otherwise specified



#### **Definitions of Accuracy Characteristics**

**Sensitivity (Sens).** The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

**Noise (V<sub>NOISE</sub>).** The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC ( $\approx 1$  G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

**Linearity** ( $\mathbf{E}_{LIN}$ ). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100 \left\{ 1 - \left[ \frac{\Delta \operatorname{gain} \times \% \operatorname{sat} \left( V_{\operatorname{IOUT\_full-scale}} \operatorname{amperes} - V_{\operatorname{IOUT}(Q)} \right)}{2 \left( V_{\operatorname{IOUT\_half-scale}} \operatorname{amperes} - V_{\operatorname{IOUT}(Q)} \right)} \right] \right\}$$

where  $V_{\text{IOUT}_{full-scale amperes}} =$  the output voltage (V) when the sampled current approximates full-scale  $\pm I_P$ .

**Symmetry (E**<sub>SYM</sub>). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

 $100 \left( \frac{V_{\text{IOUT}} + \text{full-scale amperes} - V_{\text{IOUT}(Q)}}{V_{\text{IOUT}(Q)} - V_{\text{IOUT}} - \text{full-scale amperes}} \right) = KNIKAL MALAY$ 

**Quiescent output voltage (V**<sub>IOUT(Q)</sub>). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at V<sub>CC</sub>/2. Thus, V<sub>CC</sub> = 5 V translates into V<sub>IOUT(Q)</sub> = 2.5 V. Variation in V<sub>IOUT(Q)</sub> can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

**Electrical offset voltage (V**<sub>OE</sub>). The deviation of the device output from its ideal quiescent value of V<sub>CC</sub>/2 due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy ( $E_{TOT}$ ). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0** A over  $\Delta$  temperature. Accuracy at the zero current flow including temperature effects.
- Full-scale current at 25°C. Accuracy at the full-scale current at 25°C, without the effects of temperature.
- Full-scale current over ∆ temperature. Accuracy at the fullscale current flow including temperature effects.

**Ratiometry**. The ratiometric feature means that its 0 A output,  $V_{IOUT(Q)}$ , (nominally equal to  $V_{CC}/2$ ) and sensitivity, Sens, are proportional to its supply voltage,  $V_{CC}$ . The following formula is used to derive the ratiometric change in 0 A output voltage,

 $\Delta V_{\text{IOUT}(Q)\text{RAT}}$  (%).

 $100 \left( \frac{V_{\text{IOUT}(Q)\text{VCC}} / V_{\text{IOUT}(Q)5\text{V}}}{V_{\text{CC}} / 5 \text{ V}} \right)$ 

The ratiometric change in sensitivity,  $\Delta \text{Sens}_{RAT}$  (%), is defined as:

 $100 \left( \frac{Sens_{\rm VCC} / Sens_{\rm 5V}}{V_{\rm CC} / 5 \rm V} \right)$ 

```
Output Voltage versus Sampled Current
Accuracy at 0 A and at Full-Scale Current
```





Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

I (%)

90

V<sub>CC</sub>(typ

#### **Definitions of Dynamic Response Characteristics**

Power-On Time (t<sub>PO</sub>). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, tPO, is defined as the time it takes for the output voltage to settle within  $\pm 10\%$  of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V<sub>CC</sub>(min), as shown in the chart at right.

V<sub>OUT</sub> 90% V<sub>OUT</sub> V<sub>CC</sub>(min.) t1= time at which power supply reaches minimum specified operating voltage t<sub>2</sub>= time at which output voltage settles within ±10% of its steady state value under an applied magnetic field

Primary Current

sducer Output

+t

ť

Rise time  $(t_r)$ . The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which  $f(-3 \text{ dB}) = 0.35/t_r$ . Both tr and tRESPONSE are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

200

10000

1000

10

Voise<sub>(p-p)</sub> (mA) 100 MALAYSIA



t<sub>r</sub> (µs)

3.5 5.8

17.5

73.5

88.2

291.3

623

1120







4.7

47

Allegro MicroSystems, LLC 115 Northeast Cutoff Worcester, Massachusetts 01615-0036 U.S.A. 1.508.853.5000; www.allegromicro.com

Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

#### **Chopper Stabilization Technique**

Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.



Concept of Chopper Stabilization Technique



### **Typical Applications**



Application 4. Rectified Output. 3.3 V scaling and rectification application for A-to-D converters. Replaces current transformer solutions with simpler ACS circuit. C1 is a function of the load resistance and filtering desired. R1 can be omitted if the full range is desired.

Application 5. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.



#### Improving Sensing System Accuracy Using the FILTER Pin

In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation,  $\Delta V_{ATT}$ , is a result of the resistive divider effect between the resistance of the external filter,  $R_F$  (see Application 6), and the input impedance and resistance of the customer interface circuit,  $R_{INTFC}$ . The transfer function of this resistive divider is given by:

$$\Delta V_{\rm ATT} = V_{\rm IOUT} \left( \frac{R_{\rm INTFCAY}}{R_{\rm F} + R_{\rm INTFC}} \right) / \cdot$$

Even if  $R_F$  and  $R_{INTFC}$  are designed to match, the two individual resistance values will most likely drift by different amounts over

temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance,  $R_{INTFC}$ , of a typical analog-to-digital converter (ADC) can be as low as 10 k $\Omega$ .

The ACS712 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor,  $C_F$  (see Application 7) from the FILTER pin to ground. The buffer amplifier inside of the ACS712 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for  $\Delta V_{ATT}$ . Therefore, the ACS712 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.





13

#### Package LC, 8-pin SOIC





# Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

#### **Revision History**

Revision	Revision Date	Description of Revision
Rev. 15	November 16, 2012	Update rise time and isolation, I <sub>OUT</sub> reference data, patents



Copyright ©2006-2013, Allegro MicroSystems, LLC

The products described herein are protected by U.S. patents: 5,621,319; 7,598,601; and 7,709,754.

Allegro MicroSystems, LLC reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

<u>Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.</u>

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

www.allegromicro.com



**Vishay Siliconix** 

RoHS

COMPLIANT



### **Power MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	- 1	00		
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = - 10 V	0.20		
Q <sub>g</sub> (Max.) (nC)	6	1		
Q <sub>gs</sub> (nC)	14			
Q <sub>gd</sub> (nC)	2	9		
Configuration	Sin	gle		



#### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

#### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING IN	FORMATION	
Package		TO-220AB
Lead (Ph)-free	NO.	IRF9540PbF
		SiHF9540-E3
SnDb	6 4 4	IRF9540
SHED	المعصل ملتسبيا مالاك	SiHF9540

ABSOLUTE MAXIMUM RATINGS ( $T_C$	= 25 °C, unle	ess otherwis	se noted)			
PARAMETER UNIVERSITI TE	KNIKA		SYMBOL		UNIT	
Drain-Source Voltage			V <sub>DS</sub>	- 100	V	
Gate-Source Voltage			V <sub>GS</sub>	± 20	v	
Continuous Drain Current	Vec at = 10 V	T <sub>C</sub> = 25 °C	I_	- 19		
Continuous Drain Current	VGS at - TO V	T <sub>C</sub> = 100 °C	U	- 13	А	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	- 72		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	640	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	- 19	А	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	15	mJ	
Maximum Power Dissipation	$T_{\rm C} = 2$	25 °C	PD	150	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	- 5.5	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for 1	0 s		300 <sup>d</sup>	U	
Mounting Torque	6 00 or M	0.00		10	lbf ∙ in	
	0-32 Or IV	IS SCIEW		1.1	N · m	

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b.  $V_{DD}$  = - 25 V, starting T<sub>J</sub> = 25 °C, L = 2.7 mH, R<sub>g</sub> = 25  $\Omega$ , I<sub>AS</sub> = - 19 A (see fig. 12).

c.  $I_{SD} \leq$  - 19 A, dI/dt  $\leq$  200 A/µs,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.

d. 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

Document Number: 91078 S11-0512-Rev. B, 21-Mar-11 www.vishay.com

Vishay Siliconix



PARAMETER	SYMBOL	TYP. MAX.			UNIT			
Maximum Junction-to-Ambient	R <sub>th.IA</sub>	- 62						
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.50	-					
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0					
		-1						
SPECIFICATIONS (T <sub>J</sub> = 25 °C, u	unless otherwi	ise noted)						
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							1	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V	/, I <sub>D</sub> = - 250 μA	- 100	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to	25 °C, I <sub>D</sub> = - 1 mA	-	- 0.087	-	V/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{G}$	<sub>S</sub> , I <sub>D</sub> = - 250 μΑ	- 2.0	-	- 4.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub>	<sub>s</sub> = ± 20 V	-	-	± 100	nA	
		V <sub>DS</sub> = - 1	00 V, V <sub>GS</sub> = 0 V	-	-	- 100		
Zero Gate voltage Drain Current	SIA	V <sub>DS</sub> = - 80 V, V	<sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C	-	-	- 500	μΑ	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 11 A <sup>b</sup>	-	-	0.20	Ω	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = - 5	0 V, I <sub>D</sub> = - 11 A <sup>b</sup>	6.2	-	-	S	
Dynamic 🖉	KA							
Input Capacitance	C <sub>iss</sub>	V	re = 0 V	-	1400	-		
Output Capacitance	C <sub>oss</sub>	VDS	s = - 25 V,	-	590	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	T = 1.0 F	VIHZ, see tig. 5	-	140	-		
Total Gate Charge	Qg			-	-	61		
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 19 A, V <sub>DS</sub> = - 80 V, see fig. 6 and 13 <sup>b</sup>	-	-	14	nC	
Gate-Drain Charge	Q <sub>gd</sub>	/	** **	- *	1-	29		
Turn-On Delay Time	t <sub>d(on)</sub>	- un	سىي بە	ىبوم	9 16	-		
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = - 5	0 V, I <sub>D</sub> = - 19 A,	-	73	-	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 9.1 \Omega$ , $R_D = 2.4 \Omega$ , see fig. $10^{b}$			34	-	113	
Fall Time	t <sub>f</sub>				57	-		
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from	n Li	-	4.5	-	۶IJ	
Internal Source Inductance	L <sub>S</sub>	die contact		-	7.5	-		
Drain-Source Body Diode Characteristi	cs	•						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the		-	-	- 19	^	
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	p - n junction diode		-	-	- 72	A	
Body Diode Voltage	V <sub>SD</sub>	$T_{\rm J}$ = 25 °C, I <sub>S</sub>	= - 19 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	- 5.0	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T = 25 °C	10 A dl/dt . 100 A /	-	130	260	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	ι <sub>J</sub> = 25 °C, I <sub>F</sub> = - 19 A, dl/dt = 100 A/μs <sup>p</sup>		-	0.35	0.70	μC	
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-	n-on is dor	ninated b	y L <sub>S</sub> and	L <sub>D</sub> )		

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.

www.vishay.com 2

Document Number: 91078 S11-0512-Rev. B, 21-Mar-11



**Vishay Siliconix** 





**Vishay Siliconix** 





Fig. 8 - Maximum Safe Operating Area

Document Number: 91078 S11-0512-Rev. B, 21-Mar-11



 $\mathsf{R}_\mathsf{D}$ 

V<sub>DS</sub>

**Vishay Siliconix** 



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

## Vishay Siliconix





Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms







www.vishay.com 6 Document Number: 91078 S11-0512-Rev. B, 21-Mar-11



#### **Vishay Siliconix**



#### Peak Diode Recovery dV/dt Test Circuit



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91078.

Document Number: 91078 S11-0512-Rev. B, 21-Mar-11 www.vishay.com



**Vishay Siliconix** 

### **TO-220AB**



**UNIVERSITI TEKNIKAL MALAYSIA MELAKA** 

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000



Vishay

## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

	RCHILD ONDUCTOR 11	Discrete POWI Techno	ER & Sign logies
	BC548 BC548A BC548B BC548C		
	E B C TO-92		
NPN This device and switch Process 1 Absolu	<b>General Purpose Amplifier</b> re is designed for use as general purpose amplifiers es requiring collector currents to 300 mA. Sourced from 0. See PN100A for characteristics. <b>Ute Maximum Ratings*</b> TA = 25°C unless otherwise no		
NPN This devic and switch Process 1 Absol	General Purpose Amplifier es is designed for use as general purpose amplifiers es requiring collector currents to 300 mA. Sourced from 0. See PN100A for characteristics. ute Maximum Ratings* TA = 25°C unless otherwise no Parameter	del value	9 Units
NPN This device and switch Process 1 Absolu	General Purpose Amplifier re is designed for use as general purpose amplifiers es requiring collector currents to 300 mA. Sourced from 0. See PN100A for characteristics. ute Maximum Ratings* TA = 25°C unless otherwise no Parameter Collector-Emitter Voltage	sted 30	Units V
NPN This devic and switch Process 1 Absolu	General Purpose Amplifier         re is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise not         Parameter         Collector-Emitter Voltage         Collector-Base Voltage	oted	Units V V
NPN This devic and switch Process 1 Absolu ymbol SEO SES BO	General Purpose Amplifier         e is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise not         Parameter         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage	ated Value 30 30 5.0	Units V V V
NPN This device and switch Process 1 Absolu ymbol EEO EES BO	General Purpose Amplifier         re is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise no         Parameter         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous	Value           30           30           5.0           500	V V V mA
NPN This device Process 1 Absolu Symbol SEO SES BO	General Purpose Amplifier         re is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise no         Parameter         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range	Value           30           30           5.0           500           -55 to +150	V V V MA °C
NPN This devic and switch Process 1 Absolu Symbol SED 20 255 300 * These rating NOTES: 1) These rating NOTES: 2) These are Therm	General Purpose Amplifier         the is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         the Maximum Ratings*         TA = 25°C unless otherwise nor         Collector-Emitter Voltage         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range         rs are limiting values above which the serviceability of any semiconductor device may         rs are based on a maximum junction temperature of 150 degrees C.         stady state limits. The factory should be consulted on applications involving pulsed of	bied Value 30 30 5.0 500 -55 to +150 be impaired.	V V V MA °C
NPN This devic and switch Process 1 Absolu ymbol CES EBO * These ration NOTES: 1) These ration 2) These ration Therm ymbol	General Purpose Amplifier         the is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics         the Maximum Ratings*         The 25°C unless otherwise note         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range         rate are based on a maximum junction temperature of 150 degrees C.         stady state limits. The factory should be consulted on applications involving pulsed on         al Characteristics         The 25°C unless otherwise noted         Characteristic	ted Value 30 30 5.0 500 -55 to +150 be impaired. or low duty cycle operations.	Units V V MA °C
NPN This devic and switch Process 1 Absolut SED CED CES SED * These ration NOTES: 1) These ration 2) These are Therm ymbol	General Purpose Amplifier         the is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         the Maximum Ratings*         The 25°C unless otherwise not         Parameter         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range         rs are based on a maximum junction temperature of 150 degrees C.         stady state limits. The factory should be consulted on applications involving pulsed of         at Characteristics         The 25°C unless otherwise noted	bied Value 30 30 5.0 500 -55 to +150 be impaired. or low duty cycle operations. Max BC548 / A / B / C 625	Units V V V MA °C
NPN This devic and switch Process 1 Absolu SEO EES These rating NOTES: 1) These rating 1) These rating	General Purpose Amplifier         e is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise no         Collector-Emitter Voltage         Collector-Emitter Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range         rgs are limiting values above which the serviceability of any semiconductor device may         ngs are based on a maximum junction temperature of 150 degrees C.         stady state limits. The factory should be consulted on applications involving pulsed of         al Characteristics         TA = 25°C unless otherwise noted         Characteristic         Total Device Dissipation Derate above 25°C	Value         30         30         5.0         500         -55 to +150         be impaired.         or low duty cycle operations.         Max         BC548 / A / B / C         625         5.0	Units V V V MA °C
NPN This devic and switch Process 1 Absolu SEO SES BO * These rating NOTES: 1) These rating NOTES: 2) These rating MOTES: 1) These rating 1) The	General Purpose Amplifier         er is designed for use as general purpose amplifiers         es requiring collector currents to 300 mA. Sourced from         0. See PN100A for characteristics.         ute Maximum Ratings*         TA = 25°C unless otherwise not         Collector-Emitter Voltage         Collector-Emitter Voltage         Collector-Base Voltage         Emitter-Base Voltage         Collector Current - Continuous         Operating and Storage Junction Temperature Range         rs are limiting values above which the serviceability of any semiconductor device may         ngs are based on a maximum junction temperature of 150 degrees C.         steady state limits. The factory should be consulted on applications involving pulsed of         Marcheristics         TA = 25°C unless otherwise noted         Characteristic         Image: Total Device Dissipation         Derate above 25°C         Thermal Resistance, Junction to Case	Value         30           30         30           5.0         500           -55 to +150         500           be impaired.         500           or low duty cycle operations.         500           BC548 / A / B / C         625           5.0         83.3	Units V V W MA °C Units MW mW/°C °C/W

BC548 / BC548A / BC548B / BC548C

DEF CHARACTERISTICS           (ancode)         Collector-Base Breakdown Voltage         1/c = 10 µA, 1/c = 0         30         V           (ancode)         Collector-Base Breakdown Voltage         1/c = 10 µA, 1/c = 0         30         V           (ancode)         Collector-Base Breakdown Voltage         1/c = 10 µA, 1/c = 0         30         V           (ancede)         Emitter-Base Breakdown Voltage         1/c = 10 µA, 1/c = 0         5.0         V           (ancede)         Collector Cutoff Current         Vca = 30 V, 1/c = 0, TA = +150 °C         5.0         µA           ON CHARACTERISTICS         The         DC Current Gain         Vcc = 5.0 V, 1/c = 2.0 mA         548A         110         820           Vectaan         Collector-Emitter Saturation Voltage         1/c = 10 mA, 1/a = 0.5 mA         0.658         0.70         V           Vactaan         Collector-Emitter Saturation Voltage         Vca = 5.0 V, 1/c = 2.0 mA         0.68         0.77         V           SMALL <signal characteristics<="" td="">         State         Vca = 5.0 V, 1/c = 2.0 mA         0.68         0.77         V           SMALL<signal characteristics<="" td="">         Vca = 5.0 V, 1/c = 2.0 mA         0.68         0.77         V           SMALL         Signal Current Gain         1/c = 2.0 mA / 0.28         0.77</signal></signal>	Def CHARACTERISTICS         (arccio)       Collector-Ease Breakdown Voltage       (c = 10 µA, lg = 0       30       V         (arccio)       Collector-Base Breakdown Voltage       (c = 10 µA, lg = 0       30       V         (arccio)       Collector-Base Breakdown Voltage       (c = 10 µA, lg = 0       30       V         (arccio)       Collector-Base Breakdown Voltage       (c = 10 µA, lg = 0       5.0       V         (arccio)       Collector-Cutoff Current       Vcs = 30 V, lg = 0, T_A = +150 °C       5.0       N         (b = 10 mA, lg = 0       To vs = 30 V, lg = 0, T_A = +150 °C       5.0       N       A         (b = 10 mA, lg = 0, T_A = +150 °C       S.0       N       A       A       A         (b = 10 mA, lg = 0, T_A = +150 °C       S.0       N       A	Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS           Vigences         Collector-Emitter Breakdown Voltage         lc = 10 µA, le = 0         30         V           Vigences         Collector-Base Breakdown Voltage         lc = 10 µA, le = 0         30         V           Vigences         Collector-Base Breakdown Voltage         lc = 10 µA, le = 0         30         V           Vigences         Collector-Base Breakdown Voltage         lc = 10 µA, le = 0         5.0         V           Collector-Clutof Current         Vice = 30 V, le = 0         5.0         V         V           Collector-Clutof Current         Vice = 5.0 V, le = 0, T_A = +150 °C         1.6         nA           DNCHARACTERISTICS         N         Vice = 5.0 V, le = 0.0 mA         548         110         200           Vicesati         Collector-Emitter Saturation Voltage         lic = 10 mA, le = 0.5 mA         0.265         V           Vicesati         Collector-Emitter Saturation Voltage         Vice = 5.0 V, le = 2.0 mA         0.58         0.70         V           Vicesati         Collector-Emitter Saturation Voltage         Vice = 5.0 V, le = 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         Vice = 5.0 V, le = 2.0 mA         0.58         0.77         V           NF	OFF CHARACTERISTICS           Vigueza         Collector-Base Breakdown Voltage         Lc = 10 µA, lg = 0         30         V           Vigueza         Collector-Base Breakdown Voltage         Lc = 10 µA, lg = 0         30         V           Vigueza         Collector-Base Breakdown Voltage         Lc = 10 µA, lg = 0         30         V           Vigueza         Collector-Base Breakdown Voltage         Lg = 10 µA, lg = 0         5.0         V           Collector Cutoff Current         Vog = 30 V, lg = 0         T, a = +150 °C         5.0         V           Collector Existence         Vog = 30 V, lg = 0, T_a = +150 °C         5.0         V         V           Collector Cutoff Current Gain         Vog = 5.0 V, lg = 2.0 mA         548         110         800         548           Vog = 0         Collector Emitter Saturation Voltage         Lg = 10 mA, lg = 5.0 mA         0.660         V           Vog = 0         Wog = 5.0 V, lg = 2.0 mA         0.58         0.70         V         V           Vacion         Bese-Emitter On Voltage         Vog = 5.0 V, lg = 2.0 mA         0.58         0.70         V           Vacion         Bese-Emitter On Voltage         Vog = 5.0 V, lg = 2.0 mA         0.58         0.70         V           NF         Nois						
Varagesol         Collector-Emitter Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{g} = 0$ 30         V           Varagesol         Collector-Base Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{e} = 0$ 30         V           Varagesol         Collector-Base Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{e} = 0$ 30         V           Varagesol         Collector-Base Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{c} = 0$ 30         V           Varagesol         Collector-Case Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{c} = 0$ 50         V           Varagesol         Collector-Case Breakdown Voltage $l_{c} = 10 \ \mu$ A, $l_{c} = 0$ 50         V           Varagesol         Collector-Catrof Cutoff Current $V_{cp} = 30 \ V$ , $l_{c} = 0, \ T_{A} = +150 \ ^{\circ}{\rm C}$ 110         800           ONCHARACTERISTICS         DC Current Gain $V_{Cg} = 5.0 \ V$ , $l_{c} = 2.0 \ m$ A         548         110         220           Vection         Collector-Emitter Saturation Voltage $l_{c} = 10 \ m$ A, $l_{B} = 0.5 \ m$ A         0.058         V           Vection         Collector-Emitter Saturation Voltage $V_{cg} = 5.0 \ V$ , $l_{c} = 2.0 \ m$ A         0.58         0.70         V           Value(on)         Base-Emitter On Voltage $V_{cg} = 5.0 \ V$ , $l$	Version         Collector-Emitter Breakdown Voltage         L <sub>c</sub> = 10 µA, I <sub>k</sub> = 0         30         V           Viencea         Collector-Base Breakdown Voltage         L <sub>c</sub> = 10 µA, I <sub>k</sub> = 0         30         V           Viencea         Collector-Base Breakdown Voltage         L <sub>c</sub> = 10 µA, I <sub>k</sub> = 0         30         V           Viencea         Emitter-Base Breakdown Voltage         L <sub>k</sub> = 10 µA, I <sub>k</sub> = 0         30         V           Viencea         Collector-Base Breakdown Voltage         L <sub>k</sub> = 10 µA, I <sub>k</sub> = 0         50         V           Collector-Cutoff Current         Vois = 30 V, I <sub>k</sub> = 0, T <sub>A</sub> = +150 °C         15         nA           ONCHARACTERISTICS         Nr         Stabs         110         800           Vacination         Collector-Emitter Saturation Voltage         L <sub>c</sub> = 10 mA, I <sub>b</sub> = 0.5 mA         20.25         V           V <sub>CE</sub> (ren)         DC Current Gain         Vois = 5.0 V, I <sub>c</sub> = 2.0 mA         20.80         800         V           V <sub>GE</sub> (ren)         Base-Emitter On Voltage         Vois = 5.0 V, I <sub>b</sub> = 2.0 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         Nr         Nise Figure         Vois = 5.0 V, I <sub>b</sub> = 2.0 mA         0.58         0.77         V           NF         Noise Figure         Vois = 2.0 V, I <sub>b</sub>	OFF CHA	RACTERISTICS				
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V <sub>(BR)CEO</sub>	Collector-Emitter Breakdown Voltage	$I_{\rm C} = 10 \text{ mA}, I_{\rm B} = 0$	30		V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Vances         Collector-Base Breakdown Voltage $l_c = 10 \mu A, l_c = 0$ 30         V           Vanspano         Emitter-Base Breakdown Voltage $l_c = 10 \mu A, l_c = 0$ 5.0         V           Collector Cutoff Current         Vor         30 V, l_c = 0         5.0         V           ONCHARACTERISTICS         Inter-Base Breakdown Voltage         Inter-Base Breakdown Voltage         Vor         5.0 $\mu A$ ONCHARACTERISTICS         Inter-Base Breakdown Voltage         Vor         5.0 $V_c = 5.0 V, l_c = 2.0 \text{ mA}$ 5488         110         800         5488           Vor         Stable 200         450         5488         200         450         5488         420         800         V         V         V         Vor         5480         420         800         V	V <sub>(BR)CBO</sub>	Collector-Base Breakdown Voltage	$I_{\rm C} = 10 \ \mu {\rm A}, \ I_{\rm E} = 0$	30		V
Vigneteo         Emitter-Base Breakdown Voltage         I = 10 $\mu$ A, $I_{c} = 0$ 5.0         V           Uceo         Collector Cutoff Current         V <sub>CB</sub> = 30 V, $I_{E} = 0$ T <sub>A</sub> = +150 °C         5.0 $\mu$ A           ON CHARACTERISTICS         hre         DC Current Gain         V <sub>CE</sub> = 5.0 V, $I_{c} = 2.0 \text{ mA}$ 548 ± 110 ± 220 ± 548 ± 420         800 ± 420 ± 800 ± 420         800 ± 420 ± 800 ± 420         800 ± 420 ± 800 ±	Vigsgebo         Emitter-Base Breakdown Voltage         IE         10 JA, IE         5.0         V           Useo         Collector Cutoff Current         Vois = 30 V, IE = 0, TA = +150 °C         15         nA           ON CHARACTERISTICS         hpe         DC Current Gain         Vois = 5.0 V, Ic = 2.0 mA         548         110         800           Vestion         Collector-Emitter Saturation Voltage         Ic = 10 mA, Is = 0.5 mA         0.25         V           Vestion         Base-Emitter On Voltage         Vois = 5.0 V, Ic = 2.0 mA         548         110         800           Vestion         Collector-Emitter Saturation Voltage         Ic = 10 mA, Is = 0.5 mA         0.25         V           Vestion         Base-Emitter On Voltage         Vois = 5.0 V, Ic = 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         Nre         Small-Signal Current Gain         Ic = 2.0 mA, Vois = 5.0 V, Ic = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         Nre         Noise Figure         Re = 2.0 KO, Ic = 10 mA, Vois = 5.0 V, Ic = 200 IA, Be = 2.0 KO, Ic = 10 mA, Be = 2.0 KO, Ic = 10 mA, Be = 2.0 KO, Ic = 10 mA, Be = 2.0 KO, Ic = 2.0 MA, Be = 2.0 KO, Ic = 1.0 MHz, Be = 2.0 KO, Ic = 1.0 MHz, Be = 2.0 KO, Ic = 2.0 MA, Be = 2.0 KO, Ic = 2.0 MA, Be = 2.0 KO, Ic = 2.0 MA, Be =	V <sub>(BR)CES</sub>	Collector-Base Breakdown Voltage	$I_{\rm C} = 10 \ \mu {\rm A}, \ I_{\rm E} = 0$	30		V
Collector Cutoff Current         V <sub>CB</sub> = 30 V, I <sub>E</sub> = 0, T <sub>A</sub> = +150 °C         15         nA           ONCHARACTERISTICS         here         DC Current Gain         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA         548         110         800           V <sub>CE</sub> = 30 V, I <sub>E</sub> = 0, T <sub>A</sub> = +150 °C         548.0         110         800         548.0         110         800         548.0         110         800         548.0         110         800         548.0         110         800         548.0         120         800         548.0         120         800         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA         0.05.0         V         V <sub>CE</sub> = 10 mA, I <sub>B</sub> = 0.5 mA         0.25.0         V         V         900         1         10         0.60         V         V         V         900         1         10         0.60         V         V         V         0.61         V         V         0.62         V         V         0.61         V         V         0.62         V         0.63         0.77         V         V         Small-Signal Current Gain         I <sub>L</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V, I <sub>L</sub> = 10 mA         0.68         0.77         V         Small-Signal Current Gain         I <sub>L</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V, I <sub>L</sub> = 10 mA         0.60         V         Small-Signal Current Gain         I <sub>L</sub> =	Collector Cutoff Current         Vois = 30 V, Is = 0         15         nA           Vois = 30 V, Is = 0, TA = +150 °C         5.0         µA           ONCHARACTERISTICS         Ne         DC Current Gain         Vois = 5.0 V, Ic = 2.0 mA         548         110         820         450           Vois = 30 V, Is = 0, TA = +150 °C         548A         110         800         548A         110         800         9	V <sub>(BR)EBO</sub>	Emitter-Base Breakdown Voltage	$I_{\rm E} = 10 \mu \text{A}, I_{\rm C} = 0$	5.0		V
ON CHARACTERISTICS           Impre         DC Current Gain         Vcc = 5.0 V, lc = 2.0 mA         548         110         800           Vcc(sa0)         Collector-Emitter Saturation Voltage         Ic = 10 mA, la = 0.5 mA         0.60         V           Vcc(sa0)         Collector-Emitter Saturation Voltage         Ic = 10 mA, la = 0.5 mA         0.68         0.77         V           SMALL SIGNAL CHARACTERISTICS         Vcc = 5.0 V, lc = 2.0 mA         0.58         0.77         V           Small-Signal Current Gain         Ic = 2.0 mA, Vcc = 5.0 V, lc = 10 mA         125         900         I           NF         Noise Figure         Vcc = 5.0 V, lc = 200 µA, Ba = 2.0 kD, Ic = 10 mA         10         dB           Bw = 200 RJ         Collector-Emitter Saturation Voltage         Vcc = 5.0 V, lc = 200 µA, Ba = 0.58         0.77         V           Small-Signal Current Gain         Ic = 2.0 mA, Vcc = 5.0 V, Ic = 10 mA         10         dB         Bw = 200 RJ         Ide = 1.0 kHz, Ic = 10 MA         Ide = 1.0 kHz, Ic = 200 µA, Bw = 2.0 kD, Ic = 10 MA, Bw = 2.0 kD, Ic = 10 MA, Bw = 2.0 kD, Ic = 2.0 MA         Ide = 1.0 kHz, Ic = 2.0 MA         Ide = 1.0 kHz, Ic = 2.0 MA         Ide = 2.0 MA <t< td=""><td>ON CHARACTERISTICS           Impe         DC Current Gain         Vcc = 5.0 V, lc = 2.0 mA         548         110         820           Vector         State         420         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         100         800         548         100         800         548         100         800         548         100         800         548         100         800         100         100         100         100         100         100         100         100         100         100         100         100         100         100         100         <th< td=""><td>I<sub>CBO</sub></td><td>Collector Cutoff Current</td><td><math>V_{CB} = 30 \text{ V}, I_E = 0</math> <math>V_{CD} = 30 \text{ V}, I_E = 0, T_A = +150 \text{ °C}</math></td><td></td><td>15 5 0</td><td>nA u A</td></th<></td></t<>	ON CHARACTERISTICS           Impe         DC Current Gain         Vcc = 5.0 V, lc = 2.0 mA         548         110         820           Vector         State         420         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         110         800         548         100         800         548         100         800         548         100         800         548         100         800         548         100         800         100         100         100         100         100         100         100         100         100         100         100         100         100         100         100 <th< td=""><td>I<sub>CBO</sub></td><td>Collector Cutoff Current</td><td><math>V_{CB} = 30 \text{ V}, I_E = 0</math> <math>V_{CD} = 30 \text{ V}, I_E = 0, T_A = +150 \text{ °C}</math></td><td></td><td>15 5 0</td><td>nA u A</td></th<>	I <sub>CBO</sub>	Collector Cutoff Current	$V_{CB} = 30 \text{ V}, I_E = 0$ $V_{CD} = 30 \text{ V}, I_E = 0, T_A = +150 \text{ °C}$		15 5 0	nA u A
ONCHARACTERISTICS         hre       DC Current Gain       Vcc = 5.0 V, lc = 2.0 mA       548       110       200       450         Vccesati       Collector-Emitter Saturation Voltage       lc = 10 mA, lg = 0.5 mA       0.25       V         Vgc(on)       Base-Emitter On Voltage       Vcc = 5.0 V, lg = 2.0 mA       0.58       0.70       V         SMALL SIGNAL CHARACTERISTICS         hre       Small-Signal Current Gain       lc = 2.0 mA, Vcg = 5.0 V, lg = 2.0 mA       125       900         NF       Small-Signal Current Gain       lc = 2.0 mA, Vcg = 5.0 V, lg = 2.0 mA       125       900       I         NF       Small-Signal Current Gain       lc = 2.0 mA, Vcg = 5.0 V, lg = 2.0 µA, Rg	ONCHARACTERISTICS           hre         DC Current Gain         VCE = 5.0 V, Ic = 2.0 mA         548         110         220           VCE(Ball)         Collector/Emitter Saturation Voltage         Ic = 10 mA, Ig = 0.5 mA         0.60         V           VGE(Ball)         Collector/Emitter Saturation Voltage         Vc = 5.0 V, Ic = 2.0 mA         0.68         0.70         V           VBE(OT)         Base-Emitter On Voltage         Vc = 5.0 V, Ic = 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         Noise         Ic = 1.0 kHz         125         900         Ic           NF         Noise Figure         Vc = 5.0 V, Ic = 2.0 mA, Vc = 5.0 V, Ic = 0.0 µA, MA         10         dB           MF         Noise Figure         Vc = 5.0 V, Ic = 2.0 µA, MA         10         dB           MF         Noise Figure         Vc = 2.0 µA, MA         10         dB           MF         Noise Figure         Vc = 2.0 VA, MA         10         dB           MF         Noise Figure         Vc = 2.0 VA         10         dB           MF         Noise Figure         Vc = 2.0 VA         VC = 2.0 VA         10         dB           MA         MA         MA         MA         MA         MA			$V_{CB} = 50$ V, $T_{E} = 0$ , $T_{A} = 1150$ O		0.0	μΛ
DC Current Gain         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA         548 548A         110 10 220 548C         800 420           V <sub>CE(sal)</sub> Collector-Emitter Saturation Voltage         I <sub>c</sub> = 10 mA, I <sub>B</sub> = 0.5 mA         0.25         V           V <sub>BECON</sub> Base-Emitter On Voltage         V <sub>CE</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         V <sub>RE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 10 mA         0.58         0.77         V           NF         Noise Figure         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 µA, R, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 1.0 kHz, B = 0.0 µA, R = 2.0 kQ, f = 0.0 Hz, S = 0.0 µA, R = 0.0	DC Current Gain         V <sub>CE</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA         548         110         200           Stable         Collector-Emitter Saturation Voltage         I <sub>c</sub> = 10 mA, I <sub>g</sub> = 0.5 mA         0.25         V           V <sub>CE6a00</sub> Collector-Emitter Saturation Voltage         I <sub>c</sub> = 10 mA, I <sub>g</sub> = 0.5 mA         0.60         V           V <sub>GE(000</sub> Base-Emitter On Voltage         V <sub>CE</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         N <sub>1c</sub> = 1.0 kHz         10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         I <sub>1c</sub> = 1.0 kHz         10 mA         0.77         V           NF         Noise Figure         V <sub>EE</sub> = 5.0 V, I <sub>c</sub> = 2.0 µA, R <sub>g</sub> = 2.0 kQ, f = 1.0 kHz, B <sub>W</sub> = 2.0 Hz         10         dB           JWF         Noise Figure         V <sub>EE</sub> = 5.0 V, I <sub>c</sub> = 2.0 µA, R <sub>g</sub> = 2.0 kQ, f = 1.0 kHz, B <sub>W</sub> = 2.0 Hz         10         dB           JWF         Noise Figure         V <sub>EE</sub> = 5.0 V, I <sub>c</sub> = 2.0 µA, R <sub>g</sub> = 2.0 kQ, f = 1.0 kHz, B <sub>W</sub> = 2.0 Hz         10         dB           JWF         Noise Figure         V <sub>EE</sub> = 5.0 V, I <sub>c</sub> = 2.0 µA, R <sub>g</sub> = 2.0 kQ, f = 1.0 kHz, B <sub>W</sub> = 2.0 Hz         10         dB	ON CHAR	ACTERISTICS				
Vcc(sat)         Collector-Emitter Saturation Voltage         Ic = 10 mA, Is = 0.5 mA         200         450           Vsc(m)         Base-Emitter On Voltage         Vcc = 5.0 V, Ic = 2.0 mA         0.660         V           Vsc(m)         Base-Emitter On Voltage         Vcc = 5.0 V, Ic = 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         Nre         Small-Signal Current Gain         Ic = 2.0 mA, Vcc = 5.0 V, Ic = 200 µA, Rs = 2.0 kQ, If = 1.0 kHz         125         900           NF         Noise Figure         Vcc = 5.0 V, Ic = 200 µA, Rs = 2.0 UA, Rs = 2.0 UA, Rs = 2.0 KQ, If = 1.0 kHz, Bs = 2.0 kQ, If = 1.0 kHz, Starter Sta	Stable         110         220           VCE(sain)         Collector-Emitter Saturation Voltage         Ic = 10 mA, Ia = 5.0 mA         0.25         V           Value         D         10 mA, Ia = 5.0 mA         0.25         V           Value         Base-Emitter On Voltage         Vog = 5.0 V, Ig = 2.0 mA         0.58         0.70         V           Value         Signal Current Gain         Ic = 10 mA, Vog = 5.0 V, Ig = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         In e         Small-Signal Current Gain         Ic = 2.0 mA, Vog = 5.0 V, Ig = 200 µA, Rs = 2.0 mA         0.58         0.77         V           NF         Noise Figure         Vog = 5.0 V, Ig = 200 µA, Rs = 2.0 mA         125         900         I         I         1.0         dB           Weg = 5.0 V, Ig = 200 µA, Rs = 2.0 kQ, f = 1.0 kHz, Bw = 2.0 kQ, f = 1.0 kHz, Bw = 2.0 kQ, f = 1.0 kHz, Bw = 2.0 kQ, f = 2.0 kQ,	h <sub>FE</sub>	DC Current Gain	$V_{CE} = 5.0 \text{ V}, I_C = 2.0 \text{ mA}$ 548	110	800	
S48B         200         450           V <sub>CE(sat)</sub> Collector-Emitter Saturation Voltage         I <sub>c</sub> = 10 mA, I <sub>B</sub> = 0.5 mA         0.025         V           V <sub>BE(00)</sub> Base-Emitter On Voltage         V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         NF         Noise Figure         I <sub>c</sub> = 1.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 100 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub> = 5.0 V, I <sub>c</sub> = 2.0 mA, V <sub>ce</sub>	S488         200         450           V <sub>CE(stat)</sub> Collector-Emitter Saturation Voltage         Ic = 10 mA, Ig = 5.0 mA         0.25         V           V <sub>BE(on)</sub> Base-Emitter On Voltage         Vc = 5.0 V, Ic = 2.0 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         Vc = 5.0 V, Ic = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         Ic = 1.0 kHz         125         900         1           NF         Smail-Signal Current Gain         Ic = 1.0 kHz         126         900         1           NF         Noise Figure         Vc = 5.0 V, Ic = 200 µA, Re = 5.0 V, Ic = 5.0 V,			548A	110	220	
V <sub>CE(sa)</sub> Collector-Emitter Saturation Voltage         Ic = 10 mA, I <sub>B</sub> = 5.0 mA         0.00         V           V <sub>BE(00)</sub> Base-Emitter On Voltage         V <sub>cc</sub> = 100 mA, I <sub>B</sub> = 5.0 mA         0.60         V           SMALL SIGNAL CHARACTERISTICS         V <sub>cc</sub> = 5.0 V, I <sub>c</sub> = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         I <sub>c</sub> = 2.0 mA, V <sub>cc</sub> = 5.0 V, I <sub>c</sub> = 10 mA         125         900         1           NF         Noise Figure         V <sub>cc</sub> = 5.0 V, I <sub>c</sub> = 200 µA, R <sub>s</sub> = 2.0 kQ, I = 1.0 kHz         10         dB           B <sub>W</sub> = 200 Hz         UNIVERSITI TEKNIKAL MALAYSIA MELAKA         VIVERSITI TEKNIKAL MALAYSIA MELAKA	V <sub>CE(sal)</sub> Collector-Emitter Saturation Voltage         Ic = 10 mA, I <sub>B</sub> = 0.5 mA         0.02         V           Base-Emitter On Voltage         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 mA         0.60         V           SMALL SIGNAL CHARACTERISTICS         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 10 mA         0.58         0.77         V           SMALL SIGNAL CHARACTERISTICS         I <sub>c</sub> = 1.0 kHz         125         900         1         1         0.8           NF         Noise Figure         V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 µA, V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 2.0 µA, I <sub>A</sub> 10         dB           JUNIVERSITI TEKNIKAL MALAYSIA MELAKA         VCE = 5.0 V, I <sub>C</sub> = 2.0 µA, I <sub>A</sub> 10         dB			548B 548C	200 420	450 800	
$V_{BE[0n]}$ Base-Emitter On Voltage $V_{cg} = 5.0 \text{ V}, \ l_{c} = 2.0 \text{ mA}$ $0.58$ $0.70$ $V$ SMALL SIGNAL CHARACTERISTICS $h_{fe}$ Small-Signal Current Gain $l_{c} = 2.0 \text{ mA}, V_{Cg} = 5.0 \text{ V}, \ 125$ $900$ $f$ NFNoise Figure $V_{cg} = 5.0 \text{ V}, \ l_{c} = 2.0 \text{ µA}, \ R_{g} = 2.0 \text{ µA}, \ R_{$	Le 100 mA, la 5.0 mA         0.60         V           Vacio         Voc 5.0 V, lc 2.0 mA         0.58         0.70         V           SMALL SIGNAL CHARACTERISTICS         Imali-Signal Current Gain         Ic 2.0 mA, Voc 5.0 V, lc 200 µA, lc 10         125         900         Imali-Signal Current Gain         Ic 2.0 mA, Voc 5.0 V, lc 200 µA, lc 10         0.68         0.77         V           NF         Noise Figure         Voc 5.0 V, lc 200 µA, lc 200 µA, lc 10         0         dB	V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage	$I_{\rm C} = 10 \text{ mA}, I_{\rm B} = 0.5 \text{ mA}$		0.25	V
Vec         3.5 V, b         2.0 MA         0.30         0.70         V           SMALL SIGNAL CHARACTERISTICS         Vcc         5.0 V, b         125         900         1           NF         Noise Figure         Vcc         5.0 V, b         2.00 MA         0.77         V           MF         Noise Figure         Vcc         5.0 V, b         2.00 MA         125         900         1           MF         Noise Figure         Vcc         5.0 V, b         2.00 MA         100         dB           MW         Noise Figure         Vcc         5.0 V, b         2.00 MA         100         dB           MF         Noise Figure         Vcc         5.0 V, b         2.00 MA         100         dB           MW         2.00 MZ         Vcc         3.00 MA         3.00 MA         3.00 MA         3.00 MA           MF         Noise Figure         Vcc         4.00 MA         4.00 MA         4.00 MA         4.00 MA         4.00 MA           UNIVERSITI TEKNIKAL MALAYSIA MELAKA         MALAYSIA MELAKA         4.00 MA         4.00 MA         4.00 MA         4.00 MA         4.00 MA	Vector         Dissertinited Of Voldage         Vote = 5.0 V, Ic = 10 mA         0.33         0.77         V           SMALL SIGNAL CHARACTERISTICS         Image: The standard of the	M	Pasa Emittar On Valtage	$I_{\rm C} = 100 \text{ mA}, I_{\rm B} = 5.0 \text{ mA}$	0.59	0.60	V
SMALL SIGNAL CHARACTERISTICS         he       Small-Signal Current Gain       Ic = 2.0 mA, Vce = 5.0 V,       125       900       1         NF       Noise Figure       Vce = 5.0 V, Ic = 200 µA,       10       dB         ML       Supervision       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       dB         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       HC         Multiple       Vce = 5.0 V, Ic = 200 µA,       10       HC         Multiple       Vce = 5.0 V, Ic =	SMALL SIGNAL CHARACTERISTICS         he       Small-Signal Current Gain       Ic = 2.0 mA, Vce = 5.0 V, 125       900         NF       Noise Figure       Vce = 5.0 V, 1c = 200 µA, Re = 2.0 Kg, f = 1.0 KHz, Bw = 2.0 Kg, f = 1.0 K	VBE(on)	Base-Emilier On Voltage	$V_{CE} = 5.0 \text{ V}, I_C = 2.0 \text{ mA}$ $V_{CE} = 5.0 \text{ V}, I_C = 10 \text{ mA}$	0.58	0.70	V
SMALL SIGNAL CHARACTERISTICS         hre       Small-Signal Current Gain       Ic = 2.0 mA, Vce = 5.0 V, 125       900         NF       Noise Figure       Vce = 5.0 V, 1c = 200 µA, Res = 2.0 kQ, f = 1.0 kHz, Bw = 200 Hz       10       dB         Juniversity       Main and the second	SMALL SIGNAL CHARACTERISTICS         hr       Small-Signal Current Gain       Ic = 2.0 mA, Vce = 5.0 V, 125       900         NF       Noise Figure       Vce = 5.0 V, 1c = 200 µA, Rs = 2.0 kQ, f = 1.0 kHz, Bw = 200 Hz       10       dB         JUNIVERSITI TEKNIKAL MALAYSIA MELAKA		A				
hre       Small-Signal Current Gain       Ic = 2.0 mA, Voe = 5.0 V, Ic = 200 µA,       125       900         NF       Noise Figure       Voe = 5.0 V, Ic = 200 µA,       10       dB         Bw = 200 Hz       Juniversity       Juniversity       Juniversity       Juniversity         UNIVERSITI TEKNIKAL MALAYSIA MELAKA       MALAYSIA MELAKA	hre         Small-Signal Current Gain         I <sub>c</sub> = 2.0 mA, V <sub>CE</sub> = 5.0 V,         125         900           NF         Noise Figure         V <sub>CE</sub> = 5.0 V, I <sub>c</sub> = 200 µA,         Rs         10         dB           Bw = 200 Hz         UNIVERSITI TEKNIKAL MALAYSIA MELAKA         UNIVERSITI TEKNIKAL MALAYSIA MELAKA	SMALL S	IGNAL CHARACTERISTICS				
NF       Noise Figure       I = 1.0 KHZ       I 0       dB         Rs = 2.0 kQ, f = 1.0 kHz, Bw = 200 Hz       I 0       dB         UNIVERSITI TEKNIKAL MALAYSIA MELAKA	NF       Noise Figure       Image: I	h <sub>fe</sub>	Small-Signal Current Gain	$I_{\rm C} = 2.0 \text{ mA}, V_{\rm CE} = 5.0 \text{ V},$	125	900	
الوينيون سيني تنكيكي مليسيا ملاك Bw = 200 Hz UNIVERSITI TEKNIKAL MALAYSIA MELAKA	الوينونررسيني تيكينيكيل مليسيا ملاك Bw = 200 Hz	NF	Noise Figure	f = 1.0  KHz		10	dB
لوينورسيني نيڪنيڪل مليسيا ملاك UNIVERSITI TEKNIKAL MALAYSIA MELAKA	لوينونرسيني تيڪنيڪل مليسيا ملاك UNIVERSITI TEKNIKAL MALAYSIA MELAKA			$R_{s} = 2.0 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ ,		10	GD
اونيونرسيتي تيڪنيڪل مليسيا ملاك UNIVERSITI TEKNIKAL MALAYSIA MELAKA	اونيونرسيتي ٽيڪنيڪل مليسيا ملاك UNIVERSITI TEKNIKAL MALAYSIA MELAKA			B <sub>W</sub> = 200 Hz			
UNIVERSITI TEKNIKAL MALAYSIA MELAKA	UNIVERSITI TEKNIKAL MALAYSIA MELAKA		5000000				
UNIVERSITI TEKNIKAL MALAYSIA MELAKA	UNIVERSITI TEKNIKAL MALAYSIA MELAKA						
UNIVERSITI TEKNIKAL MALAYSIA MELAKA	UNIVERSITI TEKNIKAL MALAYSIA MELAKA			••			
			IINIVERSITI TEKNI		MEI	ΔΚΔ	