UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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FINAL YEAR PROJECT REPORT

Development and Analysis of Three Phase Seven Level Trinary DC Source Multilevel Inverter

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FINAL YEAR PROJECT REPORT

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Faculty of Electrical Engineering

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(2014)

DECLARATION

"I hereby declared that this report is a result of my own work except for the excerpts that have been cited clearly in the references"

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DEDICATION

Specially dedicated to my family

ACKNOWLEDGEMENT

First and foremost, thanks to Allah for giving me this healthy body that enables me to devoted to the community as well as gaining new knowledge, experience and able to finish this report in the frame of time. Nothing can be done except with the permission of Allah.

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ABSTRACT

Inverter is electronic equipment used to convert Direct Current (DC) supply to Alternating Current (AC). There are many types of inverter exists and among all, multilevel inverter produce less harmonic compared to the conventional two level inverter. Harmonic do no useful work and it degrades the power quality of the electrical system also sometimes can cause malfunction of equipment. By using multilevel inverter, total harmonic distortion can be reduced by increase the output voltage level. However, for multilevel inverter, increasing of output voltage level will cause additional components to the circuit. This will increase the implementation cost, the inverter will be more bulky and not practical to implement. In this research, analysis of Three Phase Trinary Multilevel Inverter is conducted. Trinary multilevel inverter has the ability to produce high output voltage level with minimum components usage. The analysis is conducted using MATLAB/Simulink simulation tools for Three Phase Square Inverter, Three Phase Quasi Inverter and Three, Five, Seven and Nine Level of Trinary Multilevel Inverter, meanwhile for analysis on hardware is only focus on Three Phase Seven Level DC Source MLI. Different types of load are connected to the inverter to analyze the output voltage and current characteristics for all inverter mentioned above. Data gathered from the simulation and hardware is compared in terms of total harmonic distortion. The comparison shows that, the voltage THD is decrease as the number of level is increase. Three Level Trinary MLI produce 31.08% of voltage THD meanwhile for Nine Level Trinary MLI, the voltage THD reduce to 15.12%. This proved that the output voltage level of Trinary MLI

is significantly affected to the voltage THD which is higher level of Trinary MLI will produce lower voltage THD. Hardware and simulation result also shows that for RL load, the current THD is less than using R load.

ABSTRAK

Penyongsang adalah sejenis peralatan elektronik yang digunakan untuk menukarkan bekalan Arus Terus (AT) kepada Arus Ulang Alik (AU). Terdapat banyak jenis penyongsang wujud dan diantaranya, penyongsang pelbagai peringkat menghasilkan kurang harmonik berbanding penyongsang konvensional dua peringkat. Harmonik tidak mendatangkan sebarang faedah dan ia menyebabkan kualiti kuasa dalam sistem elekrik menjadi rendah disamping kadang kala boleh menyebabkan kepada kerosakan peralatan. Dengan menggunakan penyongsang pelbagai peringkat, jumlah herotan harmonik boleh dikurangkan dengan menambah peringkat voltan keluaran. Walau bagaimanapun, bagi penyongsang pelbagai peringkat, meningkatkan tahap voltan keluaran akan menyebabkan komponen yang digunakan juga akan bertambah. Ini akan meningkatkan kos pelaksanaan dan menyebabkan penyongsang menjadi lebih besar dan tidak praktikal untuk dilaksanakan. Dalam kajian ini, analisis penyongsang pelbagai peringkat Trinary untuk tiga fasa dijalankan. Penyongsang pelbagai peringkat Trinary mempunyai keupayaan untuk menghasilkan peringkat voltan keluaran yang lebih tinggi dengan penggunaan komponen yang minimum. Analisis ini dijalankan menggunakan alat simulasi MATLAB/Simulink untuk Penyongsang Persegi tiga fasa, Penyongsang Separa tiga fasa dan Penyongsang Trinary berperingkat tiga, lima, tujuh dan sembilan. Manakala untuk analisis untuk perkakasan hanya difokuskan pada Penyongsang Trinary tiga fasa berperingkat tujuh. Pelbagai jenis beban disambungkan pada penyongsang untuk menganalisis ciri-ciri voltan dan arus keluaran penyongsang tersebut. Data yang

dikumpul dari simulasi dibandingkan dari segi jumlah herotan harmonik. Perbandingan ini menunjukkan bahawa jumlah herotan harmonik voltan berkurangan apabila tahap tingkatan penyongsang meningkat. Penyongsang Trinary berperingkat tiga menghasilkan 31.08 % jumlah herotan harmonik voltan sementara itu, bagi penyongsang Trinary berperingkat sembilan, jumlah herotan harmonik voltan berkurangan kepada 15.12 %. Ini membuktikan bahawa peringkat keluaran voltan penyongsang Trinary ketara mempengaruhi jumlah herotan harmonik voltan, dimana penyongsang Trinary berperingkat tinggi akan menghasilkan jumlah herotan harmonik yang lebih rendah. Keputusan perkakasan dan simulasi juga menunjukkan bahawa jumlah herotan harmonik arus untuk beban RL adalah lebih rendah berbanding beban R.

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LIST OF ABREVATIONS

AC	- Alternating Current
CHBMLI	- Cascaded H-Bridge Multilevel Inverter
CM	- Common Mode
DC	- Direct Current
EMI	- Electromagnetic Interference
FCMLI	- Flying Capacitor Multilevel Inverter
IEC	- International Electrotechnical Commission
IGBT	- Insulated Gate Bipolar Transistor
MLI	- Multilevel Inverter
NPCMLI	- Neutral Current Clamped Multilevel Inverter
OHS PWM	- Optimized Harmonic Stepped Pulse Width Modulation
PCB	- Printed Circuit Board
PQ	- Power Quality
PWM	- Pulse Width Modulation

RMS - Root Mean Square

SHE PWM - Selective Harmonic Eliminated Pulse Width Modulation

SPWM - Sinusoidal Pulse Width Modulation

THD - Total Harmonic Distortion

UPS - Uninterruptible Power Supply

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CHAPTER 1

INTRODUCTION

1.1 Overview

Inverter is an electrical power converter that changes Direct Current (DC) to Alternating Current (AC). The converted AC can be at any required voltage and frequency with the use of appropriate switching and control circuits. For example, the most common method to convert DC supply to AC supply for renewable energy is using inverter. There are several types of inverters exists and among them, multilevel inverters (MLI) produce less harmonic distortion compared to the conventional two level inverters. As the level of the inverter goes higher, the total harmonic distortion will lesser. The main problem of designing conventional MLI is the complexity of the circuit and used of component such as switching devices. As level of MLI getting higher, the usage of component will be increase. In this research, the seven level of MLI is implemented in the small scale. The concept of Cascaded H-Bridge MLI using Trinary DC Source is being used. The selection of this concept is based on their simplicity, easy to control and fewer components used which will reduce the implementation cost. The switching mode will be controlled by gate drivers which receive the command from microcontroller using simple modulation technique. MATLAB/Simulink will be used as simulation tools to generate the voltage and current harmonic distortion of the MLI to be compare with the hardware implementation of MLI.

1.2 Problem Statement

Renewable energy has become an alternative power sources in recent years. There are various renewable energy sources that can be used to generate electricity such as solar, geothermal, wind and etc. Renewable energy application will require inverters act as their interfacing component. Conventional two levels inverter only generates two stages of output voltage, while MLI can provide more, depends on their designed structure. Therefore, the conventional two levels inverter provides higher harmonic distortion on the output voltage. Effect of harmonic in power system can be categories into two categories which is long term and short term effect. Short term effects often go undetected and are usually related to increased resistive losses or voltage stresses, and for long term effects are usually noticeable and are related to excessive voltage distortion. The most devices that can produce a high harmonic distortion to the power distribution system are devices that can produce heat such as ovens and furnaces. In order to minimize the harmonic distortion in the system, multilevel inverter is used. Multilevel inverters are more suitable for this application because of their low harmonic distortion of the generated output voltage compare to the conventional one.

1.3 Objective

The objectives of this study are:

1. To simulate and analyse a Three Phase Trinary DC Source Multilevel Inverter
2. To design and develop a Three Phase Seven Level Trinary DC Source Multilevel Inverter

1.4 Scope of Research

The scope of this research is to conduct simulation of the conventional Three Phase Square and Quasi Inverter and also Three Phase Seven Level Trinary DC Source MLI. The simulation will be conducted using MATLAB/Simulink software. The purpose of this simulation is to compare the performance of both inverters in term of total harmonic distortion and number of components used. The load that will be used for this simulation is a various combination of fixed R, L and C load.

After simulation result is obtained, the experimental prototype of the Three Phase Seven Level Trinary DC Source MLI will be developed. The power circuit will be consists of DC/DC boost converter IQ0515SA that used to step up the DC source of the inverter to desired value, two sets of Cascaded H-bridge power switches consists of Insulated Gate Bipolar Transistor (IGBT) type IHW30N90T and combination of RL load. As for the control scheme of the power switches, the step modulation algorithm will be uploaded to the Arduino Mega 2560 microcontroller. As the signal from the microcontroller is at logic level and the maximum output voltage it can produce is up to 5 *V* only, it does not have the ability to turn on the IGBT switches which require the range of 0 to 15 *V*. Therefore, the opto-coupler gate driver HCPL-3120-000E is used as the interface component between the microcontroller and power circuits.

Finally, after completion of the hardware development, the data achieve from hardware will be analyzed and compared with the previous obtained simulation result from MATLAB/Simulink.

1.5 Significant of Research

The significant of this research is the development of the Three Phase Seven Level Trinary DC Source MLI will produce lower total harmonic distortion compared to the conventional Square and Quasi Inverter.

As for the hardware part, it been designed and will be fully developed from nothing by using several desired component. The Printed Circuit Board (PCB) board also is specially designed to enhance the hardware implementation.

1.6 Report Outline

This report contains of five chapters start with the introduction chapter that consists of brief explanation of the research which Three Phase Seven Level Trinary DC Source MLI and why it is proposed. The objectives, scope and the significant of the research also presented in this chapter. Other chapters in this report are arranged as follow:

Chapter 2 discuss about the literature review for this research. This including explanation of power quality consists of harmonic distortion and standards. The various types of MLI topologies and control schemes also will be described in this chapter.

Chapter 3 discuss about the methodology for this research. All the methods used in accomplishing this research are explained and all the flowchart, milestone and Gantt Chart are presented in the earlier section of this chapter. The concept of Seven Level Trinary MLI also will be discussed in details with the help of particular figure, table and block diagram. The MATLAB/Simulink simulation structure for simulation section and circuit design for hardware implementation also will be presented.

Chapter 4 gathered all the results get from the simulations experimental setup of the hardware. Data taken from the simulation are consists of data from the conventional and Trinary MLI. The result gathered is discussed in details in this chapter.

Chapter 5 shows the summary of this research and the further recommendation of the research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter will discuss the literature review conducted in order to gain enough information that can be used to complete the research. All the data include in this chapter are taken from journals, thesis, books and any academic articles that are related to the research topic and will be clearly cited. The power quality knowledge, harmonic definition, harmonic standard, common inverter topologies and the control schemes are discussed in subsequences so that it can be clearly understood. The related previous work such as Square and Quasi Inverter also presented.

2.2 Power Quality

Power Quality (PQ) is a term that embraces all aspects associated with amplitude, phase and frequency of the voltage and current waveforms existing in a power circuit. Adverse PQ environment may result from transient conditions developing in the power circuit, the installation of one or more non-linear loads of relatively large rating or large numbers of non-linear loads of low rating [1-3].

Many years ago, apart from power factor and flicker concern, PQ problems were confined almost entirely to the sphere of regulated, public utilities. However, over the last decade, the issue of PQ has gained renewed interest due to the increasing use of loads sensitive to service quality such as computers, industrial drives, communications and medical equipment. In its present form, PQ is an even more complex problem than in the past because the new loads are not only sensitive to service quality but also responsible for affecting adversely the quality of power supply. It is widely acknowledged that both customer and utility equipment will suffer undue stress in an unfriendly PQ operating environment. PQ disturbances at the utility level may result in the malfunction of remote control, protective devices and energy metering, overheating of cables, transformers and rotating machineries. PQ disturbances in the customer's premises may result in the loss of computer data, due to voltage sags with duration of only a few milliseconds. Even shorter voltage sags may cause the tripping of industrial drives. This has prompted professional bodies to enact recommended practices in order to limit the severity and number of disturbances to customer equipment [1-3].

A large number of PQ disturbances have been reported in the open literature, with some of them being transient in nature and others being related to periodic, steady state operation. There is no general agreement between the various authors on a unique classification of PQ disturbances but some of the more common disturbances are voltage and current harmonics, voltage sags, swells, electric noise, impulses, notches and flicker [1-3].

2.2.1 Harmonics in Electrical System

Harmonics are actually a mathematical model of the real world distorted sinusoidal waveforms. It is simply a technique to analyze distorted AC waveforms. All complex AC voltage or current waveforms can be represented by a series of sinusoidal wave of various frequencies that are integer multiples of the fundamental frequency. On a 50 *Hz* fundamental frequency system, this could include the third, fifth, seventh order harmonics and so on. The losses due to the I^2R component are due to conductor heating and the skin effect. In particular, the third harmonics, as well as the fifth and the seventh harmonics have a significant contribution [1-3].

In an electrical distribution system, utilities normally generate almost perfect sinusoidal voltage and current. However, these perfect sinusoidal waveforms do not hold at consumer ends due to the widespread utilization of non-linear loads draw decidedly non-sinusoidal current. These loads have distorted the electrical systems voltage and current waveforms as they introduce harmonics into the electrical system. Unlike fundamental, harmonics provide no usable power to do work. They simply take up the capacity of electrical system. When presented in sufficient quantities, harmonics do not only disturb loads that are sensitive, but also may cause many undesirable effects to the power system. As a result, harmonic studies are become more imperative [1-3].

2.2.2 Total Harmonic Distortion (THD) Measurement

In performing harmonic analysis on a power system, it is important to determine how much distortion is presented in the waveform. This distortion is called THD, a measure to identify the amount of harmonics distortion in a waveform, usually expressed in percentages.

$$THD_V = \frac{\sqrt{\sum_{h=3,5,7..}^{\infty} V_h^2}}{V_1} \times 100\% \quad (2.1)$$

$$THD_I = \frac{\sqrt{\sum_{h=3,5,7..}^{\infty} I_h^2}}{I_1} \times 100\% \quad (2.2)$$

Where V_1 and I_1 are the fundamental voltage and current, V_h and I_h are the harmonics voltage and current. This index is defined as the ratio of the total Root Mean Square (RMS) value of the harmonic components to the RMS value of the fundamental component and is used to measure the deviation of a periodic waveform containing harmonics from a perfect sine wave. For a perfect sinusoidal wave at fundamental frequency, the THD is zero. Similarly, the measures of individual harmonic distortion for voltage and current at *h*-th order are defined as V_h/V_1 and I_h/I_1, respectively [1-3].

2.2.3 Harmonic Standards

In view of the widespread use of power electronic equipment connected to utility systems, various national and international agencies have proposed limits on harmonic current injection to the system by this equipment, to maintain good power quality. As a result, the following standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltage distortion at various harmonic frequencies [2].

2.2.3.1 IEC Harmonic Standard 555-2

This standard is prepared by the International Electrotechnical Commission (IEC) and accepted by its National Committees of the following countries which are Austria, Australia,

Belgium, Canada, Egypt, Finland, France, Germany, Hungary, Ireland, Japan, Korea, Netherlands, Norway, Poland, Romania, South Africa, Switzerland, Turkey and United Kingdom.

IEC 555-2 provides harmonic current limits for all electrical and electronic equipment having and input current up to 16 *A*, intended to be connected to public distribution systems of nominal 50 *Hz* or 60 *Hz* frequency. The voltages covered are 220-240 *V* single phase and 380-415 *V* three phase. The equipment is classified into four groups. Class A, for balanced three phase equipment and anything else that does not fit into another group, Class B, for any portable tools, Class C, for lighting equipment and Class D, for equipment having an input current with a special wave shape.

The harmonic limits are defined in absolute values, irrespective of the equipment's power rating. Below gives the maximum permissible harmonic current in amperes in these four groups according to the IEC 555-2.

Table 2.1: IEC 555-2 Harmonic Current Content Limits

	Odd Harmonics							**Even Harmonics**			
Harmonic Order (n)	3	5	7	9	11	13	15<n<39	2	4	6	8<n<40
Max. Permissible Harmonic Current (A)	2.30	1.14	0.77	0.40	0.33	0.21	0.15x15/n	1.08	0.43	0.30	0.23x8/n

2.2.3.2 EN 60555-2

"The Limitation of Disturbances in Electricity Supply Networks caused by Domestic and Similar Appliances Equipped with Electronic Devices," European Norm prepared by Comite Europeen de Normalisation Electrotechnique, CENELEC. This in fact is an adoption

of the IEC 555-2 standard to the CENELEC member countries and will be same for all countries in the European Union.

2.2.3.3 IEEE Standard 519-1992

"IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems,". This guide applies to every types of static power converters used in commercial and industrial power systems. The problems involved in the harmonic control and reactive compensation of such converters are addressed, and an application guide is provided. Limits of disturbances to the ac power distribution system that affect other equipment and communications are recommended. This guide is not intended to cover the effect of radio frequency interference.

2.3 Multilevel Inverter (MLI)

Circuit that convert DC to AC is called inverter. Specifically, inverter used to transfer power from a DC source to an AC load. In other applications, the objective is to create an AC voltage when only a DC voltage source is available. Inverters are often used in applications such as adjustable-speed AC motor drives, interfacing renewable energy sources such as photovoltaic to the electric power grid, Uninterruptible Power Supply (UPS) and running AC appliances from an automobile battery [4-8]. A MLI is a more powerful inverter. Recently, there are increasingly used of MLI in medium and high power applications. The concept of MLI has been introduced since 1975 essentially consist of three-level of staircase waveform [9-12]. The concept of a MLI is to achieve higher power by using series of power semiconductor switches with several lower voltage DC sources. The multiple DC voltage sources are supplied either by capacitors, batteries and renewable energy voltage sources or the combination of both.

The MLI power switches are turned on sequentially according to the control scheme to produce the desired staircase voltage output. The rated voltage of the power switches are depends on the DC voltage sources connected.

A MLI has several advantages over a conventional inverter such as low power dissipation on power switches, low switching losses, low harmonic contents, low Electromagnetic Interference (EMI) outputs, lower *dv/dt* ratio, smaller Common Mode (CM) voltage and can be operate at both fundamental switching frequency and high switching frequency [9-12].

Unfortunately, MLI do have some drawbacks and one that particular is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a MLI, each switch requires a related control scheme and gate drive circuit. This may cause the overall system to be more expensive and complex [9,10].

2.3.1 Multilevel Inverter Topologies

In recent years, several MLI topologies have been developed. The most common MLI topologies are Diode Clamped MLI or Neutral Point Clamped MLI (NPCMLI), Capacitor Clamped MLI or Flying Capacitor MLI (FCMLI) and Cascaded H-Bridge MLI (CHBMLI). There are several other topologies that have been developed according to the combination of these common topologies such as Trinary DC Source MLI, Generalized MLI, Soft-Switched MLI, Mixed Level MLI and MLI by The Connection of Three Phase Two Level Inverters [9,10].

2.3.1.1 Diode Clamped/ Neutral Point Clamped Multilevel Inverter

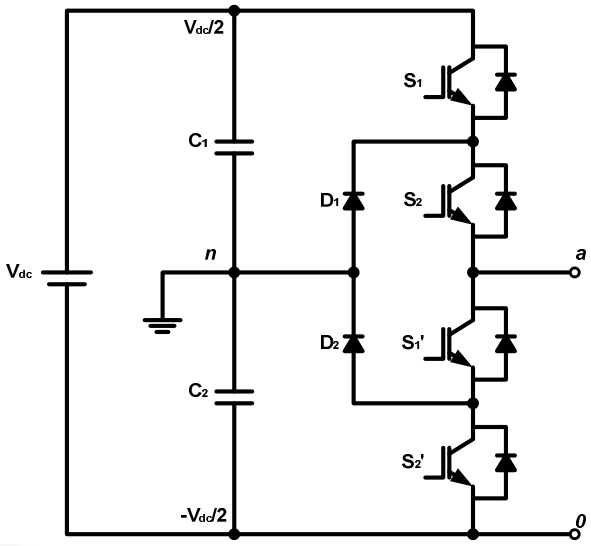


Figure 2.1: Three Level Diode Clamped MLI

Figure 2.1 shows the basic structure of a Three Level Diode-Clamped MLI. It is proposed by Nabae, Takashi and Akagi in 1981 named as Neutral Point Clamped MLI (NPCMLI) [9]. In this circuit, two series-connected bulk capacitors, C_1 and C_2 are used to split the DC-bus voltage into three levels. The *n* which is at the middle point of the two capacitors can be defined as neutral point. The single phase to neutral output voltage, V_{an} has three states which are $V_{dc}/2$, *0* and $-V_{dc}/2$. For Three Level Diode Clamped MLI, a set of two power switches is turned on at any given period of time. For example, to produce voltage level of $V_{dc}/2$, switches S_1 and S_2 need to be closed simultaneously, for voltage level of $-V_{dc}/2$, switches S_1' and S_2' need to be closed simultaneously, and for the *0* voltage level, S_2 and S_1' need to be closed simultaneously.

Table 2.2: Three Level Diode Clamped MLI switching states

Voltage V_{an}	**Switching State**			
	S_1	**S_2**	**S_1'**	**S_2'**
$V_2 = V_{dc}/2$	1	1	0	0
$V_1 = 0$	0	1	1	0
$V_0 = -V_{dc}/2$	0	0	1	1

The main components that make this circuit differ from a conventional inverter are D_1 and D_1'. These two diodes act as a clamper, to clamp the switch voltage to half of the DC-bus voltage level. When both S_1 and S_2 are closed, D_1' used to balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_2. The output voltage of V_{an} is in three level staircase AC forms.

Higher level of diode clamped multilevel inverter requires more devices to form the desired level of the inverter. If m is assumed as the total number of level for the multilevel inverter, the number of power switches (P_s), capacitors at DC side (C_{dc}), freewheeling diode (f_d) and clamping diode (C_d) can be determined using the following equations.

$$P_s = 2(m-1) \tag{2.3}$$

$$C_{dc} = m-1 \tag{2.4}$$

$$f_d = 2(m-1) \tag{2.5}$$

$$C_d = (m-1).(m-2) \tag{2.6}$$

The above equation also illustrate that the number of diodes required is quadratically related to the number of level desire. Therefore, the increase in number of level makes the topology quite bulky and impractical to implement. Moreover, the Diode Clamped MLI is

efficient in fundamental frequency switching which will cause the voltage and current total harmonic distortion to be increased.

2.3.1.2 Capacitor Clamped/ Flying Capacitor Multilevel Inverter

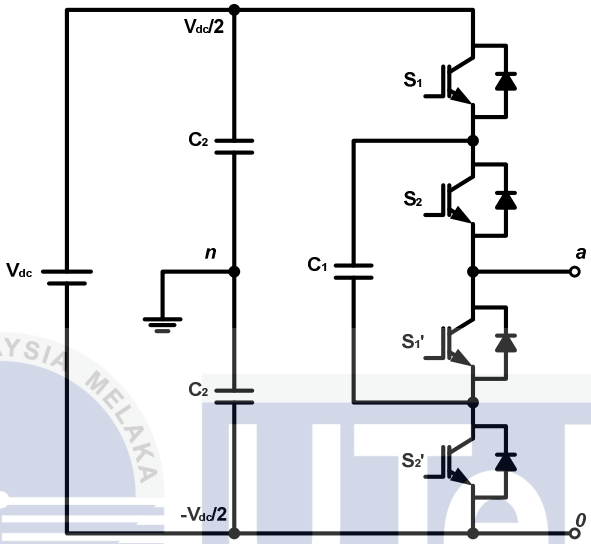


Figure 2.2: Three Level Capacitor Clamped MLI

The fundamental structure of Three Level Capacitor Clamped MLI is shown in Figure 2.2. This topology has been proposed as an alternative to the Diode Clamped MLI by Meynard in 1992 [9]. The topology also named as Flying Capacitor MLI. The clamping diode in Diode Clamped MLI is replaced by independent capacitors but the function of the capacitor is still same which is to clamp the device voltage to one capacitor voltage level. This MLI provides a three levels for single phase to neutral output voltage, V_{an} which are $V_{dc}/2$, 0 and $-V_{dc}/2$. As the Diode Clamped MLI, this topology requires two power switches to be closed simultaneously. For example, switches S_1 and S_2 need to be close to produce voltage level of $V_{dc}/2$. For $-V_{dc}/2$, switches S_1' and S_2' need to be closed and either pair (S_1, S_1') or (S_2, S_2') needs to be closed

for the *0* voltage level. When S_1 and S_1' are closed, the clamping capacitor C_1 is charged and is discharged when S_2 and S_2' are closed. If the proper selection of the *0*-level switch combination is made, the charge of C_1 can be balanced.

Table 2.3: Three Level Capacitor Clamped MLI switching states

Voltage V_{an}	**Switching State**			
	S_1	**S_2**	**S_1'**	**S_2'**
$V_2 = V_{dc}/2$	1	1	0	0
$V_1 = 0$	1	0	1	0
	0	1	0	1
$V_0 = -V_{dc}/2$	0	0	1	1

Similar to diode clamping, the higher level of the Capacitor Clamped MLI requires a large number of bulk capacitors to clamp the voltage. Provided that the main power switch is the same as the voltage rating of each capacitor so the number of power switches (P_s), capacitors at DC side (C_{dc}) and clamping capacitors (C_c) for an *m*-level inverter can be determined by the following equations.

$$P_s = 2(m-1) \tag{2.7}$$

$$C_{dc} = m-1 \tag{2.8}$$

$$C_c = ((m-1).(m-2))/2 \tag{2.9}$$

Preventing the filter demand and controlling the active and reactive power flow besides phase redundancies are the most important advantages of this Capacitor Clamped MLI topology. However, the increment in the inverter level will block the accurate charging and discharging control of capacitor. Furthermore, increase in the number of capacitor also will

increase the cost of the inverter and the device will be more enlarged due to the bulky capacitor.

2.3.1.3 Cascaded H-Bridge Multilevel Inverter

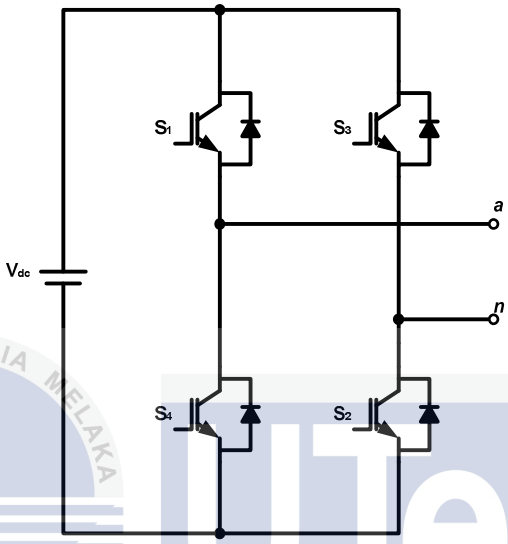


Figure 2.3: Three Level Cascaded H-Bridge MLI

Figure 2.3 shows the last structure of the most common topologies for MLI which is Three Level Cascaded H-Bridge MLI topology. This configuration recently becomes very popular in the variable speed drive applications due to its unique structure that does not require any clamping diode or capacitor [13]. This inverter consists of four units of power switches connected in H-bridge form fed by the independent voltage source. This is where the inverter got their name. This inverter can generate three levels staircase waveform of $+V_{dc}$, 0 and $-V_{dc}$ depends on the status of the particular power switches. Same as the previous explained topology, this inverter also need two power switches to be closed simultaneously to produce the desired level of output voltage, V_{an}. For example, to produce $+V_{dc}$, switch S_1 and

S_4 needs to be closed. For $-V_{dc}$, switch S_2 and S_3 needs to be closed and for *0*-level voltage, either the combination of S_1 and S_3 or S_2 and S_4 can be closed. The S_1 and S_2 or S_3 and S_4 switch can never be closed simultaneously. If this happen, can leads to damage of the circuit due to the short circuit.

Table 2.4: Three Level Cascaded H-Bridge MLI switching states

Voltage V_{an}	**Switching State**			
	S_1	**S_2**	**S_3**	**S_4**
$V_2 = V_{dc}$	1	1	0	0
$V_1 = 0$	1	0	1	0
	0	1	0	1
$V_0 = -V_{dc}$	0	0	1	1

Higher level of this type of MLI requires additional H-bridge power switches with independent source. For example, the Five Level Cascaded H-Bridge MLI will have two H-bridge circuit and two independent sources. The outputs of the different level of the H-bridge inverter are connected in series such that the desired multilevel inverter output is the sum of that particular H-bridge circuit. The output voltage for an *m*-level can be defined using the following equation with (*s*) is the number of independent source. Besides, the number of power switches (P_s) also can be determined.

$$m = 2s + 1 \tag{2.10}$$

$$P_s = 2(m - 1) \tag{2.11}$$

Among all the topologies described above, the Cascaded H-Bridge MLI used the less number of components [13]. It does not need any clamping diode or capacitor hence making it not bulky as the other two topologies for higher level of output voltage. Another advantage of

Cascaded H-Bridge MLI is the circuit layout flexibility. By adding or removing of the H-bridge circuit, the number of output voltage level can be easily adjusted.

2.3.2 Multilevel Inverter Control Schemes

The control schemes or control strategies of the MLI are also important to identify the efficiency parameters such as switching losses. The MLI control schemes are based on the fundamental and high switching frequency. There are several well-known control schemes of the multilevel inverter such as Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM) and Space Vector Pulse Width Modulation (SVM).

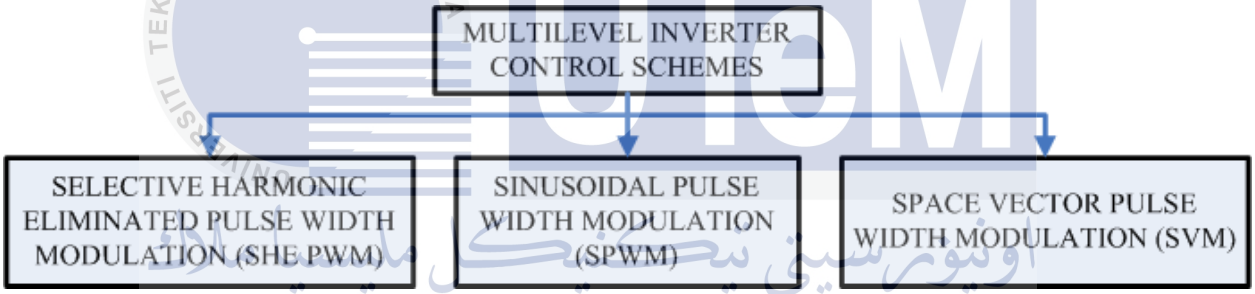


Figure 2.4: Classification of MLI Control Schemes

2.3.2.1 Sinusoidal Pulse Width Modulation (SPWM)

In Sinusoidal Pulse Width Modulation (SPWM), to get the gate signal for the MLI switching control, a sinusoidal reference voltage waveform is compared to the triangle carrier waveform in an analog or logic comparator devices. To minimize the switching losses hence increase the performance of MLI, the SPWM control method with fundamental frequency was

proposed [9]. There are two types of switching for SPWM which are SPWM with Bipolar Switching and SPWM with Unipolar Switching [14].

For Bipolar Switching, their basic generator control circuit is shown in Figure 2.5. The sinusoidal reference voltage V_r is compare with the triangular carrier signal V_c to produce bipolar switching signal.

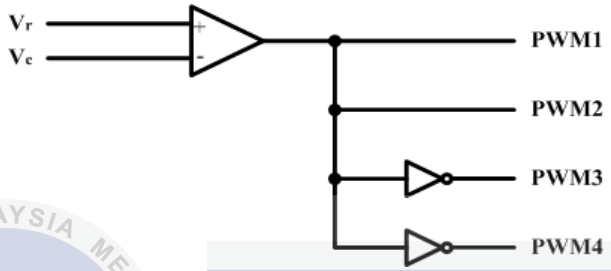


Figure 2.5: SPWM with Bipolar Switching Generator

The output generated signal for bipolar switching is cause by the comparison of V_r and V_c. The compared signal of these two signals and the output waveform produced are illustrated in Figure 2.6.

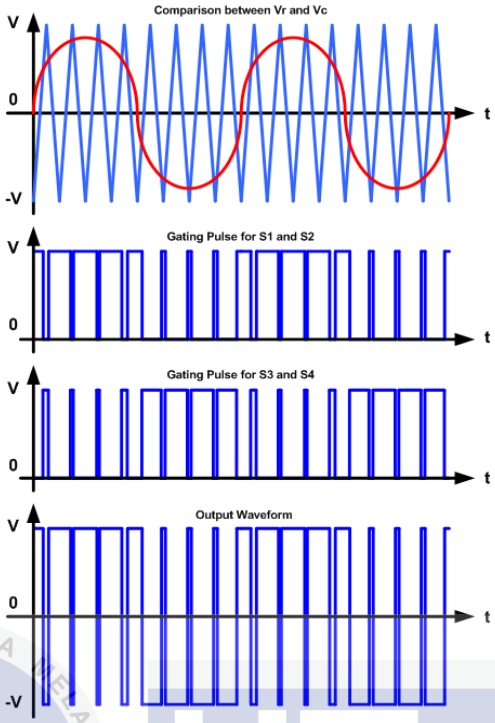


Figure 2.6: SPWM with Bipolar Switching Waveform

For Unipolar Switching, their basic generator control circuit is shown in Figure 2.5. The sinusoidal reference voltage V_r is also compare with the triangular carrier signal V_c but this time there is two V_r waveform. The other V_r is shifted 180 degree to another to produce unipolar switching signal.

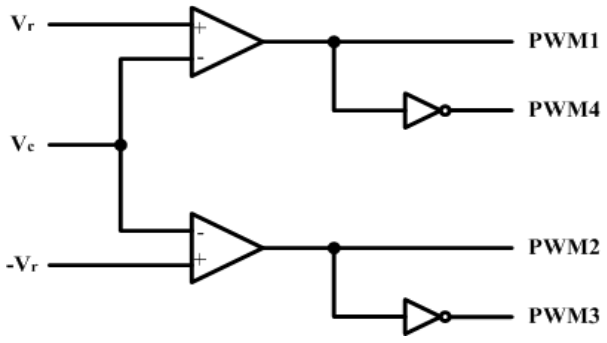


Figure 2.7: SPWM with Unipolar Switching Generator

The output generated signal for unipolar switching is cause by the comparison of two V_r and V_c. The compared signal of these two signals and the output waveform produced are illustrated in Figure 2.8.

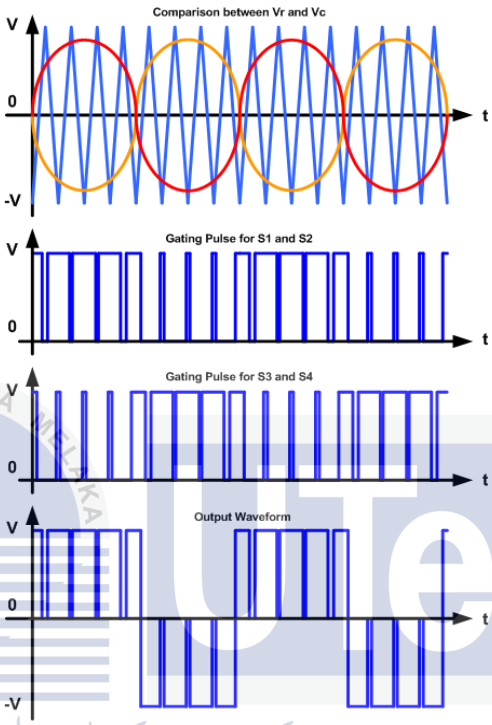


Figure 2.8: SPWM with Unipolar Switching Waveform

SPWM known as the most popular technique among others applied in multilevel inverters due to its advantages such as easy implementation, lower harmonic outputs compare to other technique and low switching losses. The desired line voltage frequency of the inverter output is depends on the sinusoidal modulating signals frequency [14].

2.3.2.2 Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM)

The Selective Eliminated Pulse Width Modulation (SHE PWM) technique normally applied in three-level conventional inverter circuits. This technique is proposed by Patel in

1974 based on the fundamental frequency switching theory and dependent on the elimination of defined harmonic content orders [9]. The objective of this method is to eliminate harmonic orders by defining the switching angles and to obtain the output voltage Fourier series expansion [15].

By using this technique, the lowest frequency harmonics are chosen by properly selecting angles among different level inverters for elimination and additional filter circuits can be used to remove the high frequency harmonics components. In order to ensure the number of eliminated harmonics at a constant level, all switching angles must be less than $\pi/2$. The main disadvantage of this modulation strategy is it provides a narrow range of modulation index [15].

In the application of SHE PWM, look up table in an independent memory of microprocessor is used to save the possible switching angles. Newton Raphson Iteration is able to solve and tackle the main defect of SHE PWM which is the requirement of calculations to determine switching angles as in fundamental frequency switching method. The initial value is based on guesses or assumes, thus the result will not be accurate and in addition, increased of DC sources or switching angles will prevent to obtain the most accurate solution [15].

2.3.2.3 Space Vector PWM (SVM)

Space Vector PWM (SVM) is known as an alternative popular control method for multilevel inverters that directly uses the control variable given by the control system and each witching vector is identified as a point in complex space of (α, β). If compared to SPWM, the SVM harmonic elimination and fundamental voltage ratios are obtained in better values. Other

than that, the maximum peak value of the output voltage is greater by 15 % than the SPWM technique. Any three phase multilevel space vector diagram consists of six vectors regardless of the type and the number of levels of the inverters [9,10].

SVM is popular generally because of several features such as good utilization of dc link voltage and low current ripple. These features make the SVM suitable to be used in high voltage and high power applications. SVM technique is quite complicated because of the sector identification and look up table requirement to determine the switching intervals for all vectors but the proper implementations of digital signal processing (DSP) and microprocessor in preparing the algorithms made the hardware to relatively easy to implement [9,10].

2.4 Summary of Review

This chapter discussed about power quality consists of harmonic definition and standards. The topologies of multilevel inverters along with their switching schemes also been explained. From the explanations, shows that both topologies and control schemes of the multilevel inverter determine the efficiency of the inverter in term of equipment used and total harmonic distortion.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter will discuss the methodology of the research consists of the flow of the research process. The brief explanations of Trinary MLI are also described in this chapter. Next, the simulation MATLAB/Simulink block diagrams are presented along with details explanation of the block and finally, hardware design consists of power circuit, control circuit and gate driver shown along with the component used.

3.2 Research Methodology

Upon completion of this research, several steps of process are made according to a sequence. All the steps or procedures in conducting this research are briefly explained in this section with assistance of flowchart, milestone and Gantt chart.

3.2.1 Flowchart

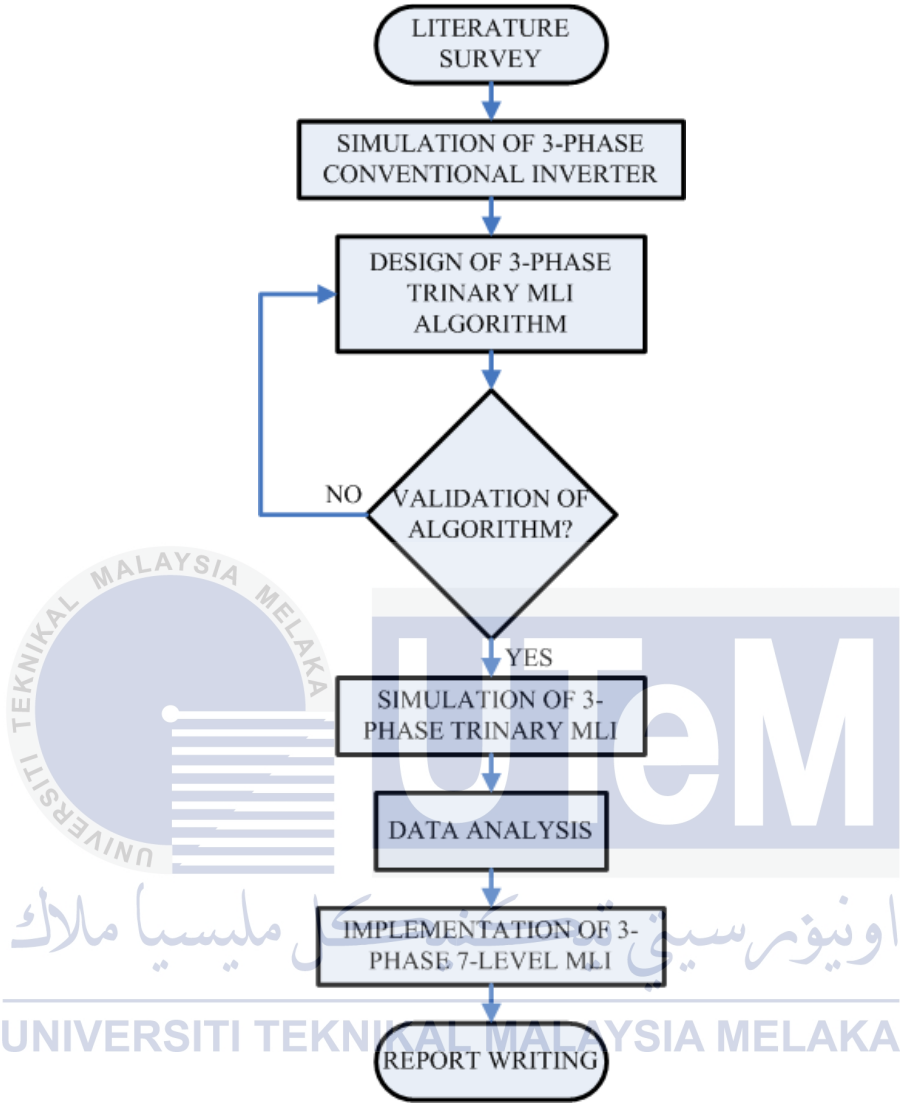


Figure 3.1: Flowchart of Research Methodology

Figure 3.1 shows the flow of activities conducted upon completion of this research based on the flowchart diagram. First, the information and data required to conduct the research are gathered and studied to ensure the research to run smoothly. All the data gathered are presented in Chapter 2. After gathering enough information, the simulation of three phase conventional inverters which are Square and Quasi Inverter is constructed using

MATLAB/Simulink tools. Then the result from the simulation is captured and saved for further analysis.

The next step of the research flow is designing the algorithm for Three Phase Trinary DC Source MLI. In this simulation, odd numbers of Three Phase Trinary DC Source MLI levels from three up to nine will be produce for comparison purposes. Different level of the MLI requires different switching states so that the inverter can produce the desired staircase output voltage waveform. The switching algorithm then is used in the MATLAB/Simulink to test the effectiveness. If the algorithm is applicable, the process will proceed for the simulation of Three Phase Trinary DC Source MLI. The simulation result is gathered and compared with the conventional result taken before.

After the simulation process succeeds, the hardware for Three Phase Seven Level Trinary DC Source MLI will be implemented according to the algorithm designed in the MATLAB/Simulink simulation. Finally, research report is written and compiled. All result, analysis and discussion on the data gathered will be presented in the report.

3.2.2 Milestone

Below is the milestone stone set for this research.

Milestone 1 – Research on MLI

Milestone 2 – Simulation of the three phase conventional and Trinary DC Source MLI

Milestone 3 – Validate the data obtain from simulation

Milestone 4 – Development of Three Phase Seven Level Trinary DC Source MLI

Milestone 5 – Validate the data obtain from hardware

Milestone 6 – Report writing

3.2.3 Gantt Chart

Table 3.1: Gantt Chart of Research Methodology

Milestone	Year	2013				2014				
	Task	9	10	11	12	1	2	3	4	5
1	Research on MLI									
2	Simulation of the three phase conventional and Trinary DC Source MLI									
3	Validate the data obtain from simulation									
4	Development of Three Phase Seven Level Trinary DC Source MLI									
5	Validate the data obtain from hardware									
6	Report writing									

Table 3.1 shows the chart of activities conducted according to the month upon completion of this research. The research starts on September 2013. For the first three months, will be focused more on research of MLI consists of their topologies and control schemes. Two month is provided to conduct the simulation of both conventional and the proposed Trinary DC Source MLI. At the same time, result from the simulation is validated. After the simulation is complete, the hardware is implemented and the time proposed for this process is approximately six months. Next, four months is used to do the analysis on data gathered

during simulations and hardware design. The report writing is conducted along the way of the research process and no fixed time is provided.

3.3 Trinary DC Source Multilevel Inverter

The basic structure of Trinary MLI is same as the H-bridge cascaded multilevel inverter except that, the Trinary MLI occupies different value of input DC sources. Two sets of H-bridge connected power switches with different DC source supplies are required to produce different level of output voltage up to nine levels. Therefore, the Trinary MLI possessed all the H-bridge cascaded multilevel inverter advantages such as reliability and modularity. As an addition, the Trinary MLI have the lowest number of components used compared to other MLI topologies for higher level of output voltage. Table 3.2 shows the comparison of number of component between various types of MLI.

Table 3.2: Number of Components for Single Phase of the Nine Level MLI

Topology	Diode Clamped MLI	Capacitor Clamped MLI	Cascaded H-Bridge MLI	Trinary DC Source MLI
Number of Power Switches	16 units	16 units	16 units	8 units
Number of Clamped Diodes	56 units	0	0	0
Number of Flying Capacitors	0	28 units	0	0

Figure 3.2 shows a circuit configuration for Trinary MLI employing different DC sources feeding the two sets of H-bridge power switches.

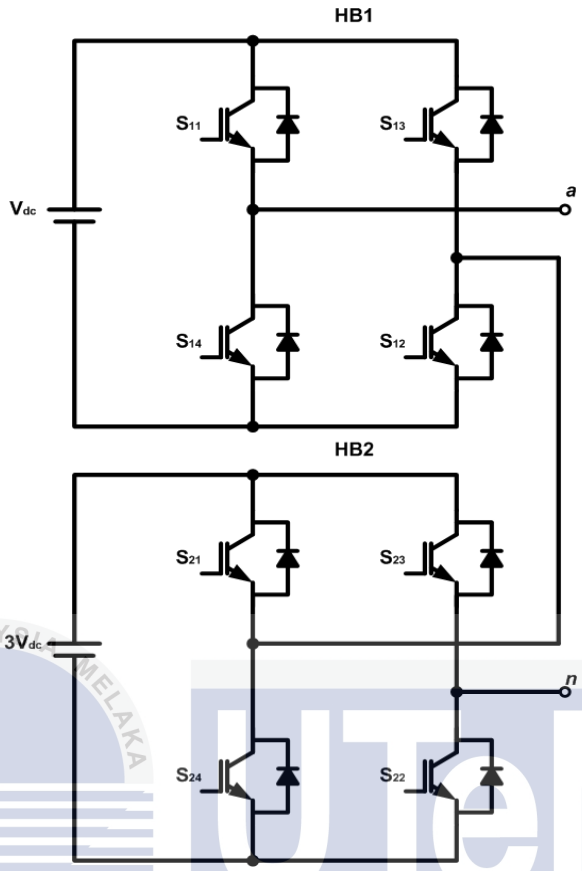


Figure 3.2: Trinary DC Source MLI

The inverter can synthesized up to nine output levels which are $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, $2V_{dc}$, $3V_{dc}$ and $4V_{dc}$ by using the V_{dc} and $3V_{dc}$ supply. The upper inverter (HB1) terminal voltage can generates range of $-V_{dc}$ to V_{dc}, while for the lower inverter (HB2) terminal voltage generates the range of $-3V_{dc}$ to $3V_{dc}$. Here, the final voltage level output of the multilevel inverter becomes the sum of the terminal voltage of HB1 and HB2 of the inverter.

$$V_{out} = V_{HB1} + V_{HB2} \tag{3.1}$$

For example, to produce $+2V_{dc}$, switch S_{12} and S_{13} needs to be closed to able the HB1 to produce $-V_{dc}$ at the terminal voltage. While for the HB2, switch S_{21} and S_{24} needs to be closed to produce $+3V_{dc}$. Therefore, by using the above equation, the output voltage of the multilevel inverter will become $+2V_{dc}$. The rest of the switching sequence of the Three Level, Five Level, Seven Level and Nine Level Trinary DC Source MLI are as following.

Table 3.3: Switching Sequence of Three Level Trinary DC Source MLI

V_{out}	**HB 1**				**HB 2**			
	S_{11}	**S_{12}**	**S_{13}**	**S_{14}**	**S_{21}**	**S_{22}**	**S_{23}**	**S_{24}**
V_{dc}	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1

Table 3.4: Switching Sequence of Five Level Trinary DC Source MLI

V_{out}	**HB 1**				**HB 2**			
	S_{11}	**S_{12}**	**S_{13}**	**S_{14}**	**S_{21}**	**S_{22}**	**S_{23}**	**S_{24}**
$2V_{dc}$	0	0	1	1	1	1	0	0
V_{dc}	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1

Table 3.5: Switching Sequence of Seven Level Trinary DC Source MLI

V_{out}	HB 1				HB 2			
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
$3V_{dc}$	0	1	0	1	1	1	0	0
$2V_{dc}$	0	0	1	1	1	1	0	0
V_{dc}	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1
$-3V_{dc}$	0	1	0	1	0	0	1	1

Table 3.6: Switching Sequence of Nine Level Trinary DC Source MLI

V_{out}	HB 1				HB 2			
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
$4V_{dc}$	1	1	0	0	1	1	0	0
$3V_{dc}$	0	1	0	1	1	1	0	0
$2V_{dc}$	0	0	1	1	1	1	0	0
V_{dc}	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1
$-3V_{dc}$	0	1	0	1	0	0	1	1
$-4V_{dc}$	0	0	1	1	0	0	1	1

3.4 Simulation

The simulation of Three Phase Square Inverter, Three Phase Quasi Inverter and Three Phase Trinary DC Source MLI is conducted using MATLAB/Simulink simulation tools. The inverter structures are construct using several subsystem block consists of logic and electronic components. The block diagram of these three types of inverter is as the following.

3.4.1 Three Phase Conventional Multilevel Inverter

This section shows the MATLAB/Simulink simulation block diagram of Three Phase Square Inverter and Three Phase Quasi Inverter.

3.4.1.1 Three Phase Square Inverter

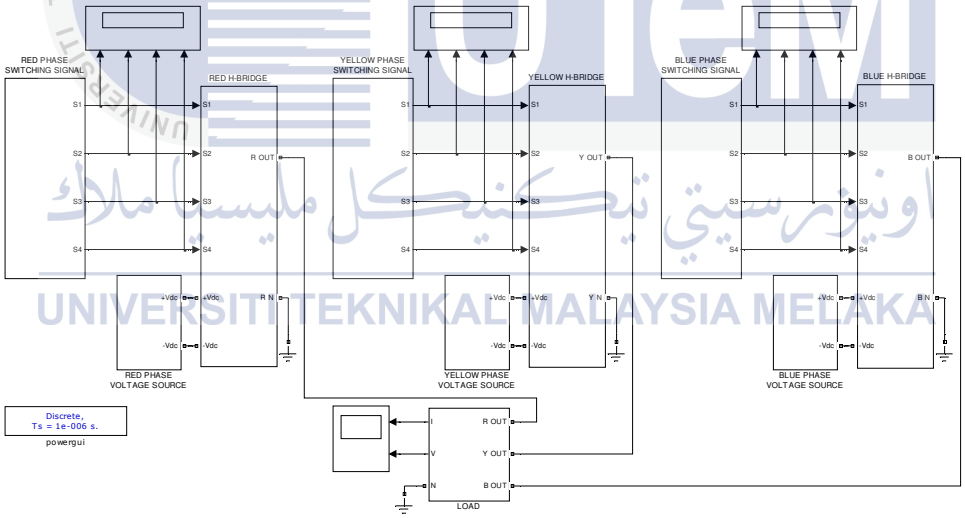


Figure 3.3: Three Phase Square Inverter Simulation Block

Figure 3.3 shows the simulation block diagram for Three Phase Square Inverter. The block diagram consists of switching signal, H-bridge, voltage source and load subsystem for

every phase. Switching signal subsystem is used to generate desired signal to turn on the power switches while four units of IGBTs form a sets of H-bridge occupies the H-bridge subsystem. The H-bridge is fitted by the 100 V DC voltage source from the voltage source subsystem and the load subsystem consists of several combination of 100 Ω resistor, 0.2 H inductor and 100 μF capacitor. Scope is used to measure the output voltage, current and as well as the voltage and current THD. Figure 3.4 shows the simulated switching signal generation of the Three Phase Square Inverter.

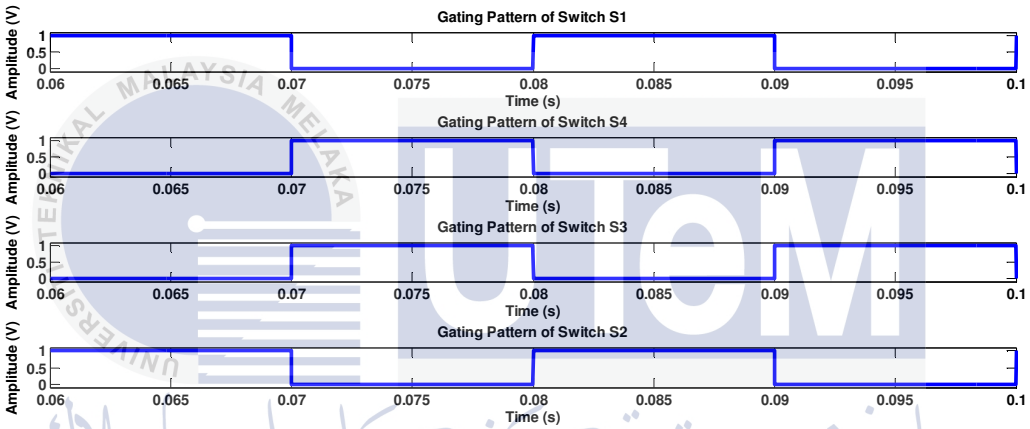


Figure 3.4: Three Phase Square Inverter Switching Signal Generation

3.4.1.2 Three Phase Quasi Inverter

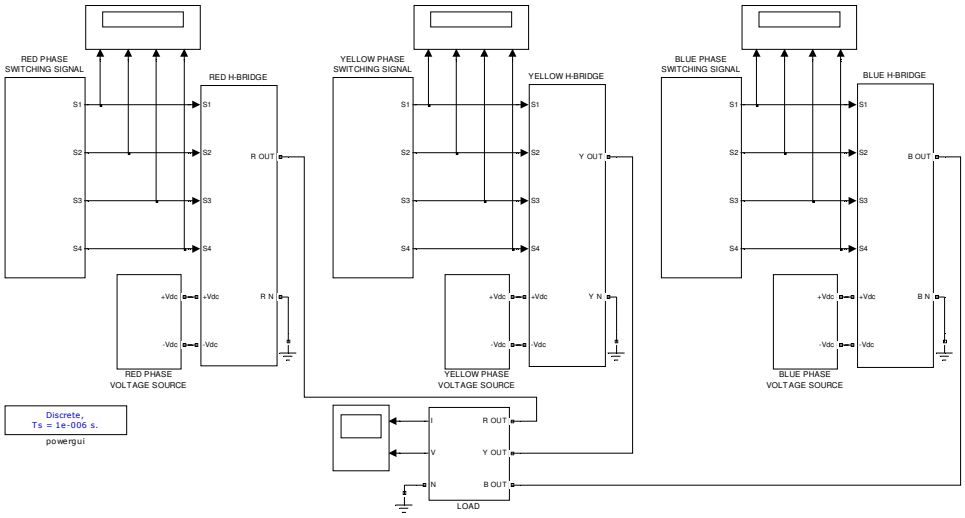


Figure 3.5: Three Phase Quasi Inverter Simulation Block

Figure 3.5 shows the simulation block diagram for Three Phase Quasi Inverter. The block diagram consists of switching signal, H-bridge, voltage source and load subsystem for every phase. Switching signal subsystem is used to generate desired signal to turn on the power switches while four units of IGBTs form a sets of H-bridge occupies the H-bridge subsystem. The H-bridge is fitted by the 100 V DC voltage source from the voltage source subsystem and the load subsystem consists of several combination of 100 Ω resistor, 0.2 H inductor and 100 μF capacitor. Scope is used to measure the output voltage, current and as well as the voltage and current THD. Figure 3.6 shows the simulated switching signal generation of the Three Phase Quasi Inverter.

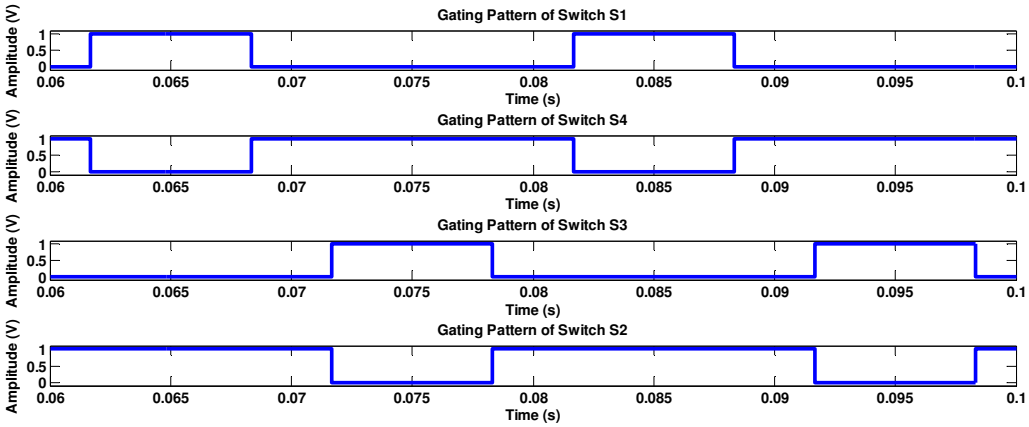


Figure 3.6: Three Phase Quasi Inverter Switching Signal Generation

3.4.2 Three Phase Trinary DC Source Multilevel Inverter

This section shows the MATLAB/Simulink simulation block diagram of Three Phase Trinary DC Source MLI and its switching signal generation of the Three Level, Five Level, Seven Level and Nine Level. Simple modulation technique is used to drive the IGBT power switches.

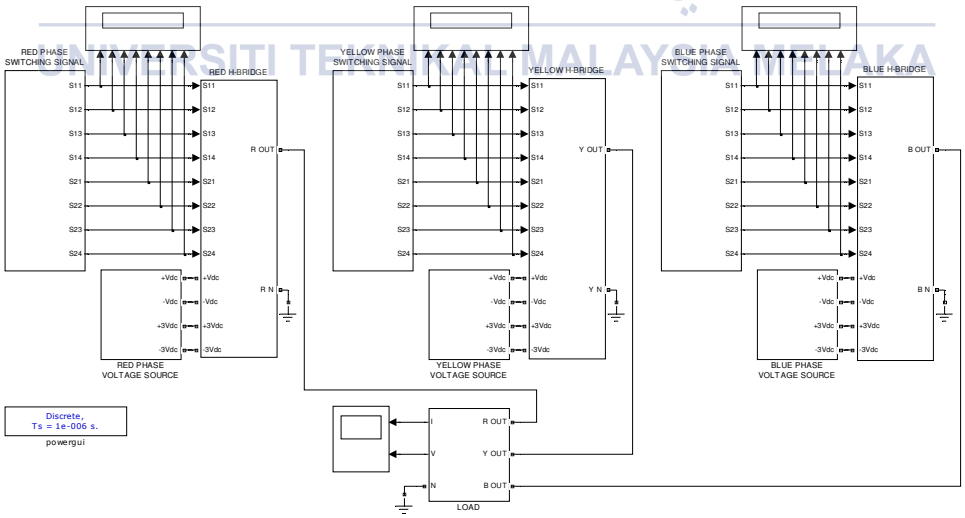
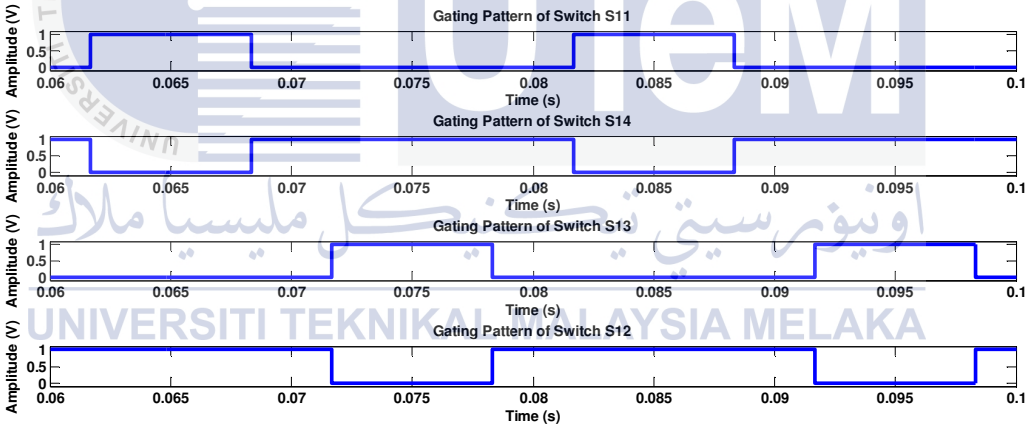
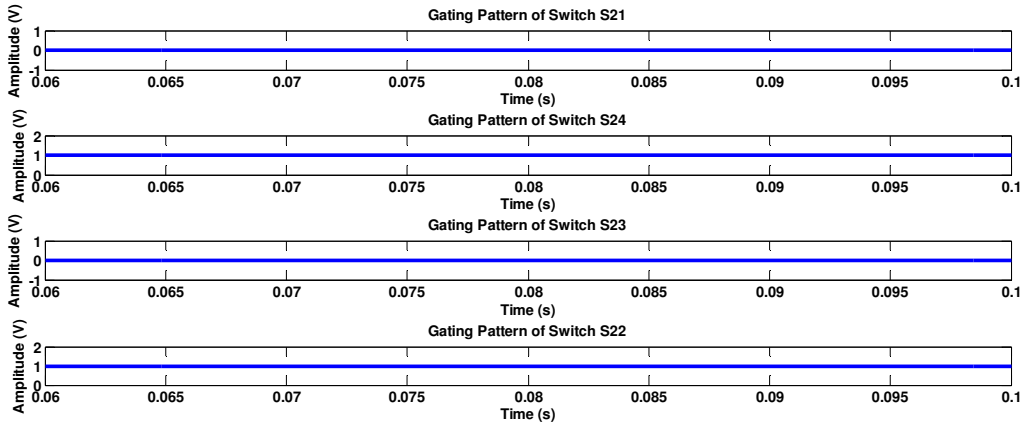


Figure 3.7: Three Phase Trinary DC Source MLI Simulation Block

Figure 3.7 shows the simulation block diagram for Three Phase Trinary DC Source MLI. The block diagram consists of switching signal, H-bridge, voltage source and load subsystem for every phase. Switching signal subsystem is used to generate desired signal to turn on the power switches while eight units of IGBTs form two sets of H-bridge occupies the H-bridge subsystem. The H-bridge is fitted by the 100 V and 300 V DC voltage source from the voltage source subsystem and the load subsystem consists of several combination of 100 Ω resistor, 0.2 H inductor and 100 μF capacitor. Scope is used to measure the output voltage, current and as well as the voltage and current THD. Figure 3.8, Figure 3.9, Figure 3.10 and Figure 3.11 show the simulated switching signal generation of the Three Phase Trinary DC Source MLI for Three Level, Five Level, Seven Level and Nine Level.

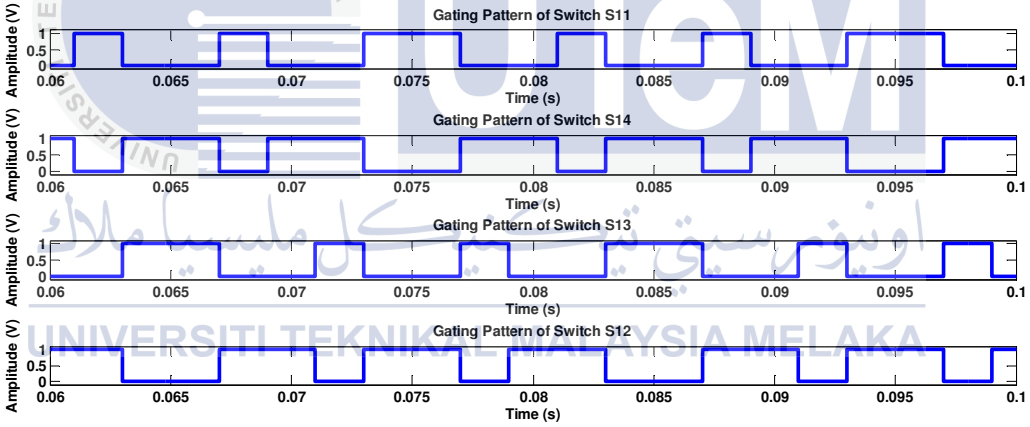


(a)

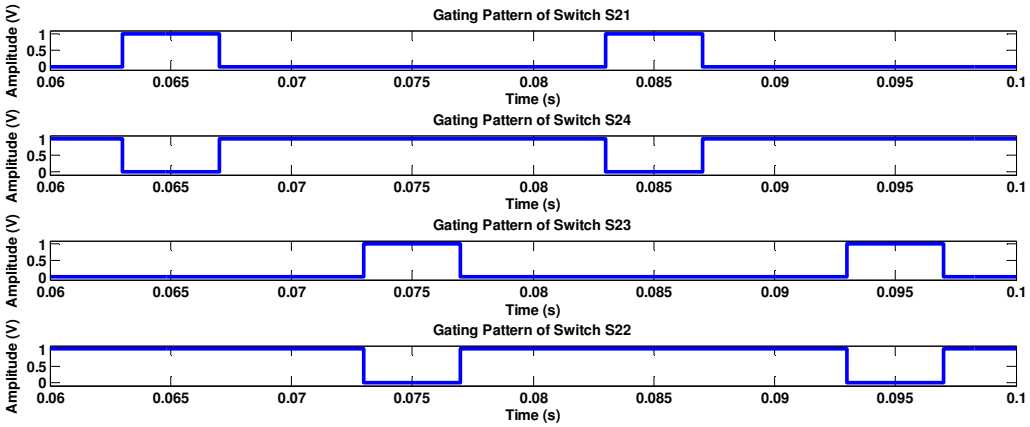


(b)

Figure 3.8: Three Phase Three Level Trinary DC Source MLI Switching Signal Generation for (a) Switch S11, S12, S13 and S14 (b) Switch S21, S22, S23 and S24

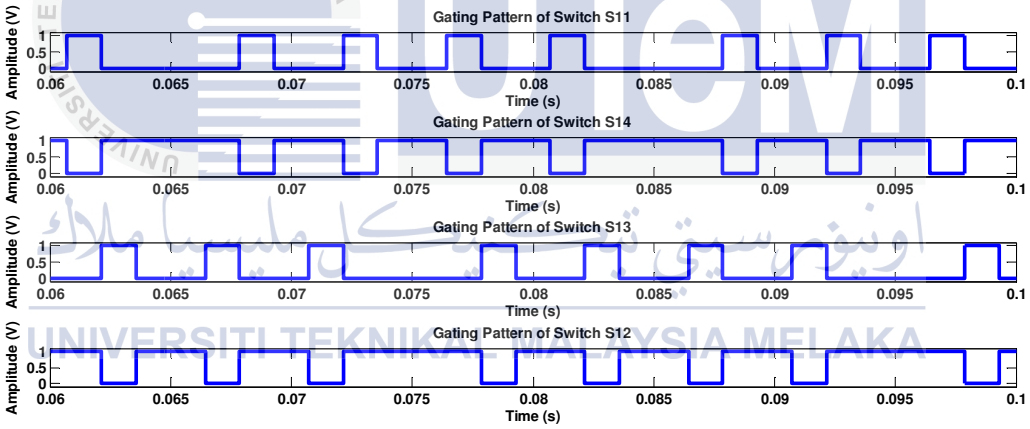


(a)

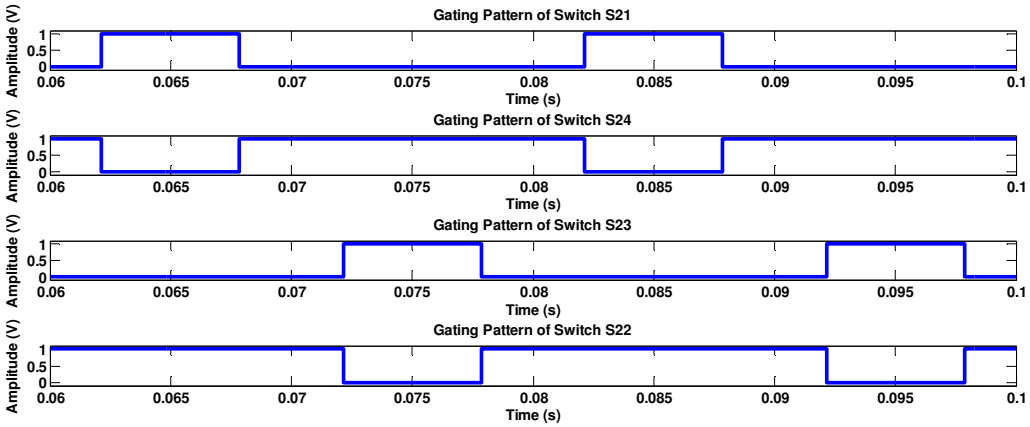


(b)

Figure 3.9: Three Phase Five Level Trinary DC Source MLI Switching Signal Generation for (a) Switch S11, S12, S13 and S14 (b) Switch S21, S22, S23 and S24

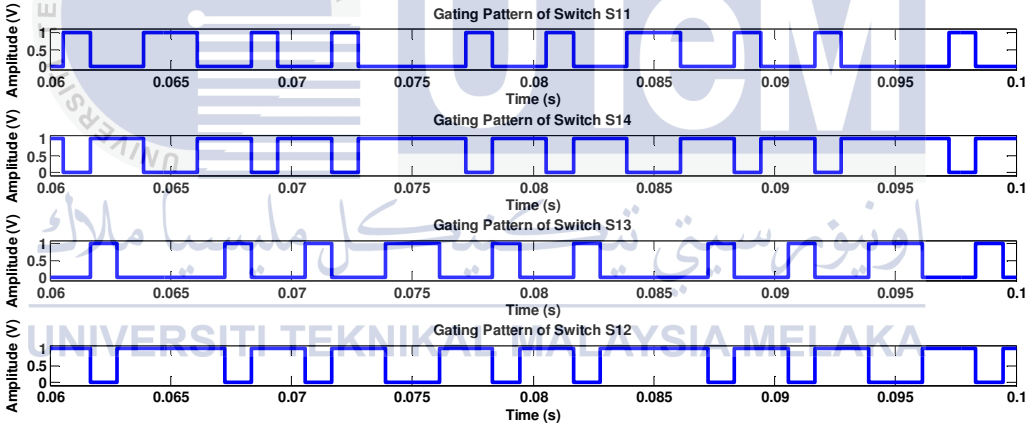


(a)

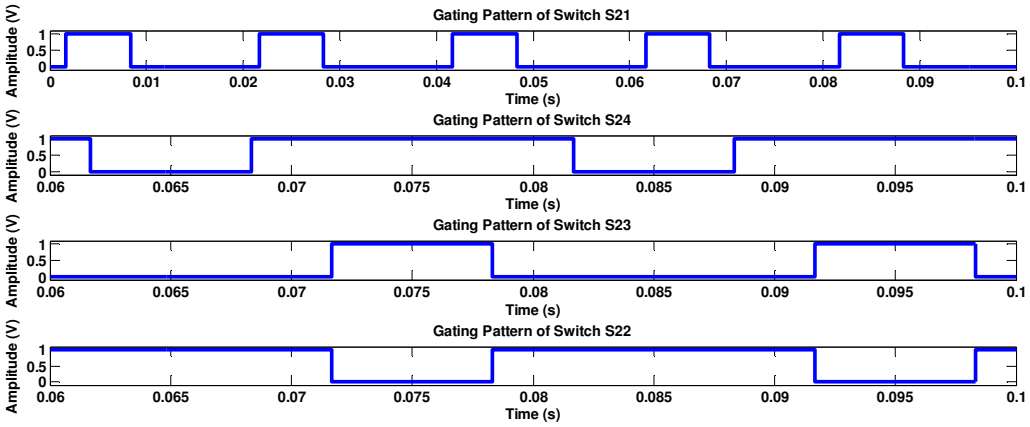


(b)

Figure 3.10: Three Phase Seven Level Trinary DC Source MLI Switching Signal Generation for (a) Switch S11, S12, S13 and S14 (b) Switch S21, S22, S23 and S24



(a)



(b)

Figure 3.11: Three Phase Nine Level Trinary DC Source MLI Switching Signal Generation for (a) Switch S11, S12, S13 and S14 (b) Switch S21, S22, S23 and S24

3.5 Hardware

The proposed circuit of Three Phase Seven Level Trinary DC Source MLI is presented in this section. The circuits structures are constructed using several circuit namely H-Bridge inverter, gate drive, DC/DC converter and microcontroller.

3.5.1 H-Bridge Inverter Circuit

This H-bridge inverter circuit shown in Figure 3.12 consists of four sets of IGBT type IHW30N90T. The switching signals for IGBT are coming from gate drive circuit.

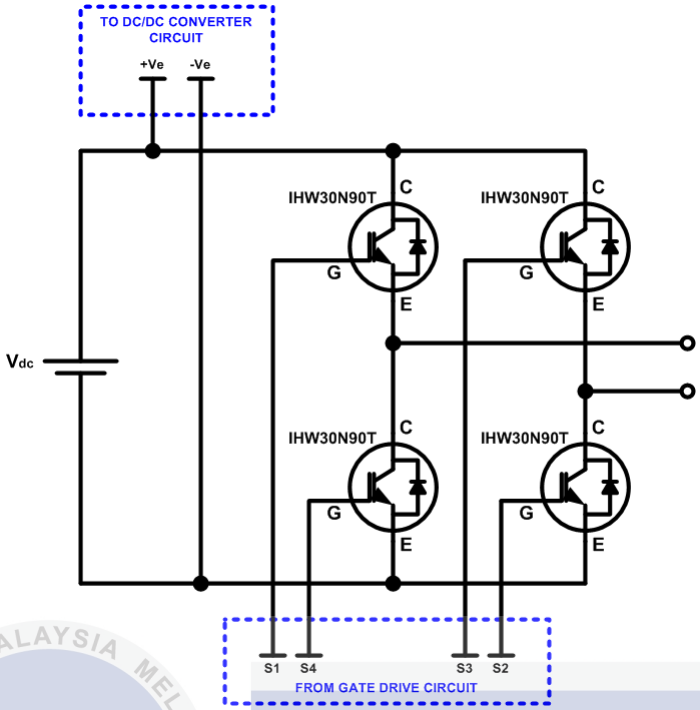


Figure 3.12: H-Bridge Inverter Circuit for Phase A

3.5.2 Gate Drive Circuit

Microcontroller generates signal in logic form. This signal is not capable to switch on the IGBT power switch because of the level of output voltage from microcontroller only generates 5 *V* DC source. In order to switch ON and OFF IGBT, the gate drive is needed to boost up the 5 *V* PWM signal to 15 *V* PWM signal. Figure 3.13 shows the proposed gate driver circuit consists of Arduino Mega 2560 microcontroller, HCPL-3120-000E gate drive, 100 Ω current limiting resistor and zener diode to make sure the voltage fed to the gate drive limited at 15 *V* only.

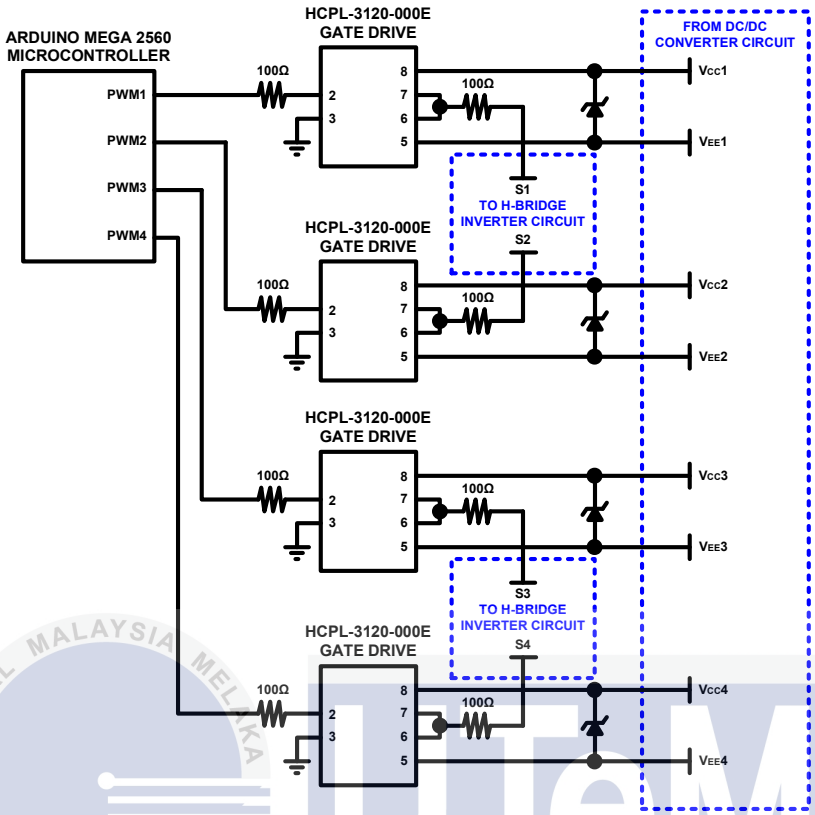


Figure 3.13: Gate Drive Circuit for Phase A

3.5.3 DC/DC Converter Circuit

DC/DC converter functioned to step-up or step-down the DC voltage. In this project, the DC/DC converter type IQ0515SA is used to generate 15 *V* DC output voltages. This supply is connected to gate drive circuit in order to enable the gate drive to transform the low voltage 5 *V* logic signal to 15 *V* DC voltage to drive the IGBT power switches. Figure 3.14 shows the proposed DC/DC converter circuit.

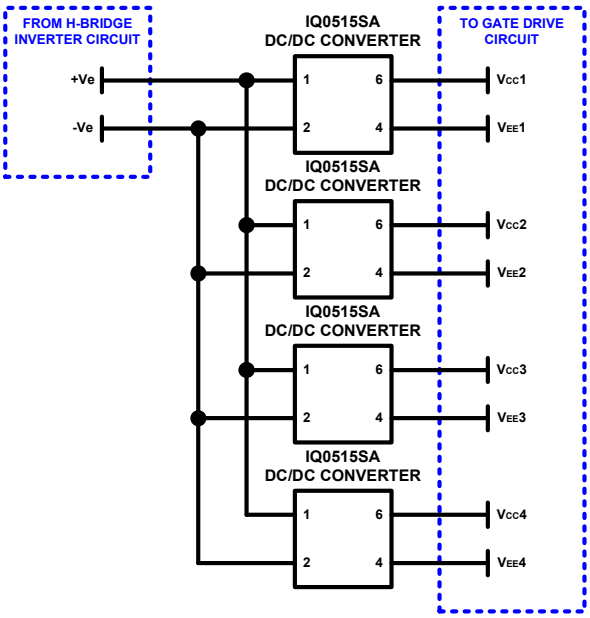


Figure 3.14: DC/DC Converter Circuit for Phase A

3.5.4 Arduino Mega 2560 Microcontroller

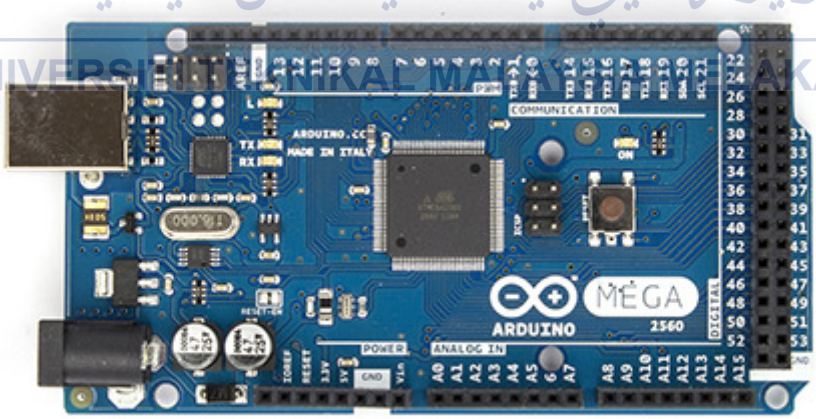


Figure 3.15: Arduino Mega 2560

Arduino Mega 2560 Microcontroller which shown in Figure 3.15 is used to generate the desired switching signal that connected to the gate drive circuit by giving the instruction on the microcontroller using Arduino programming language. Arduino Mega 2560 is selected because it has the sufficient digital output which used to send the signal to the MLI. For Three Phase Seven Level Trinary DC Source MLI, overall signal need to be sent is twenty four. The digital output from Arduino Mega 2560 is only 5 *V*. This level of voltage is boosted to 15 *V* by using DC/DC converter. Table 3.7 shows the parameters of Arduino Mega 2560.

Table 3.7: Arduino Mega 2560 Parameters

Parameters	
Microcontroller	ATmega2560
Operating Voltage	5 *V*
Input Voltage (recommend)	7 - 12 *V*
Input Voltage (limits)	6 - 20 *V*
Digital I/O Pins	54 (of which 15 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	40 *mA*
DC Current for 3.3 *V* Pin	50 *mA*
Flash Memory	256 *kB* of which 8 *kB* used by bootloader
SRAM	8 *kB*
EEPROM	4 *kB*
Clock Speed	16 *MHz*

3.5.5 PCB Design

In order to make the circuit simple easy to manage and compact, the specially designed Printed Circuit Board (PCB) is used. First the diagram of the designed circuit is drawn in the

using OrCad Capture CIS software. After that, the circuit is transferred to OrCad Layout Plus to produce the PCB layout. The PCB layout then is printed on the tracing paper. After that, the process of producing the designed PCB begin from etching process, hole drilling process and component insertion process. All the procedures are stated in APPENDIX D.

3.5.6 Experimental Setup

The previously designed circuit is combined in to such way so that it can be functioned as Three Phase Seven Level DC Source MLI.

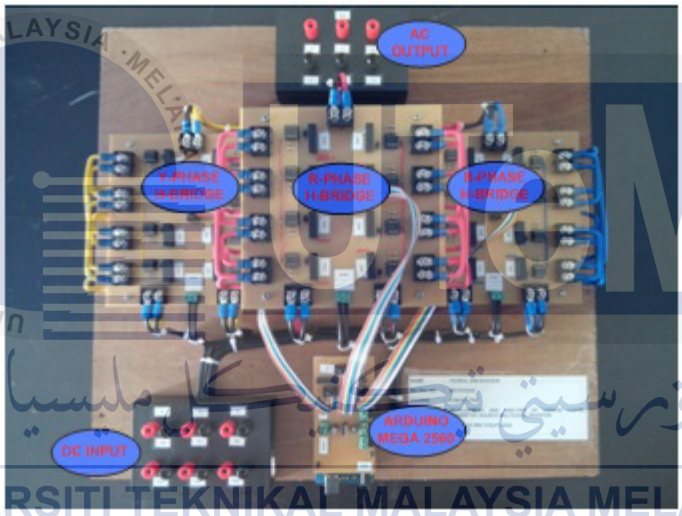


Figure 3.16: Hardware Configuration

After all the three H-Bridge circuits had been combined, it will function as a Three Phase Seven Level Trinary DC Source MLI. The complete configuration of the hardware implementation is shown as in Figure 3.16.

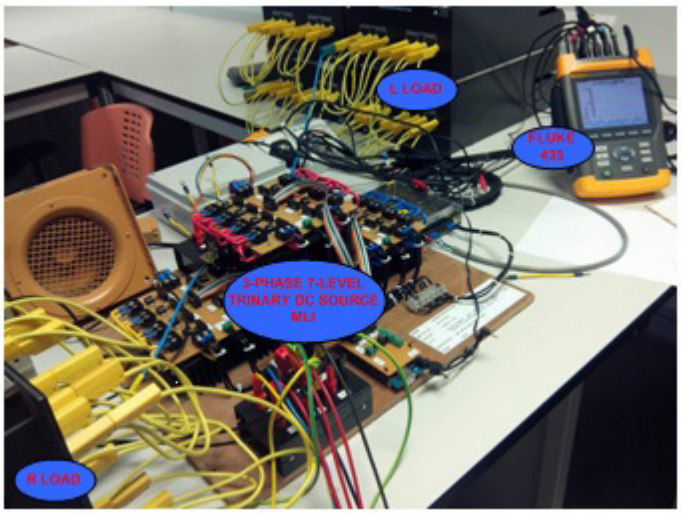


Figure 3.17: Experimental Setup

Figure 3.17 shows the experimental setup to test the performance of the Three Phase Seven Level Trinary DC Source MLI. Separate VDC and 3VDC power supply is used as the MLI input. Resistance and inductance is used as load and Fluke 435 Power Quality Analyzer is used to record all the data such as voltage, current and THD reading to be compared to the simulation result. Table 3.8 shows the parameters used in this experimental setup.

Table 3.8: Experimental Setup Parameters

Parameters	
Microcontroller Input Voltage	9 *V*
DC/DC Converter Input Voltage	5 *V*
DC/DC Converter Output Voltage	12 *V*
VDC Inverter Input Voltage	10 *V*
3VDC Inverter Input Voltage	30 *V*
Data Recorder	Fluke 435 Power Quality Analyzer

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

This chapter presents all the result gathered from the simulation of Three Phase Square Inverter, Three Phase Quasi Inverter and the Three Level, Five Level, Seven Level and Nine Level Trinary DC Source MLI.

4.2 Simulation Result

This section displays the output waveform and harmonic spectrum resulting from the MATLAB/Simulink simulations for different types of inverter attached to the various combination of load.

4.2.1 Three Phase Square Inverter

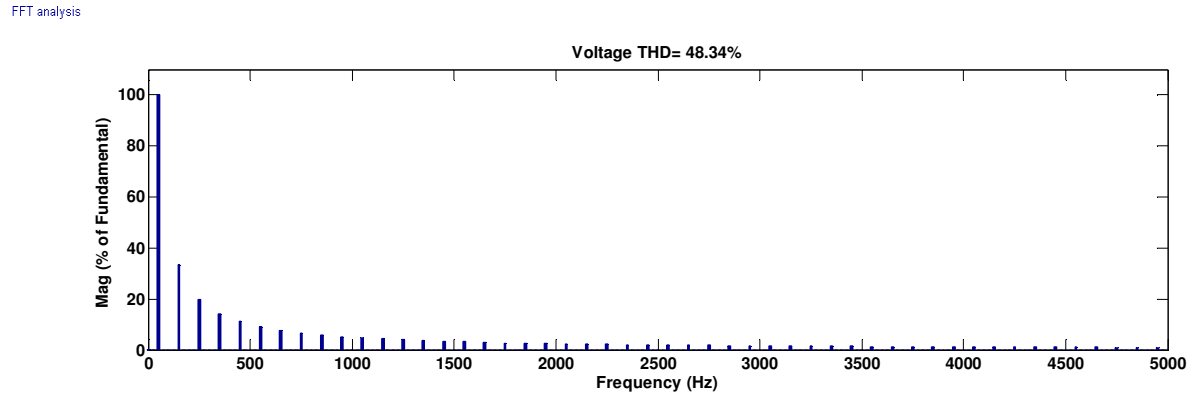


Figure 4.1: Three Phase Square Inverter Voltage Harmonic Spectrum

Figure 4.1 shows the voltage harmonic spectrum of the Three Phase Square Inverter. The voltage total harmonic distortion is 48.34 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.1.1 Three Phase Square Inverter with R Load

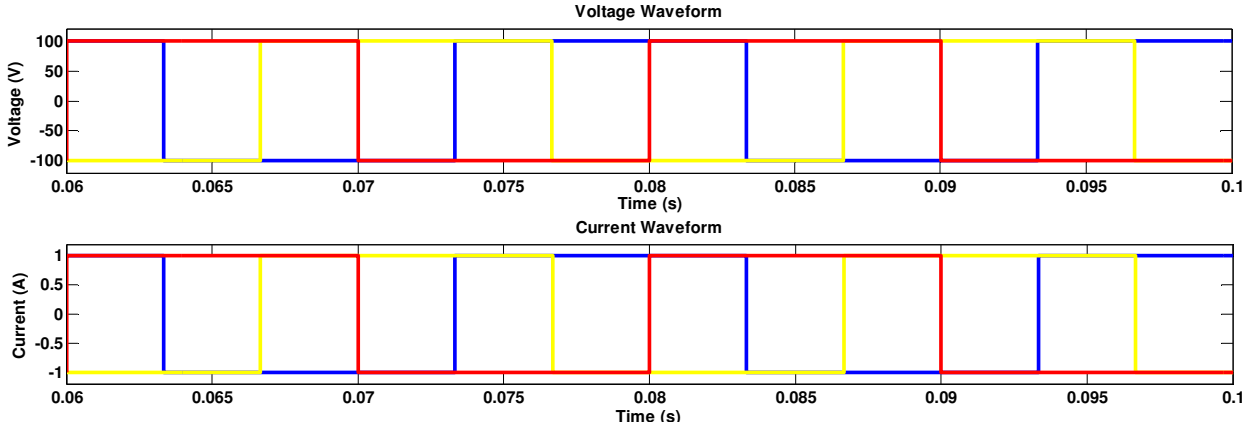


Figure 4.2: Three Phase Square Inverter with R Load Output

Figure 4.2 shows the output voltage and current of Three Phase Square Inverter connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

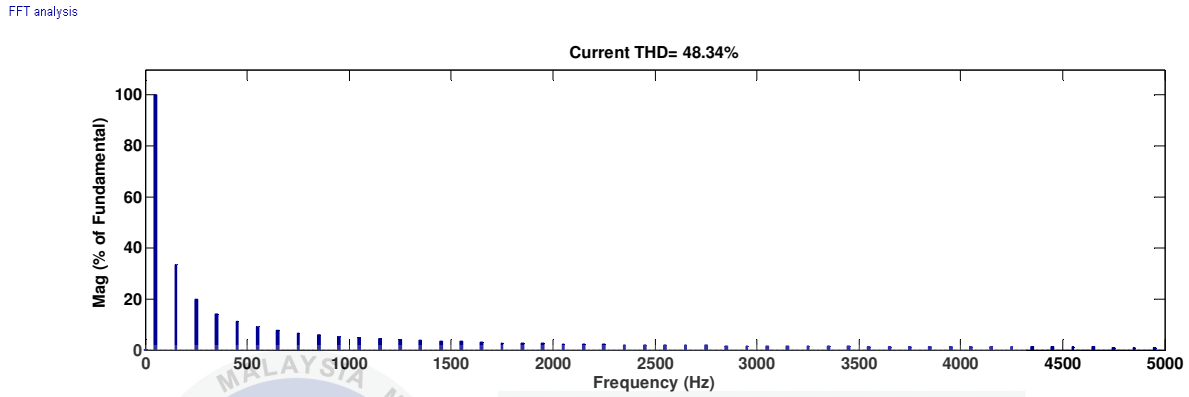


Figure 4.3: Three Phase Square Inverter with R Load Current Harmonic Spectrum

Figure 4.42 shows the current harmonic spectrum of Three Phase Square Inverter connected to R load. The value of current total harmonic distortion is 48.34 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.1.2 Three Phase Square Inverter with RL Load

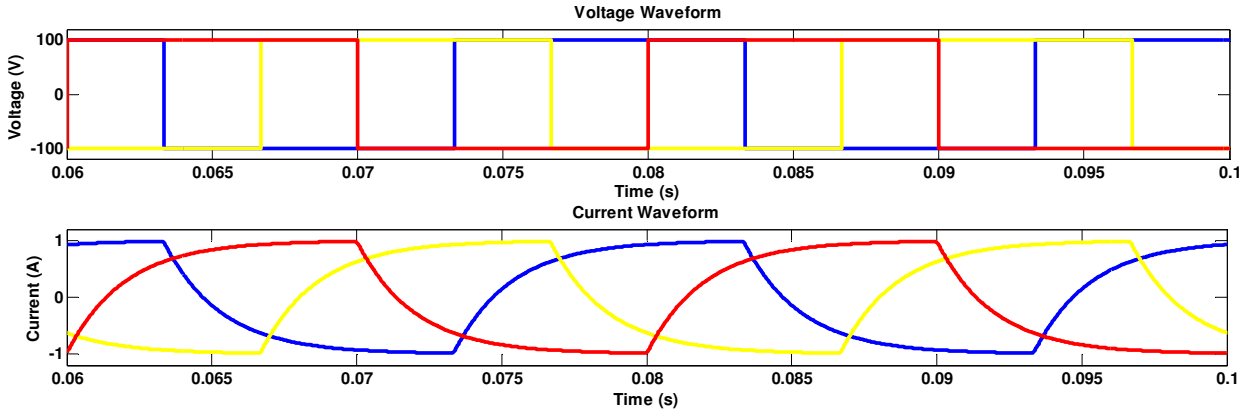


Figure 4.4: Three Phase Square Inverter with RL Load Output

Figure 4.4 shows the output voltage and current of Three Phase Square Inverter connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

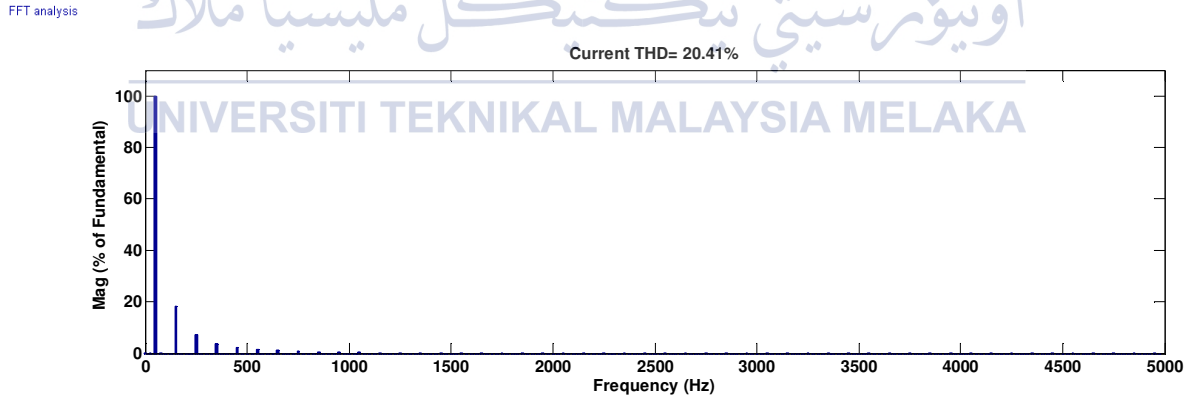


Figure 4.5: Three Phase Square Inverter with RL Load Current Harmonic Spectrum

Figure 4.5 shows the current harmonic spectrum of Three Phase Square Inverter connected to RL load. The value of current total harmonic distortion is 20.41 %.

4.2.1.3 Three Phase Square Inverter with RC Load

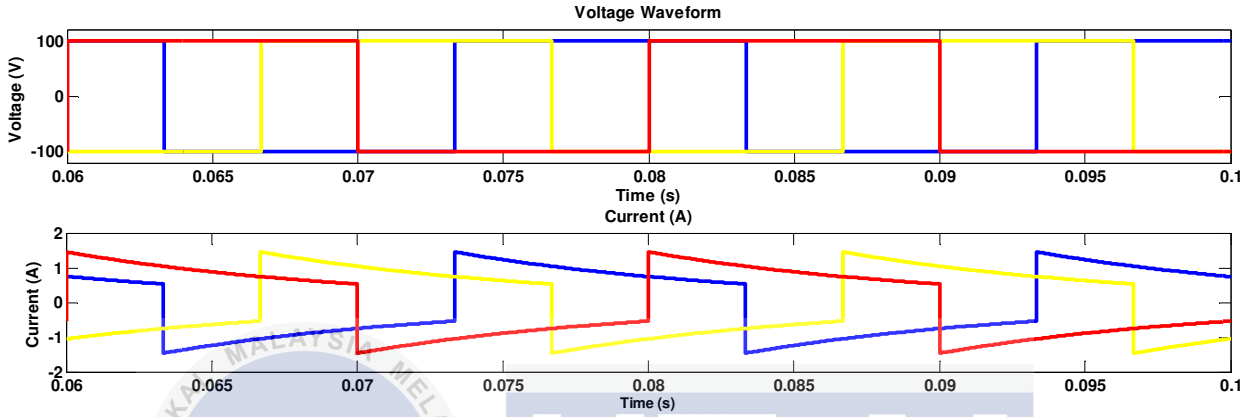


Figure 4.6: Three Phase Square Inverter with RC Load Output

Figure 4.6 shows the output voltage and current of Three Phase Square Inverter connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

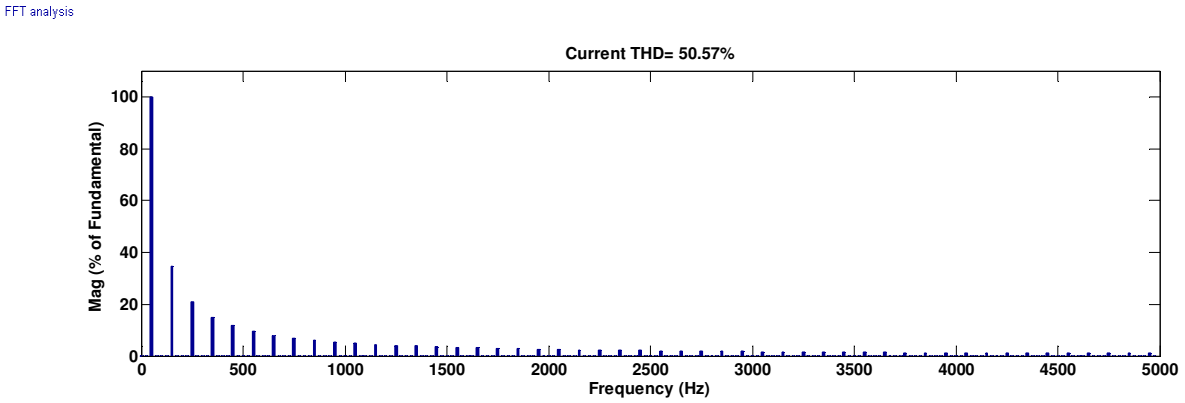


Figure 4.7: Three Phase Square Inverter with RC Load Current Harmonic Spectrum

Figure 4.7 shows the current harmonic spectrum of Three Phase Square Inverter connected to RC load. The value of current total harmonic distortion is 50.57 %.

4.2.2 Three Phase Quasi Inverter

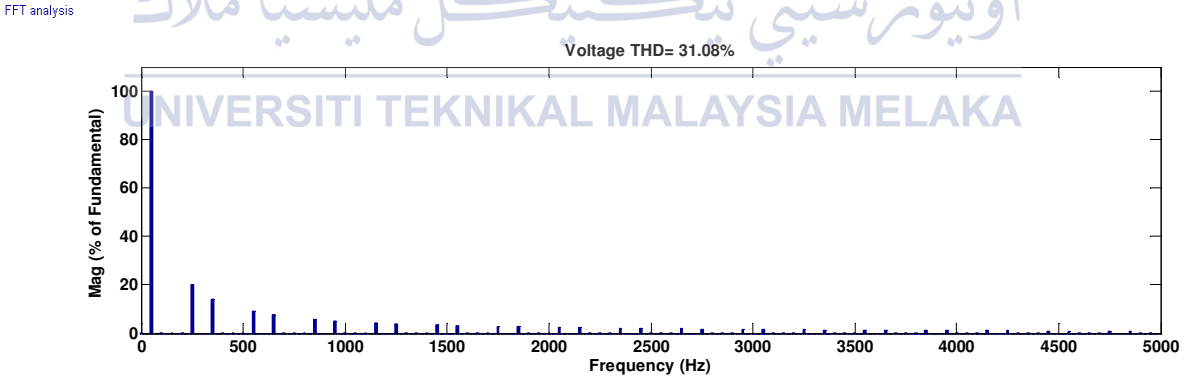


Figure 4.8: Three Phase Quasi Inverter Voltage Harmonic Spectrum

Figure 4.8 shows the voltage harmonic spectrum of the Three Phase Quasi Inverter. The voltage total harmonic distortion is 31.08 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.2.1 Three Phase Quasi Inverter with R Load

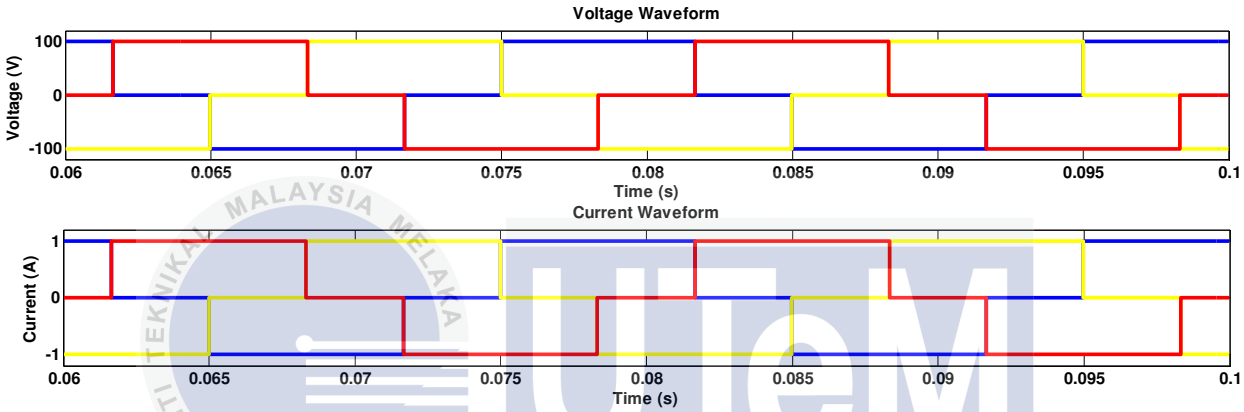


Figure 4.9: Three Phase Quasi Inverter with R Load Output

Figure 4.9 shows the output voltage and current of Three Phase Quasi Inverter connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

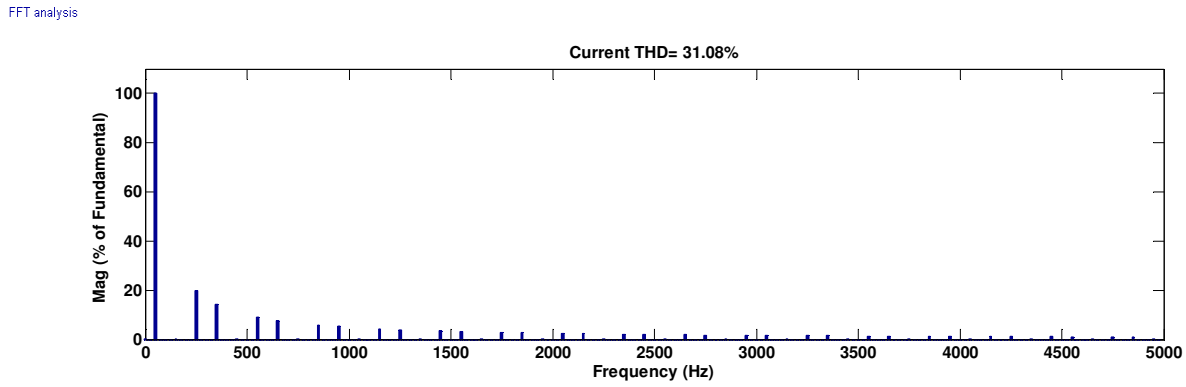


Figure 4.10: Three Phase Quasi Inverter with R Load Current Harmonic Spectrum

Figure 4.10 shows the current harmonic spectrum of Three Phase Square Inverter connected to R load. The value of current total harmonic distortion is 31.08 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.2.2 Three Phase Quasi Inverter with RL Load

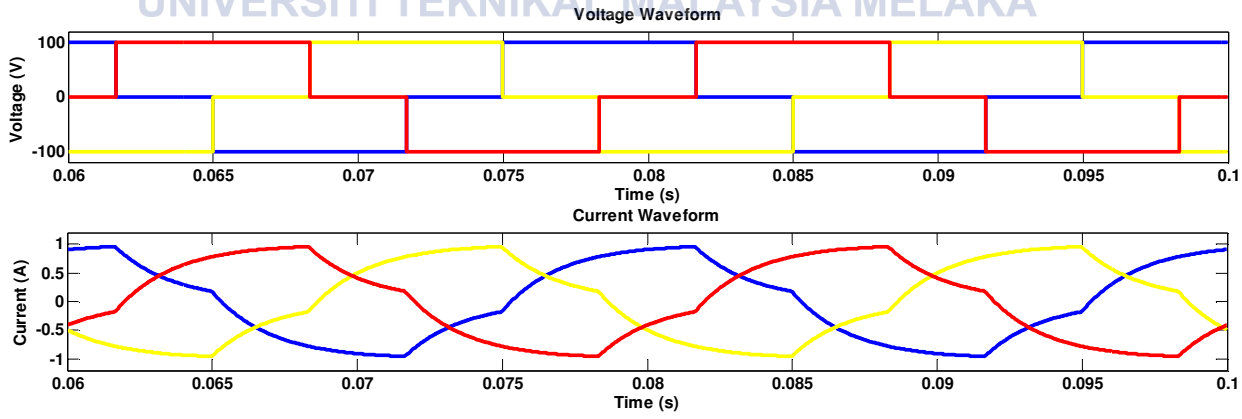


Figure 4.11: Three Phase Quasi Inverter with RL Load Output

Figure 4.11 shows the output voltage and current of Three Phase Quasi Inverter connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

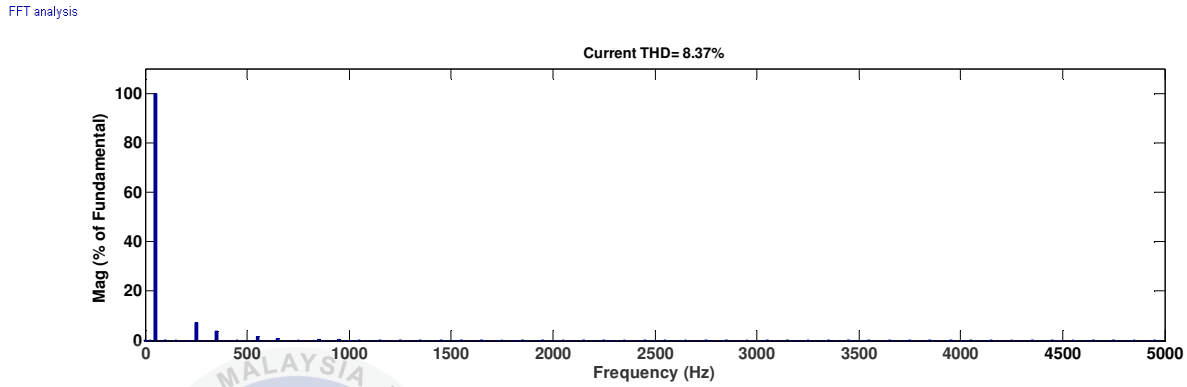


Figure 4.12: Three Phase Quasi Inverter with RL Load Current Harmonic Spectrum

Figure 4.12 shows the current harmonic spectrum of Three Phase Quasi Inverter connected to RL load. The value of current total harmonic distortion is 8.37 %.

4.2.2.3 Three Phase Quasi Inverter with RC Load

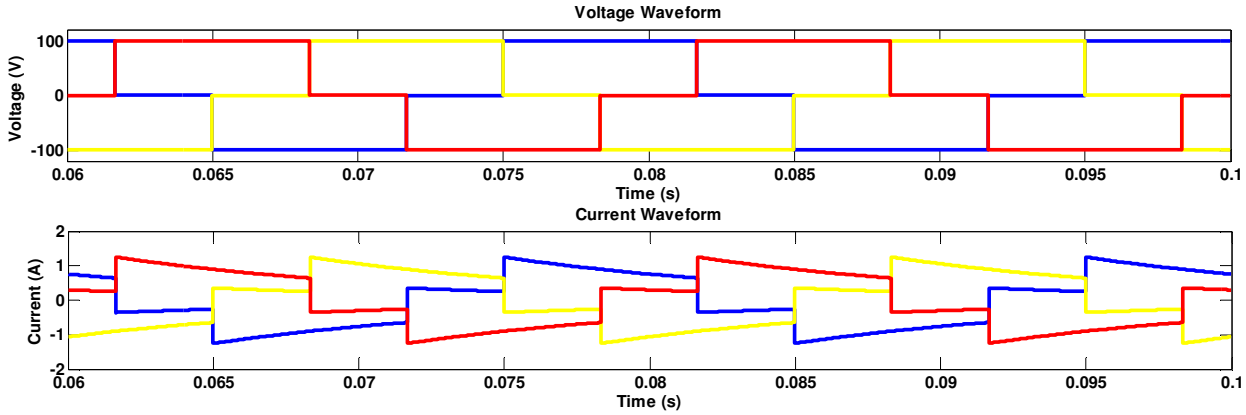


Figure 4.13: Three Phase Quasi Inverter with RC Load Output

Figure 4.13 shows the output voltage and current of Three Phase Quasi Inverter connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

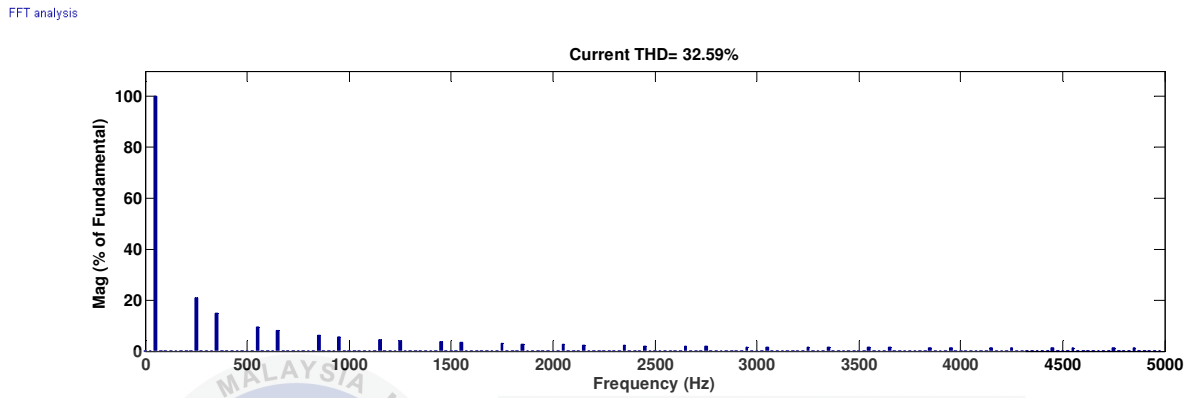


Figure 4.14: Three Phase Quasi Inverter with RC Load Current Harmonic Spectrum

Figure 4.14 shows the current harmonic spectrum of Three Phase Quasi Inverter connected to RC load. The value of current total harmonic distortion is 32.59 %.

4.2.3 Three Phase Three Level Trinary DC Source MLI

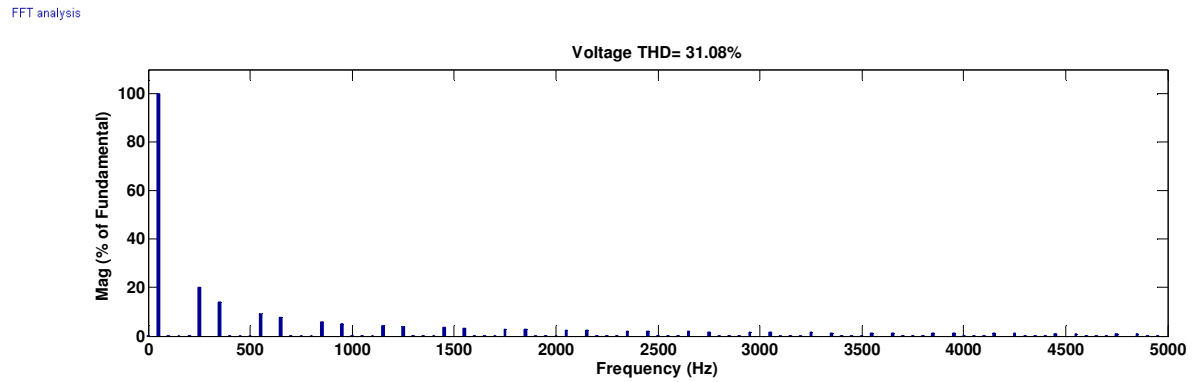


Figure 4.15: Three Phase Three Level Trinary DC Source MLI Voltage Harmonic Spectrum

Figure 4.15 shows the voltage harmonic spectrum of the Three Phase Three Level Trinary DC Source MLI. The voltage total harmonic distortion is 31.08 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.3.1 Three Phase Three Level Trinary DC Source MLI with R Load

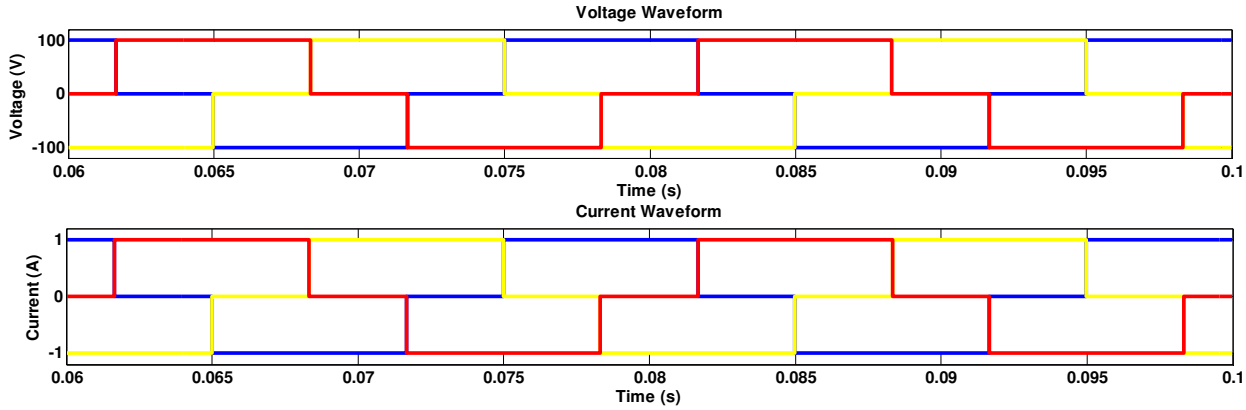


Figure 4.16: Three Phase Three Level Trinary DC Source MLI with R Load Output

Figure 4.16 shows the output voltage and current of Three Phase Three Level Trinary DC Source MLI connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

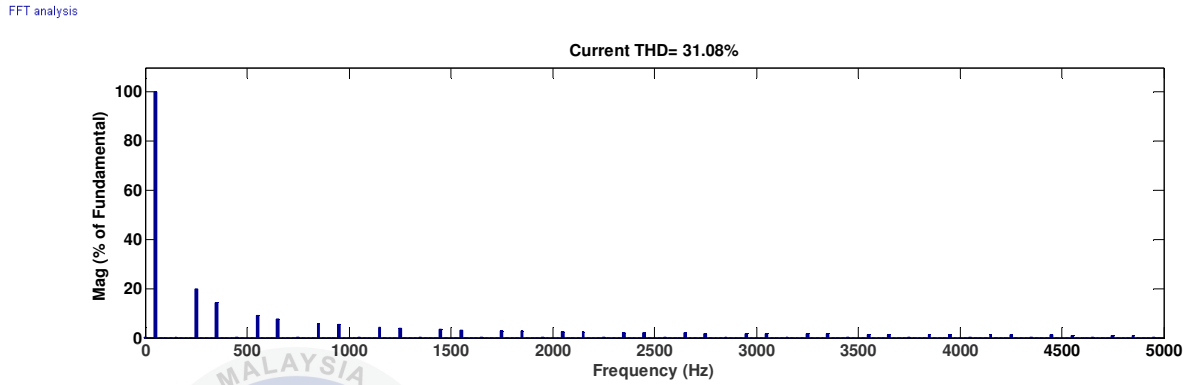


Figure 4.17: Three Phase Three Level Trinary DC Source MLI with R Load Current Harmonic Spectrum

Figure 4.17 shows the current harmonic spectrum of Three Phase Three Level Trinary DC Source MLI connected to R load. The value of current total harmonic distortion is 31.08 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.3.2 Three Phase Three Level Trinary DC Source MLI with RL Load

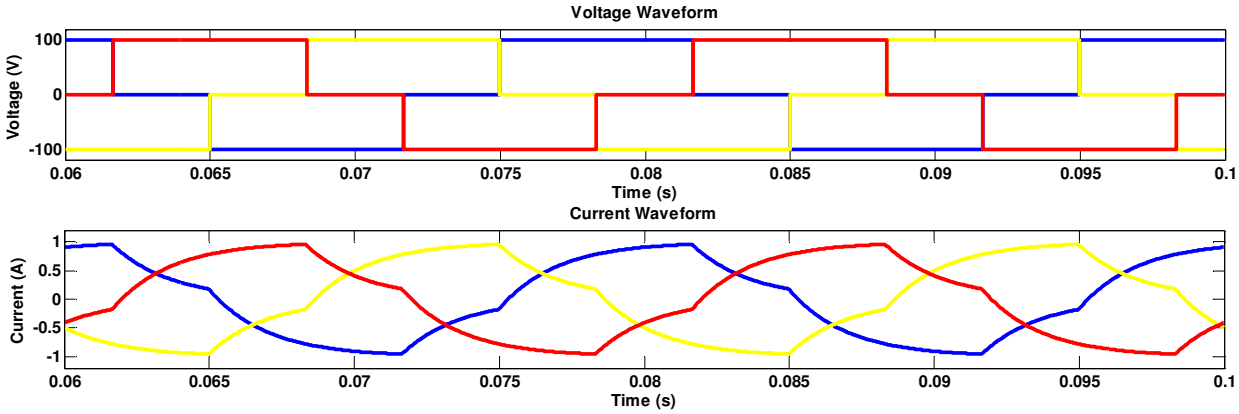


Figure 4.18: Three Phase Three Level Trinary DC Source MLI with RL Load Output

Figure 4.18 shows the output voltage and current of Three Phase Three Level Trinary DC Source MLI connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

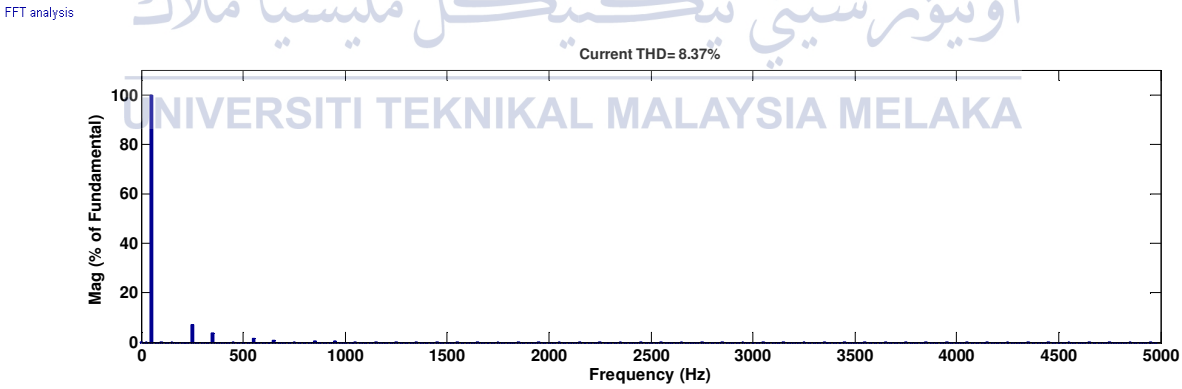


Figure 4.19: Three Phase Three Level Trinary DC Source MLI with RL Load Current Harmonic Spectrum

Figure 4.19 shows the current harmonic spectrum of Three Phase Three Level Trinary DC Source MLI connected to RL load. The value of current total harmonic distortion is 8.37 %.

4.2.3.3 Three Phase Three Level Trinary DC Source MLI with RC Load

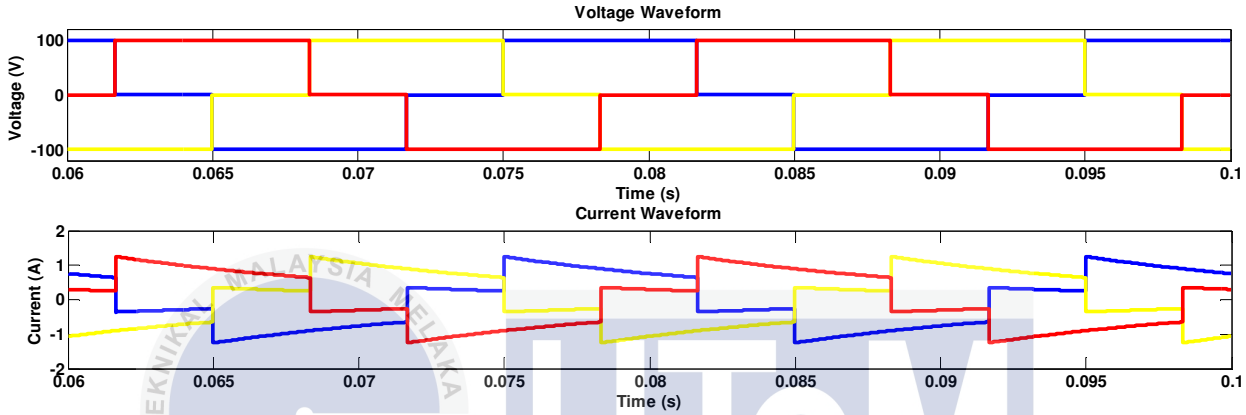


Figure 4.20: Three Phase Three Level Trinary DC Source MLI with RC Load Output

Figure 4.20 shows the output voltage and current of Three Phase Three Level Trinary DC Source MLI connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

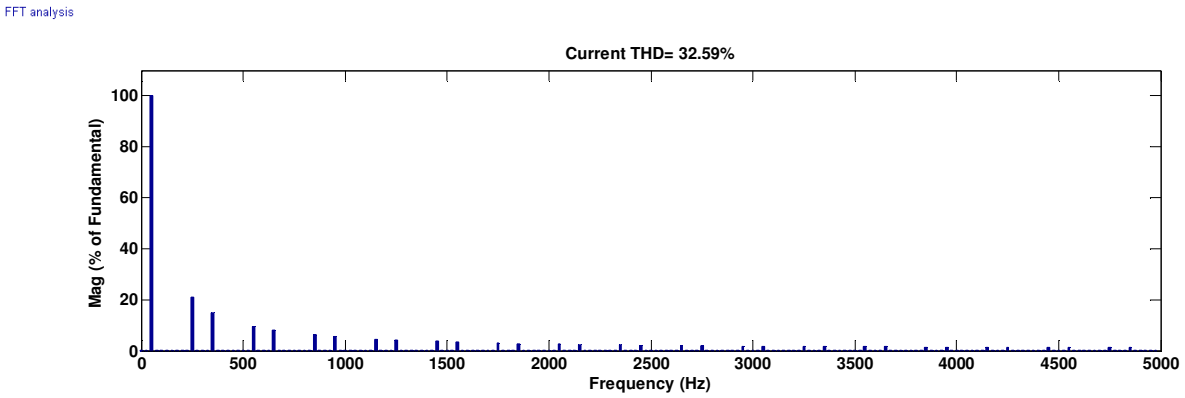


Figure 4.21: Three Phase Three Level Trinary DC Source MLI with RC Load Current Harmonic Spectrum

Figure 4.21 shows the current harmonic spectrum of Three Phase Three Level Trinary DC Source MLI connected to RC load. The value of current total harmonic distortion is 32.59 %.

4.2.4 Three Phase Five Level Trinary DC Source MLI

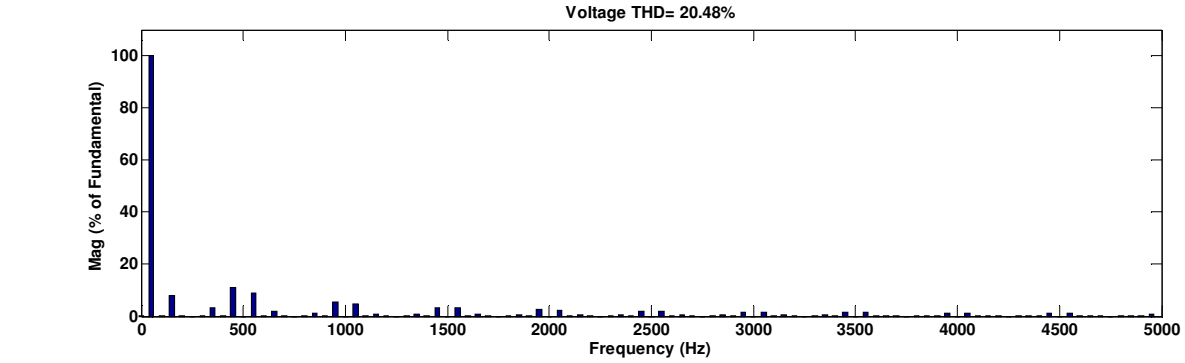


Figure 4.22: Three Phase Five Level Trinary DC Source MLI Voltage Harmonic Spectrum

Figure 4.22 shows the voltage harmonic spectrum of the Three Phase Five Level Trinary DC Source MLI. The voltage total harmonic distortion is 20.48 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.4.1 Three Phase Five Level Trinary DC Source MLI with R Load

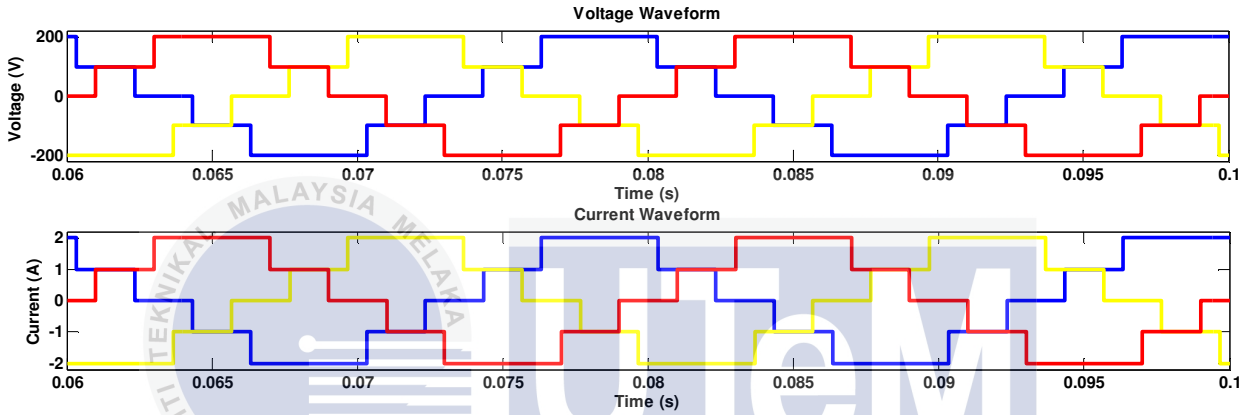


Figure 4.23: Three Phase Five Level Trinary DC Source MLI with R Load Output

Figure 4.23 shows the output voltage and current of Three Phase Five Level Trinary DC Source MLI connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

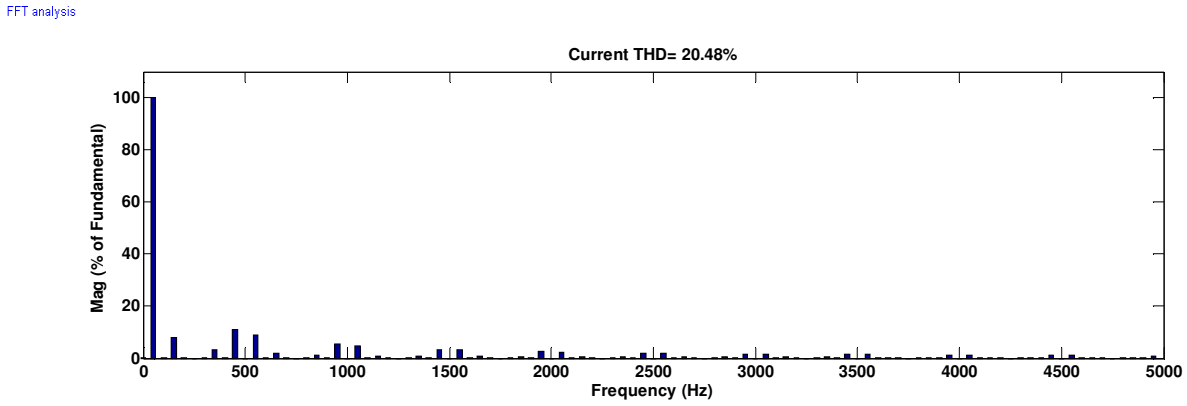


Figure 4.24: Three Phase Five Level Trinary DC Source MLI with R Load Current Harmonic Spectrum

Figure 4.24 shows the current harmonic spectrum of Three Phase Five Level Trinary DC Source MLI connected to R load. The value of current total harmonic distortion is 20.48 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.4.2 Three Phase Five Level Trinary DC Source MLI with RL Load

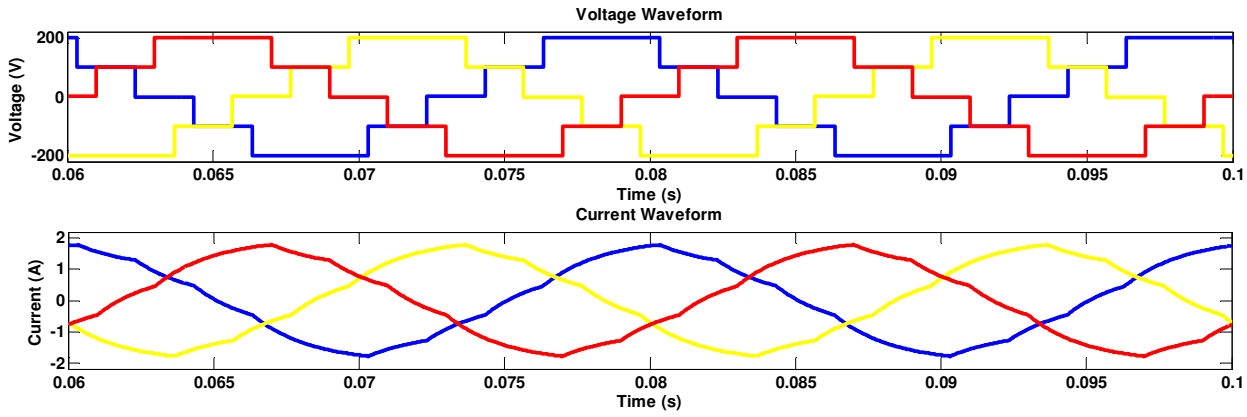


Figure 4.25: Three Phase Five Level Trinary DC Source MLI with RL Load Output

Figure 4.25 shows the output voltage and current of Three Phase Five Level Trinary DC Source MLI connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

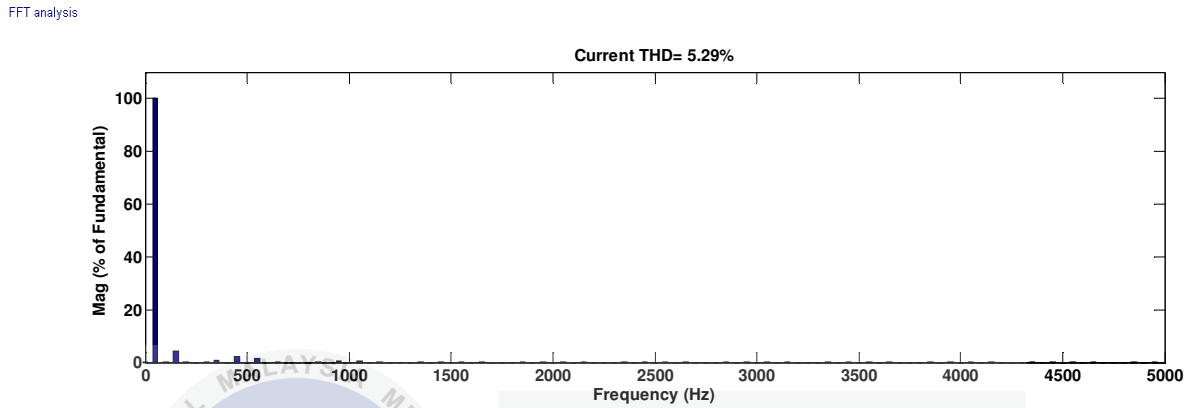


Figure 4.26: Three Phase Five Level Trinary DC Source MLI with RL Load Current Harmonic Spectrum

Figure 4.26 shows the current harmonic spectrum of Three Phase Five Level Trinary DC Source MLI connected to RL load. The value of current total harmonic distortion is 5.29 %.

4.2.4.3 Three Phase Five Level Trinary DC Source MLI with RC Load

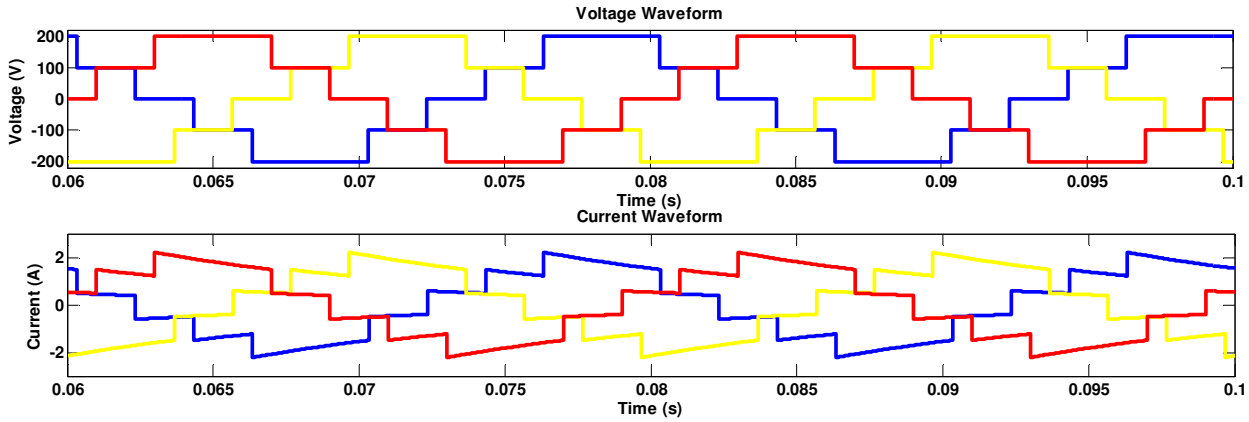


Figure 4.27: Three Phase Five Level Trinary DC Source MLI with RC Load Output

Figure 4.27 shows the output voltage and current of Three Phase Five Level Trinary DC Source MLI connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

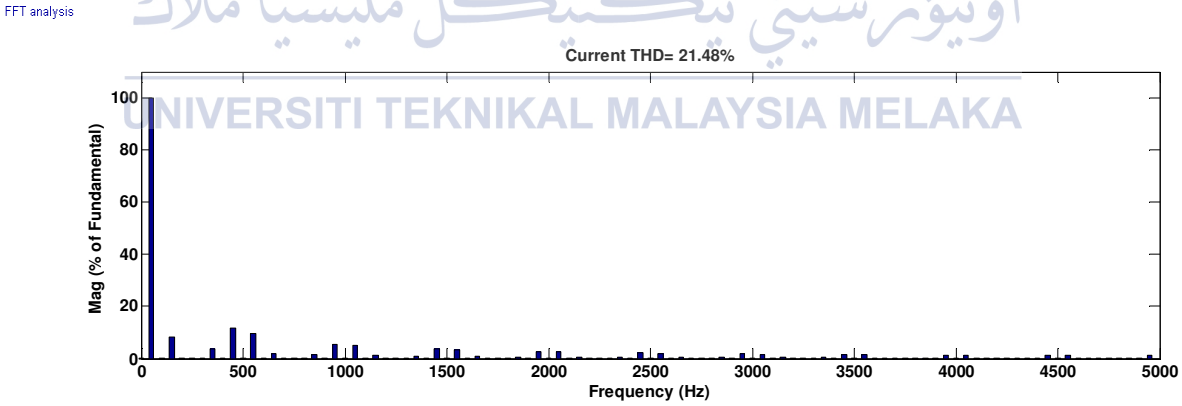


Figure 4.28: Three Phase Five Level Trinary DC Source MLI with RC Load Current Harmonic Spectrum

Figure 4.28 shows the current harmonic spectrum of Three Phase Five Level Trinary DC Source MLI connected to RC load. The value of current total harmonic distortion is 21.48 %.

4.2.5 Three Phase Seven Level Trinary DC Source MLI

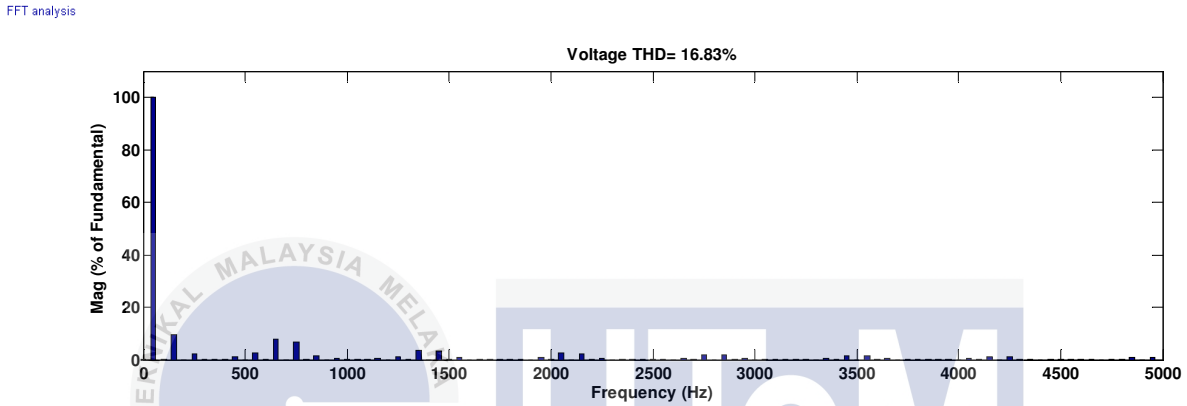


Figure 4.29: Three Phase Seven Level Trinary DC Source MLI Voltage Harmonic Spectrum

Figure 4.29 shows the voltage harmonic spectrum of the Three Phase Seven Level Trinary DC Source MLI. The voltage total harmonic distortion is 16.83 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.5.1 Three Phase Seven Level Trinary DC Source MLI with R Load

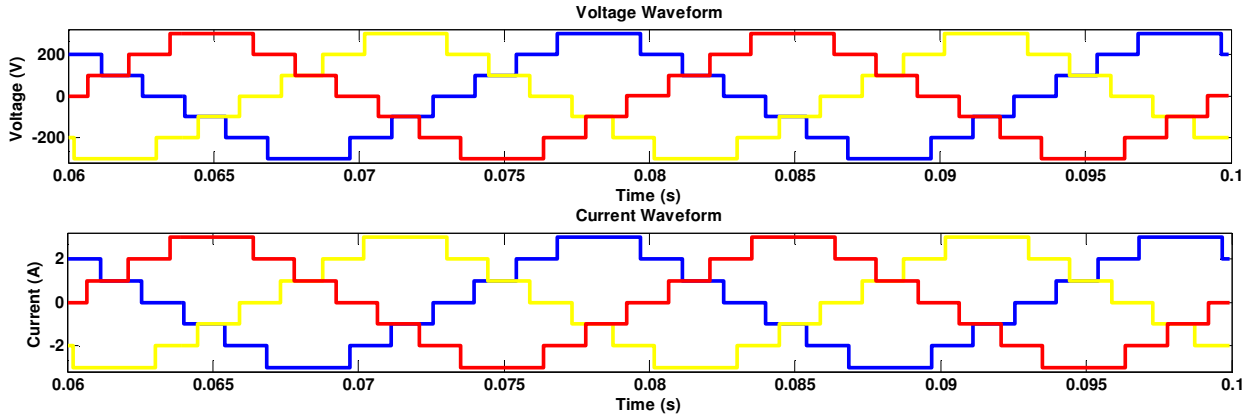


Figure 4.30: Three Phase Seven Level Trinary DC Source MLI with R Load Output

Figure 4.30 shows the output voltage and current of Three Phase Seven Level Trinary DC Source MLI connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

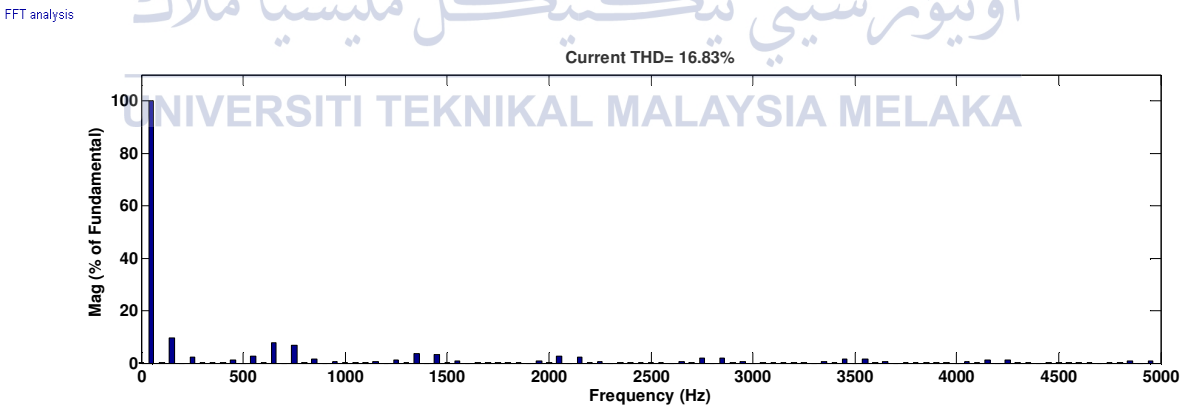


Figure 4.31: Three Phase Seven Level Trinary DC Source MLI with R Load Current Harmonic Spectrum

Figure 4.31 shows the current harmonic spectrum of Three Phase Seven Level Trinary DC Source MLI connected to R load. The value of current total harmonic distortion is 16.83 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.5.2 Three Phase Seven Level Trinary DC Source MLI with RL Load

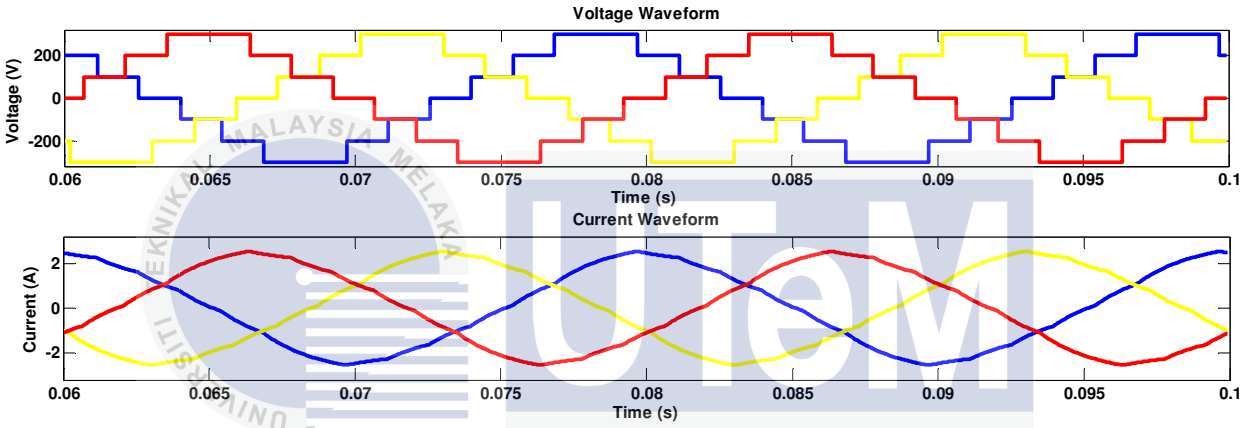


Figure 4.32: Three Phase Seven Level Trinary DC Source MLI with RL Load Output

Figure 4.32 shows the output voltage and current of Three Phase Seven Level Trinary DC Source MLI connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

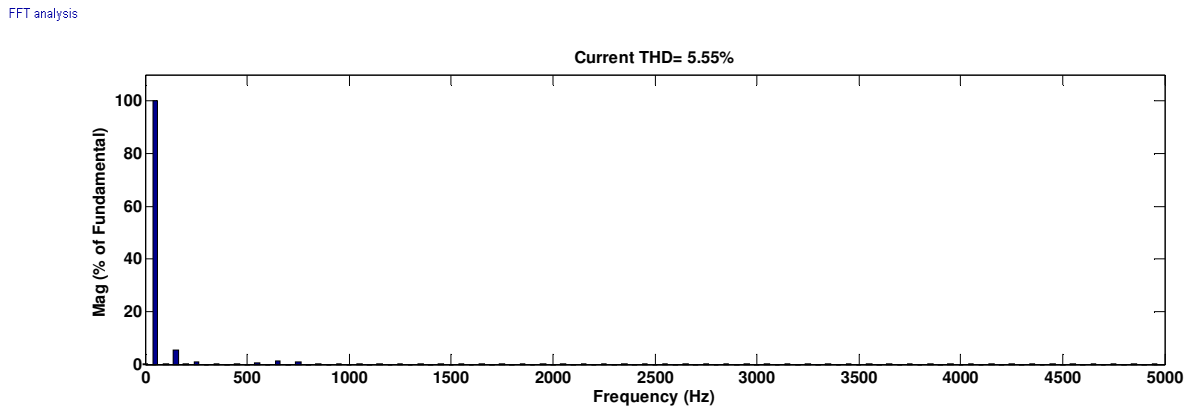


Figure 4.33: Three Phase Seven Level Trinary DC Source MLI with RL Load Current Harmonic Spectrum

Figure 4.33 shows the current harmonic spectrum of Three Phase Seven Level Trinary DC Source MLI connected to RL load. The value of current total harmonic distortion is 5.55 %.

4.2.5.3 Three Phase Seven Level Trinary DC Source MLI with RC Load

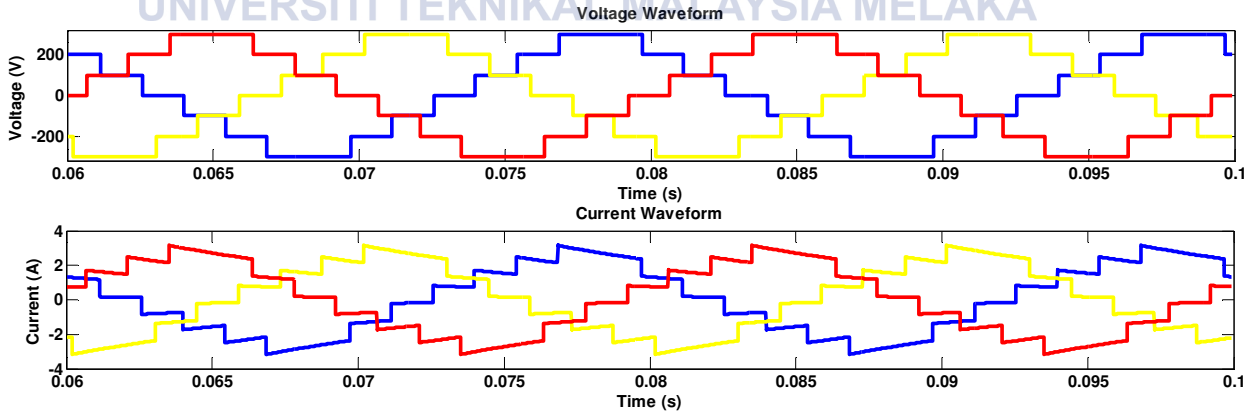


Figure 4.34: Three Phase Seven Level Trinary DC Source MLI with RC Load Output

Figure 4.34 shows the output voltage and current of Three Phase Seven Level Trinary DC Source MLI connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

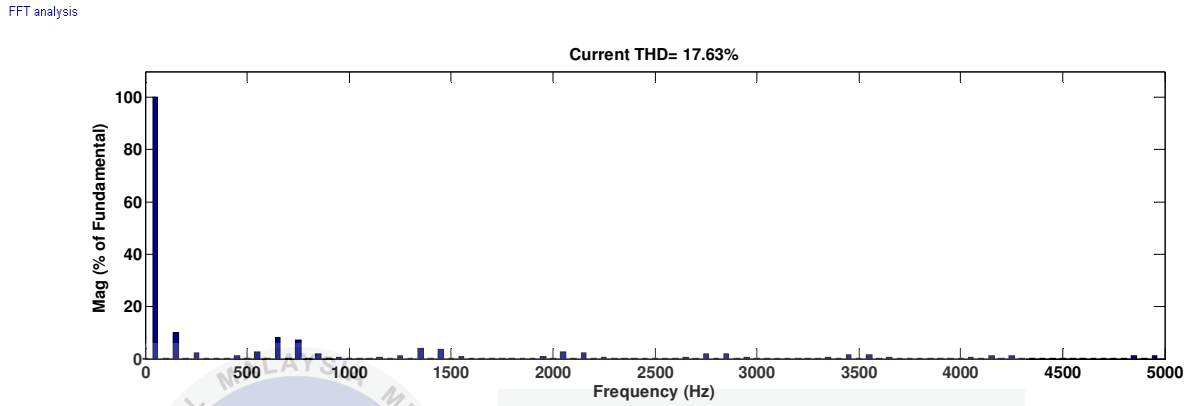


Figure 4.35: Three Phase Seven Level Trinary DC Source MLI with RC Load Current Harmonic Spectrum

Figure 4.35 shows the current harmonic spectrum of Three Phase Seven Level Trinary DC Source MLI connected to RC load. The value of current total harmonic distortion is 17.63 %.

4.2.6 Three Phase Nine Level Trinary DC Source MLI

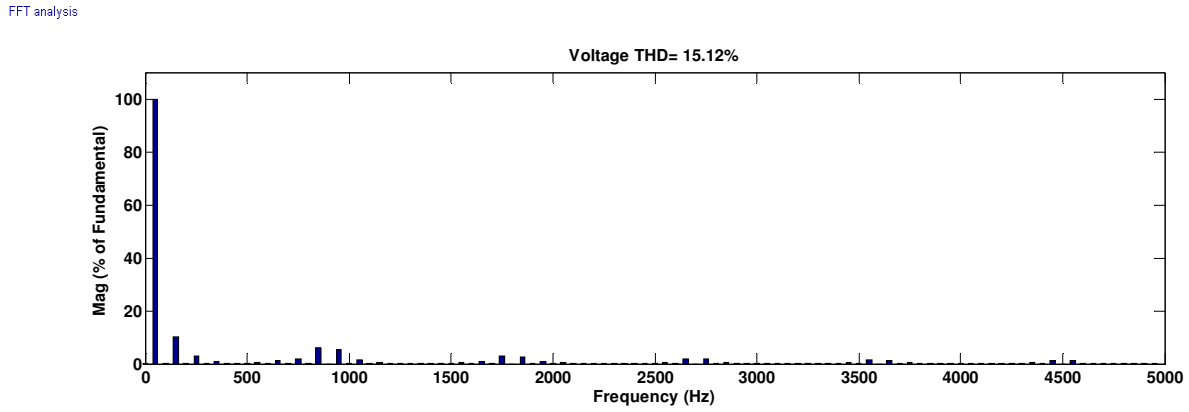


Figure 4.36: Three Phase Nine Level Trinary DC Source MLI Voltage Harmonic Spectrum

Figure 4.36 shows the voltage harmonic spectrum of the Three Phase Nine Level Trinary DC Source MLI. The voltage total harmonic distortion is 15.12 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.2.6.1 Three Phase Nine Level Trinary DC Source MLI with R Load

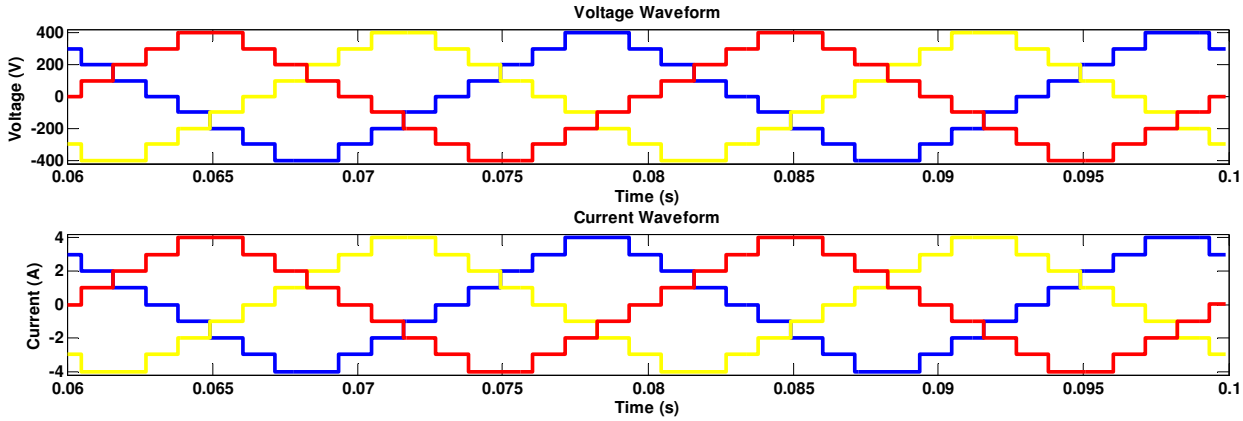


Figure 4.37: Three Phase Nine Level Trinary DC Source MLI with R Load Output

Figure 4.37 shows the output voltage and current of Three Phase Nine Level Trinary DC Source MLI connected to R load. The current waveform is same as voltage waveform because the R load will only affect the amplitude of the output current.

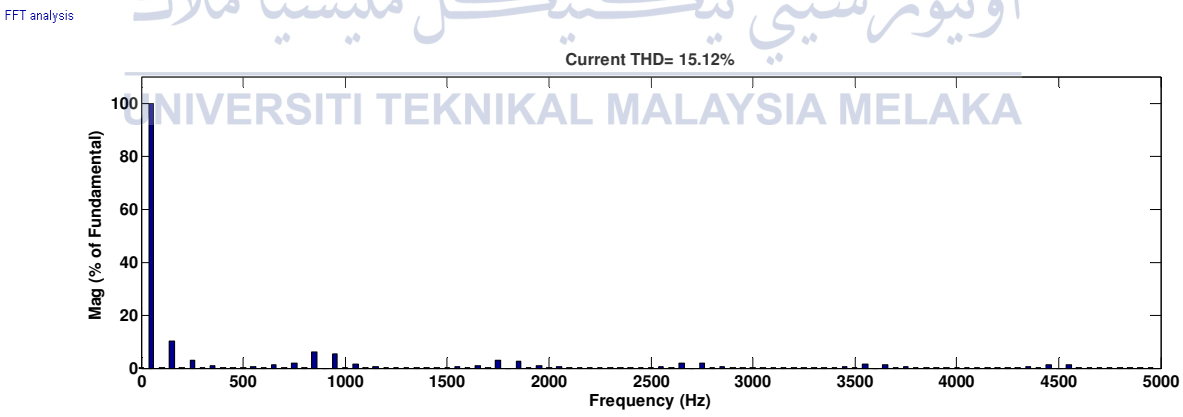


Figure 4.38: Three Phase Nine Level Trinary DC Source MLI with R Load Current Harmonic Spectrum

Figure 4.38 shows the current harmonic spectrum of Three Phase Nine Level Trinary DC Source MLI connected to R load. The value of current total harmonic distortion is 15.12 % which is same as the voltage harmonic distortion as both voltage and current waveform for R load possessed the same square waveform characteristic.

4.2.6.2 Three Phase Nine Level Trinary DC Source MLI with RL Load

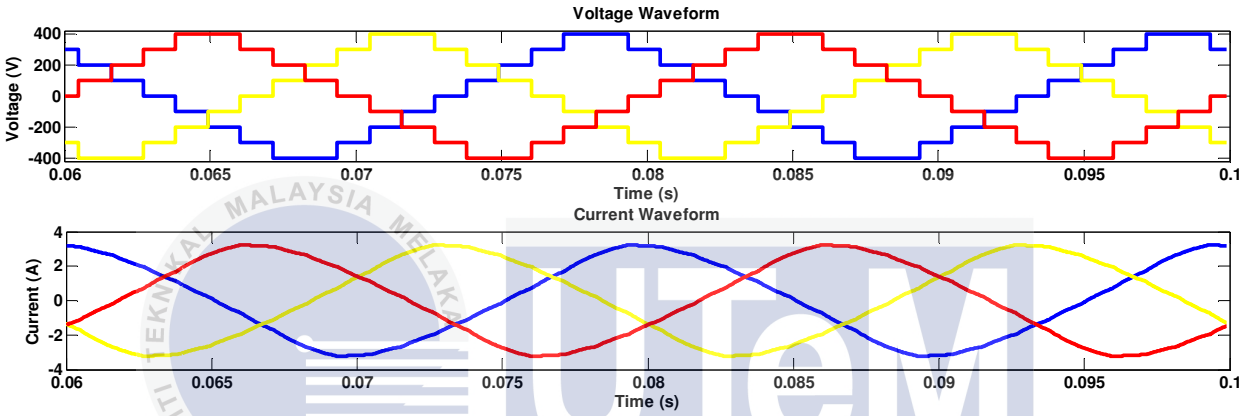


Figure 4.39: Three Phase Nine Level Trinary DC Source MLI with RL Load Output

Figure 4.39 shows the output voltage and current of Three Phase Nine Level Trinary DC Source MLI connected to RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

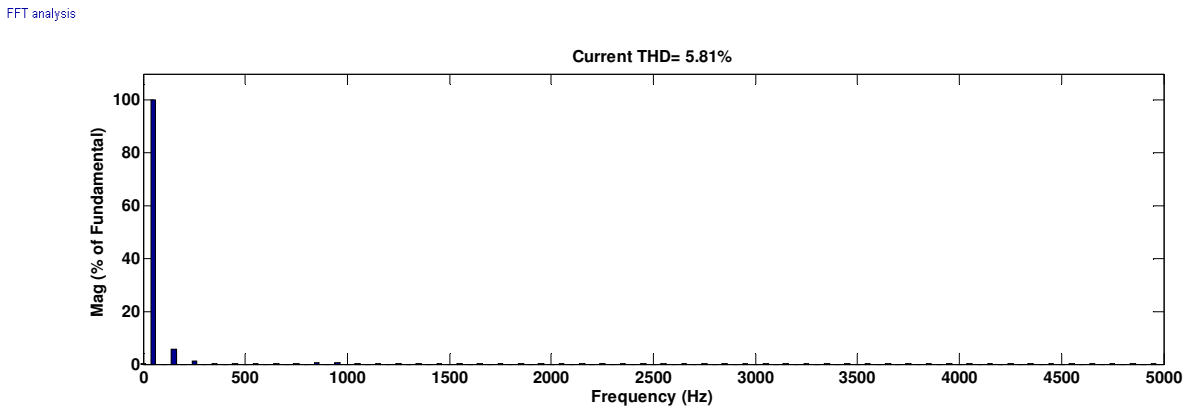


Figure 4.40: Three Phase Nine Level Trinary DC Source MLI with RL Load Current Harmonic Spectrum

Figure 4.40 shows the current harmonic spectrum of Three Phase Nine Level Trinary DC Source MLI connected to RL load. The value of current total harmonic distortion is 5.81 %.

4.2.6.3 Three Phase Nine Level Trinary DC Source MLI with RC Load

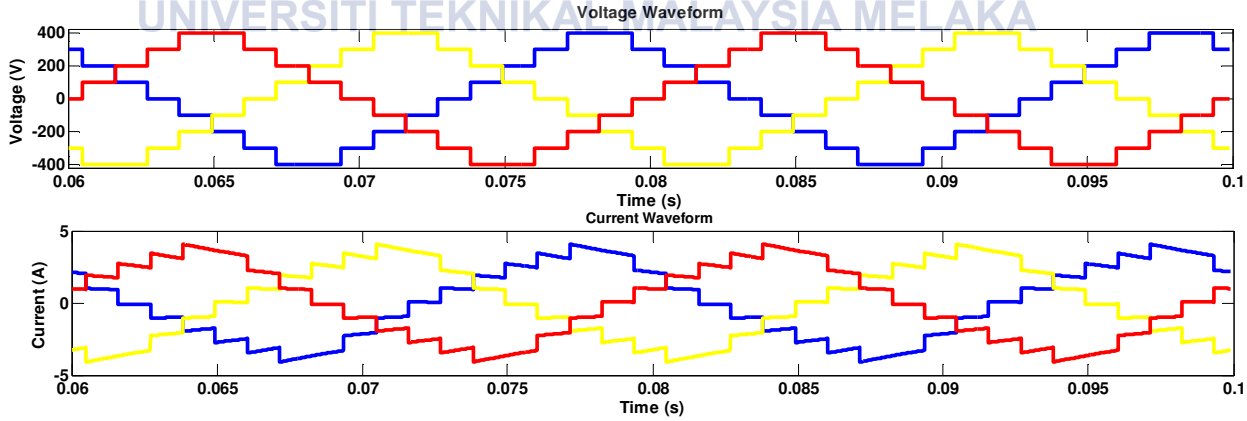


Figure 4.41: Three Phase Nine Level Trinary DC Source MLI with RC Load Output

Figure 4.41 shows the output voltage and current of Three Phase Nine Level Trinary DC Source MLI connected to RC load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the C load.

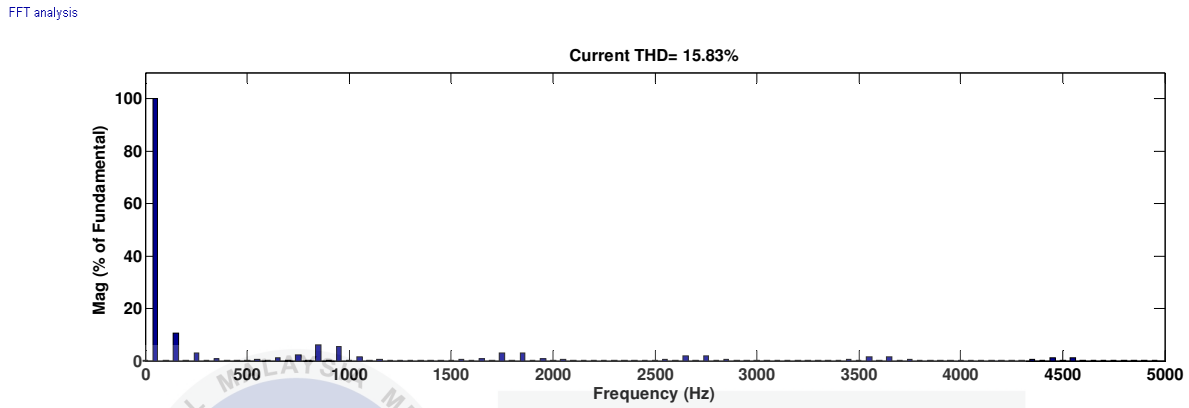


Figure 4.42: Three Phase Nine Level Trinary DC Source MLI with RC Load Current Harmonic Spectrum

Figure 4.42 shows the current harmonic spectrum of Three Phase Nine Level Trinary DC Source MLI connected to RC load. The value of current total harmonic distortion is 15.83 %.

4.3 Hardware Result

This section discuss the output waveform and harmonic spectrum result from the hardware development for Three Phase Seven Level Trinary DC Source MLI. The hardware setup for Three Phase Seven Level DC Source MLI tested only using R load and RL load. The load parameter for this experimental setup is shown in Table 4.1.

Table 4.1: Experimental Setup Load Parameter

Parameters	
R Load	228 Ω
RL Load	5 Ω, 1.6 H

4.3.1 Three Phase Seven Level Trinary DC Source MLI

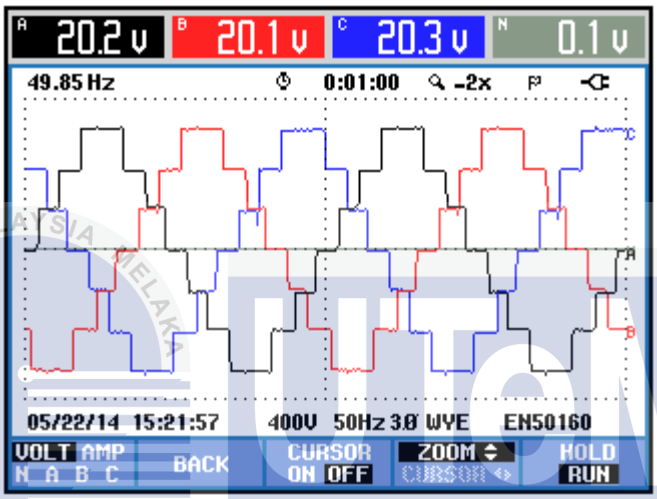


Figure 4.43: Three Phase Seven Level Trinary DC Source MLI Voltage Waveform

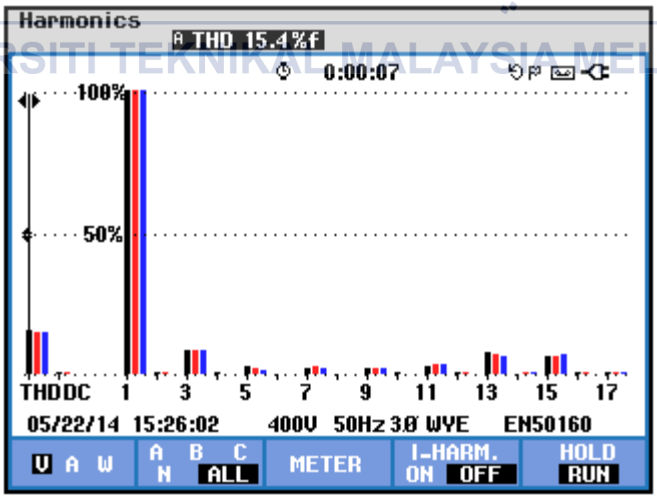


Figure 4.44: Three Phase Seven Level Trinary DC Source MLI Voltage Harmonic Spectrum

Figure 4.43 and Figure 4.44 show the voltage waveform and harmonic spectrum of the Three Phase Seven Level Trinary DC Source MLI. The voltage total harmonic distortion is 15.4 %. This value is same for any combinations of load because the output voltage will not affect although the inverter attach to various types of load.

4.3.1.1 Three Phase Seven Level Trinary DC Source MLI with R Load

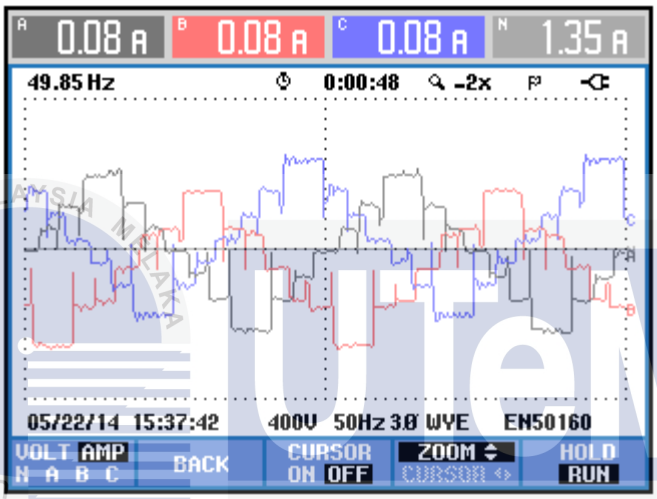


Figure 4.45: Three Phase Seven Level Trinary DC Source MLI with R Load Current Waveform

Figure 4.45 shows the output current of Three Phase Seven Level Trinary DC Source MLI connected to 228 Ω, R load. The current waveform looks quite similar as voltage waveform because the R load will only affect the amplitude of the output current.

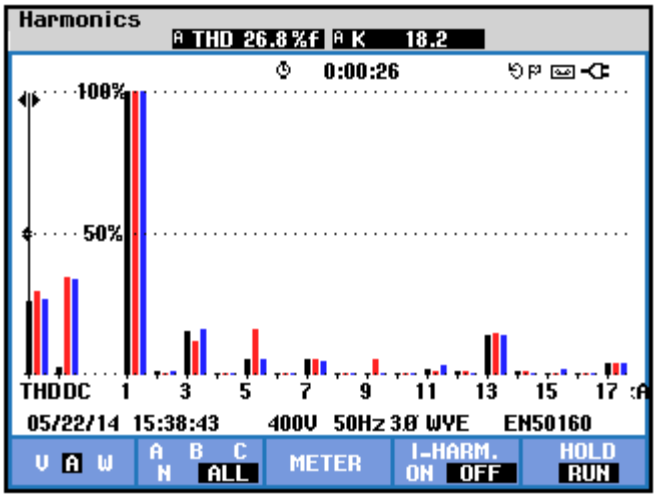


Figure 4.46: Three Phase Seven Level Trinary DC Source MLI with R Load Current Harmonic Spectrum

Figure 4.46 shows the current harmonic spectrum of Three Phase Seven Level Trinary DC Source MLI connected to 228 Ω, R load. The value of current total harmonic distortion is 26.8 %.

4.3.1.2 Three Phase Seven Level Trinary DC Source MLI with RL Load

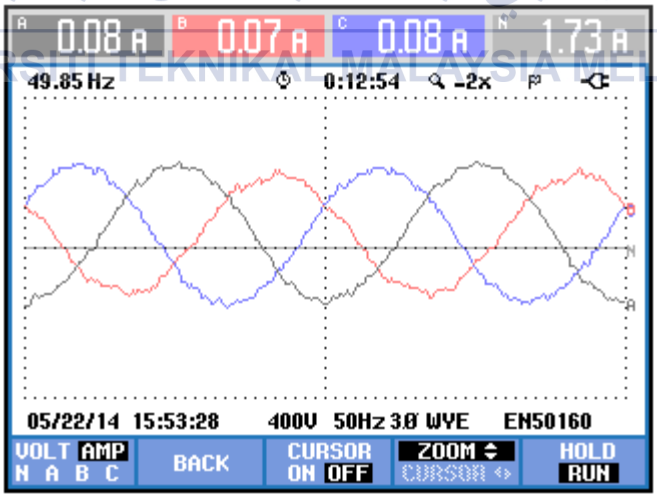


Figure 4.47: Three Phase Seven Level Trinary DC Source MLI with RL Load Current Waveform

Figure 4.47 shows the output voltage and current of Three Phase Seven Level Trinary DC Source MLI connected to 5 Ω and 1.6 H, RL load. The current waveform is different compared to the voltage waveform because of the charge and discharge characteristic of the L load.

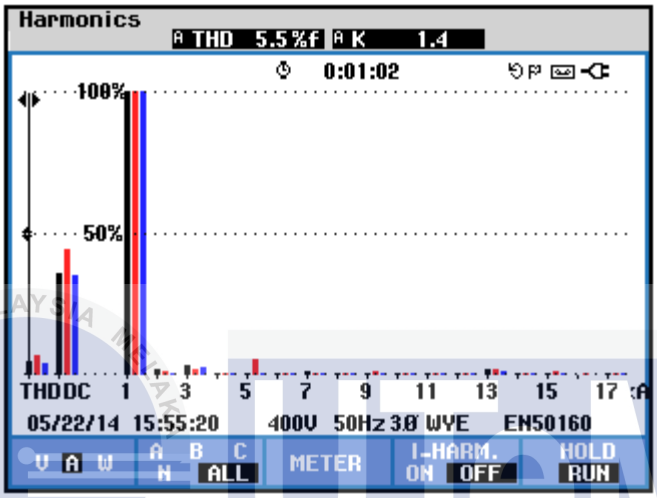


Figure 4.48: Three Phase Seven Level Trinary DC Source MLI with RL Load Current Harmonic Spectrum

Figure 4.48 shows the current harmonic spectrum of Three Phase Seven Level Trinary DC Source connected to 5 Ω and 1.6 H, RL load. The value of current total harmonic distortion is 5.5 %.

4.4 Summary

The voltage and current THD data in Table 4.2 and Table 4.3 collected from the MATLAB/Simulink simulation by using Fast Fourier Transform (FFT) Analysis embedded in the MATLAB/Simulink software itself.

Table 4.2: Comparison between Various Inverter Voltage THD

Load	Conventional MLI		Trinary MLI			
	Square	Quasi	Three Level	Five Level	Seven Level	Nine Level
R,L,C	48.34 %	31.08 %	31.08 %	20.48 %	16.83 %	15.12 %

Table 4.2 shows the comparison of voltage THD between Three Phase Square Inverter, Quasi Inverter and Trinary DC Source MLI. The Three Level Trinary DC Source MLI produced same voltage THD as the Quasi Inverter because the output voltage waveform generated by Quasi Inverter is same as the Three Level Trinary DC Source MLI. Square Inverter contributes the highest voltage THD among all and for Trinary DC Source MLI, the voltage THD is decrease as the number of level increase. The Nine Level Trinary DC Source MLI contributes the lowest voltage THD.

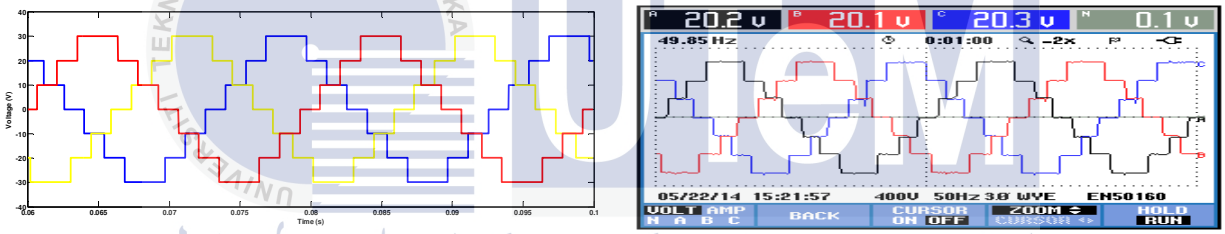
Table 4.3: Comparison between Various Inverter Current THD

Load	Conventional MLI		Trinary MLI			
	Square	Quasi	Three Level	Five Level	Seven Level	Nine Level
R	48.34 %	31.08 %	31.08 %	20.48 %	16.83 %	15.12 %
RL	20.41 %	8.37 %	8.37 %	5.29 %	5.55 %	5.81 %
RC	50.57 %	32.59 %	32.59 %	21.48 %	17.63 %	15.83 %

Table 4.3 shows the comparison of current THD between Three Phase Square Inverter, Quasi Inverter and Trinary DC Source MLI connected to various load combination. As mentioned in the voltage THD section, the Three Level Trinary DC Source MLI produced same current THD as the Quasi Inverter as well because the output current waveform generated by Quasi Inverter is also same as the Three Level Trinary DC Source MLI. Square

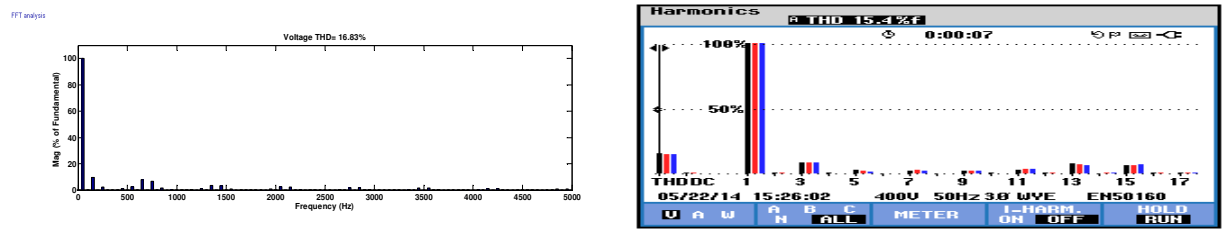
Inverter contributes the highest current THD among all. For Trinary DC Source MLI, the current THD for R and RC connected load is decrease as the number of level increase. While for RL connected load, the current THD is decrease from three level to five level types of inverter but slightly increase for five level to nine level inverter. However this slight increase can be neglect as it is too small. Overall, the Nine Level Trinary DC Source MLI contributes the lowest voltage THD.

The voltage waveform and frequency spectrum in Figure 4.49 and Figure 4.50 are collected from the MATLAB/Simulink simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI.



(a) Simulation (b) Hardware

Figure 4.49: Comparison between Simulation and Hardware Voltage Waveform



(a) Simulation (b) Hardware

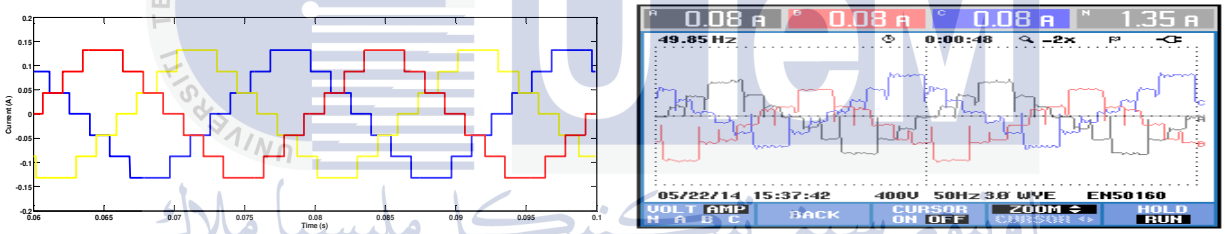
Figure 4.50: Comparison between Simulation and Hardware Voltage Frequency Spectrum

The voltage THD data in Table 4.4 are extracted from the MATLAB/Simulink simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI as shown in Figure 4.50.

Table 4.4: Comparison between Simulation and Hardware Voltage THD

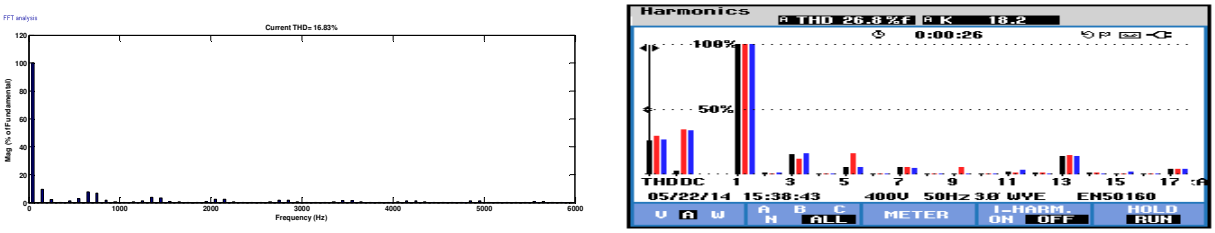
Load	Simulation	Hardware	% error
R,L	16.83 %	15.4 %	8.5 %

The current waveform and frequency spectrum in Figure 4.51 and Figure 4.52 are collected from the MATLAB/Simulink simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI with R load.



(a) Simulation (b) Hardware

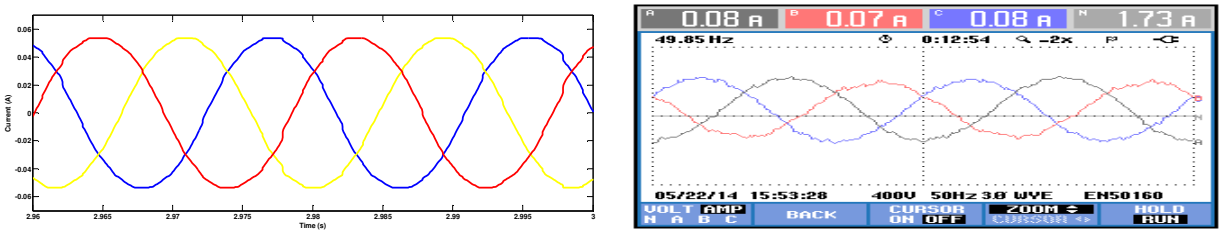
Figure 4.51: Comparison between Simulation and Hardware Current Waveform with R Load



(a) Simulation (b) Hardware

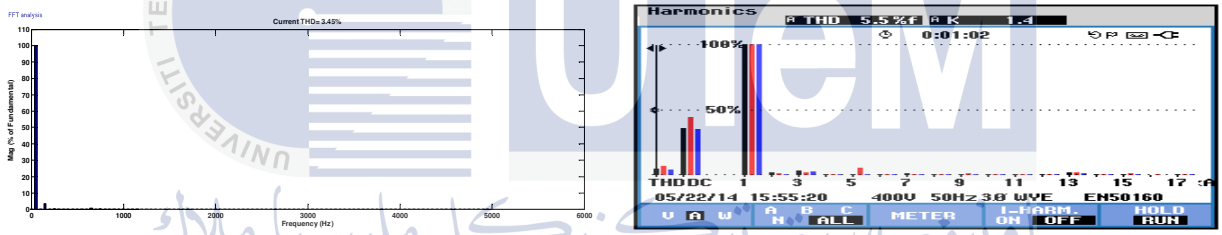
Figure 4.52: Comparison between Simulation and Hardware Current Frequency Spectrum with R Load

The current waveform and frequency spectrum in Figure 4.53 and Figure 4.54 are collected from the MATLAB/Simulink simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI with RL load.



(a) Simulation (b) Hardware

Figure 4.53: Comparison between Simulation and Hardware Current Waveform with RL Load



(a) Simulation (b) Hardware

Figure 4.54: Comparison between Simulation and Hardware Current Frequency Spectrum with RL Load

The current THD data in Table 4.5 are extracted from the MATLAB/Simulink simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI with R Load and Three Phase Seven Level Trinary DC Source MLI with RL Load as shown in Figure 4.52 and Figure 4.54.

Table 4.5: Comparison between Simulation and Hardware Current THD

Load	Simulation	Hardware	% error
R	16.83 %	26.8 %	-59.24 %
RL	3.45 %	5.5 %	-59.42 %

Table 4.4 and Table 4.5 show the comparison of voltage and current THD between simulation and hardware result of the Three Phase Seven Level Trinary DC Source MLI connected to R and RL load. The value of simulation and hardware result is slightly different but still can be accepted because in the simulation, ideal component is used while in the hardware, it is impossible to have the ideal component. Furthermore, the spiking or transient current that occur during switching also contribute to the increase of THD in experimental setup.

CHAPTER 5

CONCLUSION

Many power electronics equipments are designed to have as minimum losses as possible. For inverters, switching losses is one of the biggest enemies. Many types of inverters have been produced in terms of either low or high frequency. Trinary DC Source MLI used low frequency and simple algorithm for their switching generation, so the switching losses can be minimized and easy to implement compared to other inverters that produce the same output but require high frequency or complex switching signal generation. Besides, among the existing inverters, this topology requires the minimum number of component for high levels output voltage. In addition, the voltage THD is also decrease as the number of level is increase. Three Level Trinary MLI produce 31.08 % of voltage THD meanwhile for Nine Level Trinary MLI, the voltage THD reduce to 15.12 %. This proved that the output voltage level of Trinary MLI is significantly affected to the voltage THD, which is higher level of Trinary MLI will produce lower voltage THD. Hardware and simulation result shows that for RL load, the current THD is less than using R load.

RECOMMENDATION

Based on Table 4.5, shows that the current THD is quite high compared to the simulation current THD. This is because there are current transient occur during the switching which can be seen in Figure 4.51 and Figure 4.53. This spike can be eliminates by using snubber circuit. Snubber circuit functioned as a protection of transient current for IGBT. It is suggested that the hardware setup used snubber to reduce the THD. Figure 5.1 shows the RCD snubber clamp circuit that can be used.

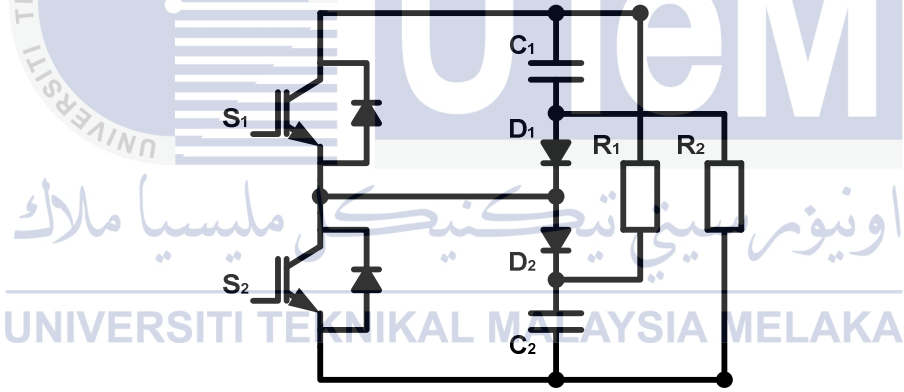


Figure 5.1: RCD Snubber Clamp Circuit

REFERENCES

[1] Acha, E., & Madrigal, M. (2001) Power Quality. *Power Systems Harmonics: Computer Modelling and Analysis* (pp. 4-5). Chichester: Wiley.

[2] Kularatna, N. (1998). Power Factor Correction and Harmonic Control. *Power Electronics Design Handbook Low-Power Components and Applications* (pp. 248-249). Boston: Newnes.

[3] Prathiba, T., and Renuga, P. (2012). A comparative Study of Total Harmonic Distortion in Multilevel Inverter Topologies. *Journal of Information Engineering and Applications,* 2(3), 26-36.

[4] Hart, D.W. (2011). Inverters. *Power Electronics* (pp. 331-340). New York: McGraw-Hill.

[5] Luo, F. L., & Ye, H. (2010). *Power electronics: advanced conversion technologies*. Boca Raton: CRC Press/Taylor & Francis.

[6] Mohan, N., & Undeland, T. M. (2003). *Power electronics: converters, applications, and design* (3rd ed.). New York: John Wiley & Sons.

[7] Jacob, J. M. (2002). *Power electronics: principles & applications*. Albany: Delmar Thomson Learning.

[8] Rashid, M. H. (2001). *Power electronics handbook*. San Diego: Academic Press.

[9] Colak, I., Kabalci, E., & Bayindir, R. (2011). Review of Multilevel Voltage Source Inverter Topologies and Control Schemes. *Energy Conversion and Management,* 52(2), 1114-1128.

[10] Rodriguez, Lai, J. S., & Peng, F. Z. (2002). Multilevel Inverters: A Survey Of Topologies, Controls, And Applications. *IEEE Transactions on Industrial Electronics*, *49*(4), 724-738.

[11] Franquelo L. G., Rodriguez J., Kouro S., Portillo R., and Prats M. A. M. (2008). The age of multilevel converter arrives. *IEEE Ind. Electron. Magazine*, 28-39.

[12] Lai, J. S., and Peng, F. Z. (1996). Multilevel Converters-A New Breed of Power Converters. *IEEE Trans. Ind. Appl.,* 32(3), 509-517.

[13] Corzine, K. A., Wielebski, M. W., and Peng, F. Z. (2004). Control of Cascaded Multilevel Inverters. *IEEE Trans. Power Electronics,* 19, 732-738.

[14] Zope, P.H., Bhangale, P.G., Sonare, P. & Suralkar, S.R. (2012). Design and Implementation of Carrier Based Sinusoidal PWM Inverter. *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,* 1(4), 230-236.

[15] Ashok, B., and Rajendran, A. (2013). Selective Harmonic Elimination of Multilevel Inverter using SHE PWM Technique. *International Journal of Soft Computing and Engineering (IJSCE),* 3(2), 79-82.

[16] Bharath, R. & Arun V. (2012). 9-Level Trinary DC Source Inverter Using Embedded Controller. *IOSR Journal of Engineering (IOSRJEN),* 2(10), 90-95.

[17] L. M. Tolbert, F. Z. Peng, and T. Habetler (1999). Multilevel Converters for Large Electric Drives. *IEEE Trans. Ind. Applicat*, 35, 36-44.

[18] R. Seyezhai and B. L. Mathur (2008). Hybrid cascaded H-bridge multilevel inverter for fuel cell power conditioning systems. 1-5.

[19] S. Daher, J. Schmid, and F. M. L. Antunes (2008). Multilevel Inverter Topologies for Stand-alone PV Systems. IEEE Transactions on Industrial Electronics, 55, 2703-2712.

[20] Y. S. Lai and F. S. Shyu (2003). Topology for hybrid multilevel inverter. 449-458.

[21] Nurul Aisyah Yusof, Norazliani Md Sapari, Hazlie Mokhlis, and Jeyraj Selvaraj (2012). A Comparative Study of 5-level and 7-level Multilevel Inverter Connected to the Grid. *IEEE International Conference on Power and Energy (PECon)*, 542.

APPENDIX A: IGBT IHW30N90T DATASHEET

IHW30N90T

Soft Switching Series

Low Loss DuoPack : IGBT in TrenchStop® and Fieldstop technology with anti-parallel diode

Features:

- 1.1V Forward voltage of antiparallel diode
- TrenchStop® and Fieldstop technology for 900 V applications offers :
  - very tight parameter distribution
  - high ruggedness, temperature stable behavior
  - easy parallel switching capability due to positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Qualified according to JEDEC[1] for target applications
- Application specific optimisation of inverse diode
- Pb-free lead plating; RoHS compliant

Applications:

- Microwave Oven
- Soft Switching Applications for ZCS

Type	V_{CE}	I_C	$V_{CE(sat),T_j=25°C}$	$T_{j,max}$	Marking	Package
IHW30N90T	900V	30A	1.5V	175°C	H30T90	PG-TO-247-3

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	900	V
DC collector current	I_C		A
T_C = 25°C		60	
T_C = 100°C		30	
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	90	
Turn off safe operating area $V_{CE} \le 900V$, $T_j \le 175°C$	-	90	
Diode forward current	I_F		
T_C = 25°C		23	
T_C = 100°C		13	
Diode pulsed current, t_p limited by T_{jmax}	I_{Fpuls}	36	
Gate-emitter voltage	V_{GE}	±20	V
Transient Gate-emitter voltage (t_p < 5 ms)		±25	
Power dissipation, T_C = 25°C	P_{tot}	428	W
Operating junction temperature	T_j	-40...+175	°C
Storage temperature	T_{stg}	-55...+175	°C
Soldering temperature, 1.6mm (0.063 in.) from case for 10s	-	260	

[1] J-STD-020 and JESD-022

APPENDIX B: GATE DRIVE HCPL-3120-000E DATASHEET

HCPL-3120/J312, HCNW3120

2.5 Amp Output Current IGBT Gate Drive Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

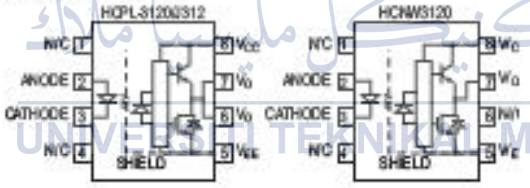
Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available; -xxxE denotes a lead-free product

Description

The HCPL-3120 contains a GaAsP LED while the HCPL-J312 and the HCNW3120 contain an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the HCPL-3120 series can be used to drive a discrete power stage which drives the IGBT gate. The HCNW3120 has the highest insulation voltage of V_{IORM} = 1414 Vpeak in the IEC/EN/DIN EN 60747-5-2. The HCPL-J312 has an insulation voltage of V_{IORM} = 891 V_{peak} and the V_{IORM} = 630 V_{peak} is also available with the HCPL-3120 (Option 060).

Functional Diagram



TRUTH TABLE

LED	V_{CC} - V_{EE} "POSITIVE GOING" (i.e., TURN-ON)	V_{CC} - V_{EE} "NEGATIVE GOING" (i.e., TURN-OFF)	V_O
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

Features

- 2.5 A maximum peak output current
- 2.0 A minimum peak output current
- 25 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- 0.5 V maximum low level output voltage (V_{OL}) Eliminates need for negative gate drive
- I_{CC} = 5 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} range: 15 to 30 Volts
- 500 ns maximum switching speeds
- Industrial temperature range: -40°C to 100°C
- Safety Approval:
  - UL Recognized
    - 3750 Vrms for 1 min. for HCPL-3120/J312
    - 5000 Vrms for 1 min. for HCNW3120
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-2 Approval
    - V_{IORM} = 630 V_{peak} for HCPL-3120 (Option 060)
    - V_{IORM} = 891 V_{peak} for HCPL-J312
    - V_{IORM} = 1414 V_{peak} for HCNW3120

Applications

- IGBT/MOSFET gate drive
- AC/Brushless DC motor drives
- Industrial inverters
- Switch mode power supplies

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

APPENDIX C: DC/DC CONVERTER IQ0515SA DATASHEET

1 Watt
IQ Series

xppower.com

- Single & Dual Output
- SIP Package
- 1000 VDC Isolation
- Optional 3000 VDC Isolation
- -40 °C to +85 °C Operation
- Semi-regulated
- 3 Year Warranty

Specification

Input

Input Voltage Range	• Nominal ±10%
Input Reflected Ripple Current	• 5 & 12 V: 20 mA, 15 V: 30 mA 24 V: 40 mA, 48 V: 50 mA pk-pk, 5 Hz to 20 MHz
Input Reverse Voltage Protection	• None

Output

Output Voltage	• See table
Minimum Load	• None[4]
Line Regulation	• 1.2%/1% Δ Vin
Load Regulation	• See table (10-100%)
Setpoint Accuracy	• ±3%
Ripple & Noise[5]	• 50 mV pk-pk max, 20 MHz bandwidth
Temperature Coefficient	• 0.02 %/°C
Maximum Capacitive Load	• See table

General

Efficiency	• See table
Isolation Voltage	• 1000 VDC minimum, 3000 VDC option[6]
Isolation Resistance	• 10⁹ Ω
Isolation Capacitance	• 60 pF typical
Switching Frequency	• Variable, 55 kHz-85 kHz
MTBF	• >1.1 MHrs to MIL-HDBK-217F at 25 °C, GB

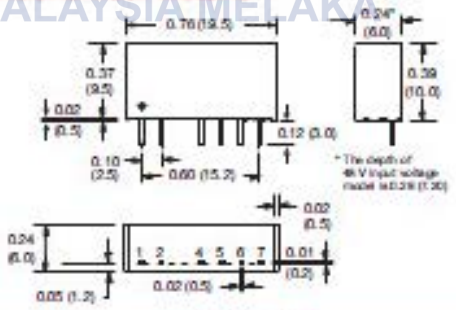
Environmental

Operating Temperature	• -40 °C to +85 °C
Storage Temperature	• -40 °C to +125 °C
Case Temperature	• 100 °C max
Cooling	• Convection-cooled

Input Voltage	Output Voltage	Output Current	No Load Input Current	Max Capacitive Load	Efficiency	Load Reg.	Model[7] Number
5 VDC	5.0 V	200 mA	20 mA	200 µF	83%	6.0%	IQ0505SA†^
	9.0 V	111 mA	20 mA	200 µF	86%	5.5%	IQ0509SA†^
	12.0 V	83 mA	20 mA	100 µF	87%	5.5%	IQ0512SA†^
	15.0 V	67 mA	20 mA	100 µF	87%	5.0%	IQ0515SA†^
12 VDC	5.0 V	200 mA	15 mA	200 µF	84%	4.0%	IQ1205SA†^
	9.0 V	111 mA	15 mA	200 µF	86%	3.5%	IQ1209SA†^
	12.0 V	83 mA	15 mA	100 µF	88%	3.5%	IQ1212SA†^
	15.0 V	67 mA	15 mA	100 µF	88%	3.0%	IQ1215SA†^
15 VDC	5.0 V	200 mA	10 mA	200 µF	84%	4.0%	IQ1505SA†^
	9.0 V	111 mA	10 mA	200 µF	86%	3.5%	IQ1509SA†^
	12.0 V	83 mA	10 mA	100 µF	87%	3.5%	IQ1512SA†^
	15.0 V	67 mA	10 mA	100 µF	89%	3.0%	IQ1515SA†^
24 VDC	5.0 V	200 mA	7 mA	200 µF	81%	4.0%	IQ2405SA†^
	9.0 V	111 mA	7 mA	200 µF	84%	3.5%	IQ2409SA†^
	12.0 V	83 mA	7 mA	100 µF	85%	3.5%	IQ2412SA†^
	15.0 V	67 mA	7 mA	100 µF	86%	2.5%	IQ2415SA†^
48 VDC	5.0 V	200 mA	5 mA	200 µF	78%	4.0%	IQ4805SA†^
	9.0 V	111 mA	5 mA	200 µF	80%	3.5%	IQ4809SA†^
	12.0 V	83 mA	5 mA	100 µF	81%	3.0%	IQ4812SA†^
	15.0 V	67 mA	5 mA	100 µF	81%	3.0%	IQ4815SA†^

† Available from Farnell & element14. See pages 284-290.
^ Available from Newark. See pages 291-296.

Mechanical Details



Notes

1. Operation at no load will not damage unit but it may not meet all specifications.
2. For optional 3000 VDC isolation, add suffix '-H' to the model number.
3. For dual output delete suffix 'A' and split output current equally between rails.
4. All dimensions in inches (mm).
5. Pin pitch tolerance: ±0.014 (±0.35)
6. Case tolerance: ±0.02 (±0.5)
7. Weight: 0.05 lbs (2.8 g)

Pin Connections				
Pin	Single	Dual	Single-H	Dual-H
1	+Vin	+Vin	+Vin	+Vin
2	-Vin	-Vin	-Vin	-Vin
4	-Vout	-Vout	N.P.	N.P.
5	N.P.	Common	-Vout	-Vout
6	+Vout	+Vout	N.P.	Common
7	N.P.	N.P.	+Vout	+Vout

APPENDIX D: PCB DESIGN

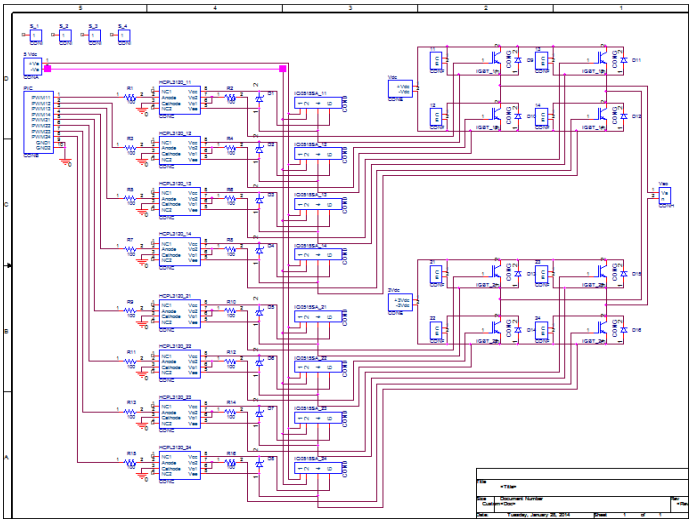


Figure AE - 1: OrCad Capture CIS Diagram

Figure AE - 1 shows the designed circuit drawn by using OrCad Capture CIS before it is transferred to OrCad Layout Plus.

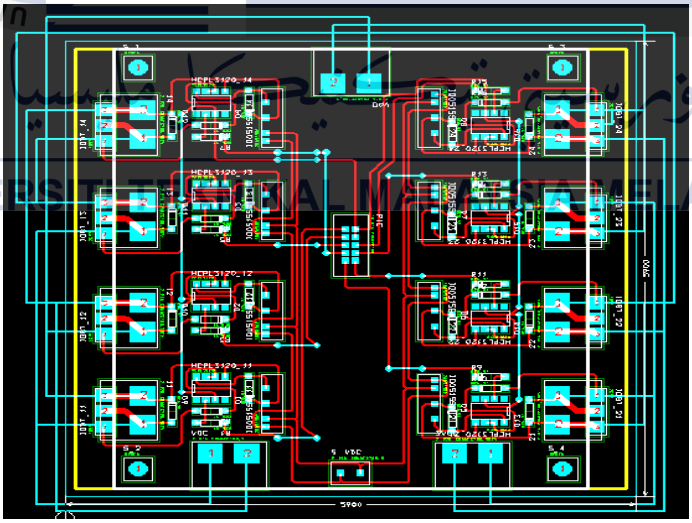


Figure AE - 2: OrCad Layout Plus PCB Layout

Figure AE - 2 shows the designed circuit diagram after being transferred to PCB Layout by using OrCad Layout Plus.

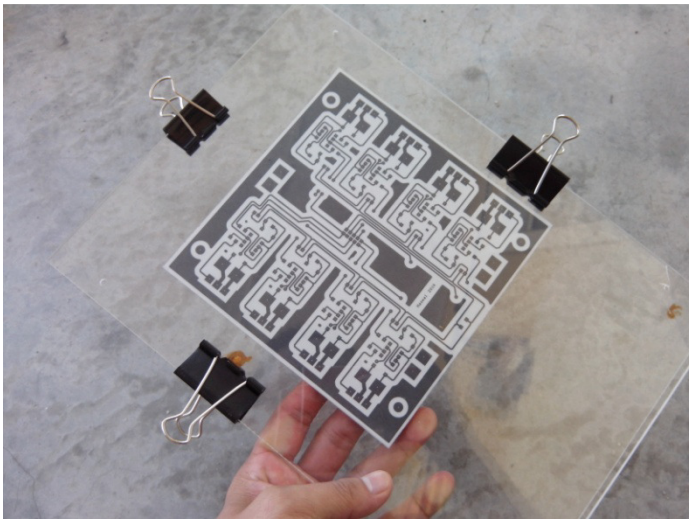


Figure AE - 3: Printed PCB Layout

Figure AE - 3 shows the PCB layout printed on the tracing paper. The tracing paper is then placed on an Ultra Violet (UV) board and exposed to the sun for about one minute to able the UV board to capture the printed image.

Figure AE - 4: PCB Developer

Figure AE - 4 shows the UV board with the designed circuit on top of it is soaked in PCB Developer to wipe out the entire unwanted UV layer to reveal the designed circuit.

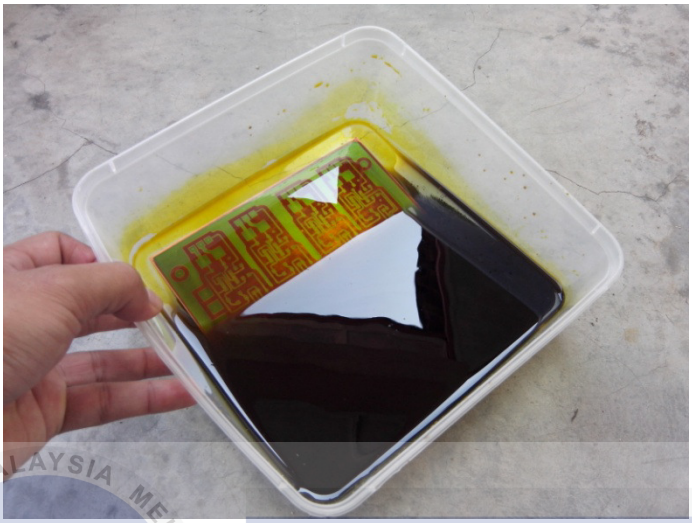


Figure AE - 5: Ferric Chloride

Next step, the PCB is soaked into Ferric Chloride to wipe out the unwanted copper layer on the PCB as shown in Figure AE - 5.

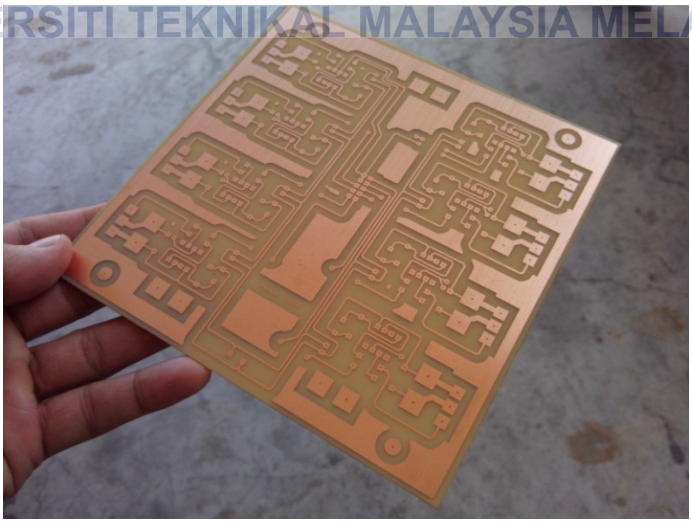


Figure AE - 6: Designed PCB

Figure AE - 6 shows the finish product of the designed PCB. For Three Phase Seven Level Trinary DC Source MLI, the similar PCB is duplicate two more for yellow and blue phase.

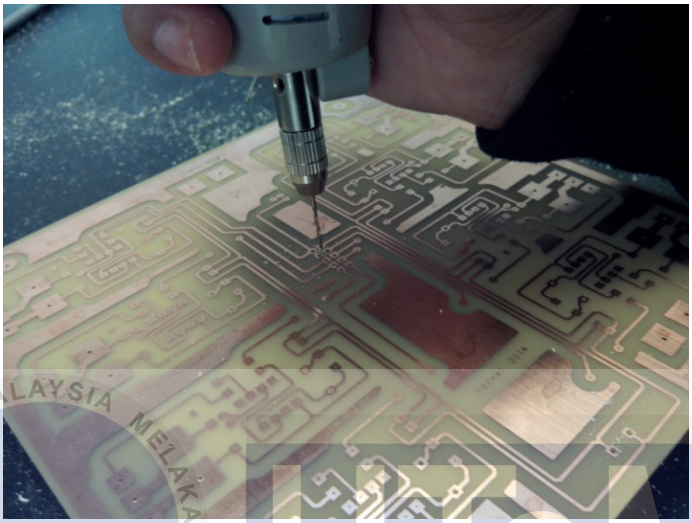


Figure AE - 7: Hole Drilling

Figure AE - 7 shows the drilling process of the PCB. The hole is drilled based on the components exact size.

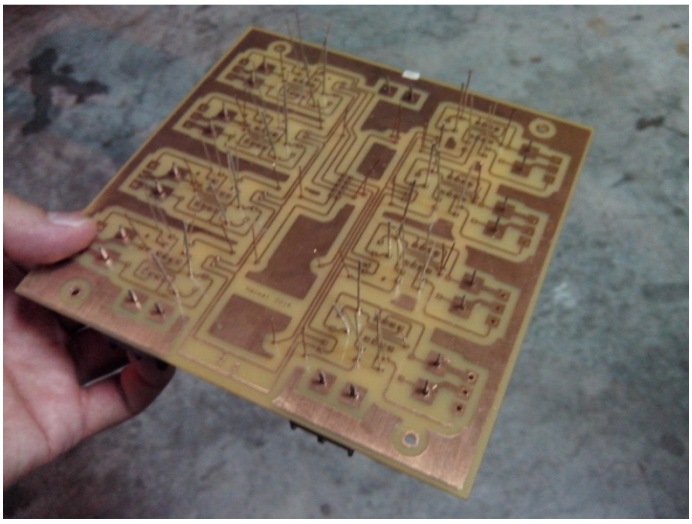


Figure AE - 8: Component Insertion

Figure AE - 8 shows the component being inserted into the PCB and ready to be soldered.

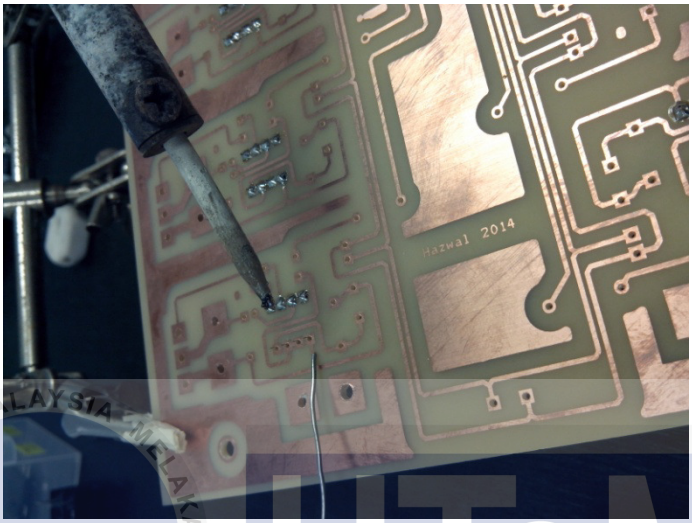


Figure AE - 9: Soldering

Figure AE - 9 shows the soldering process after the component had been inserted onto the PCB board. The circuit then is tested by using multi-meter and other suitable equipment such as oscilloscope and DC power supply to make sure that the circuit is in good condition.

APPENDIX E: JOURNAL

IOSR Journal of Engineering (IOSRJEN)
e-ISSN: 2250-3021, p-ISSN: 2278-8719, www.iosrjen.org
Volume 2, Issue 10 (October 2012), PP 90-95

9-Level Trinary DC Source Inverter Using Embedded Controller

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Abstract : *This paper presents the Trinary DC source H-bridge multilevel multilevel inverter. Embedded switching pattern scheme is used to improve the performance of Multilevel Inverter. This scheme reduces the switching loss. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. Unlike other schemes, the proposed firing method significantly reduces the Total Harmonic Distortion (THD) and switching losses. The circuit configuration is simple and easy to control.To validate the developed technique; simulations are carried out through MATLAB/SIMULINK.*

Keywords: *THD, Vrms, MLI, Embedded controller .*

I. INTRODUCTION

Multilevel inverters can be divided into three presentable topologies; diode-clamped, flying-capacitor, and cascaded H-bridge cell [1]-[5]. Among them, cascaded H-bridge multilevel inverters have been received a great attention because of their merits such as minimum number of components, reliability, and modularity. In the viewpoint of obtaining a sinusoidal output voltage wave, multilevel inverters may increase the number of output voltage levels. However, it will need more components resulted in complexity and cost increase. To minimize these drawbacks, multilevel inverters employing cascaded transformers have been studied [6]-[8]. Owing to the Trinary characteristic of output voltage, they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer, they obtain galvanic isolation between source and loads. However, the transformer may decrease the power conversion efficiency, and volume and cost will be increased To alleviate these problems, we propose a cascaded H-bridge multilevel inverter using Trinary DC input source without transformers [6] To alleviate these problems, we propose a cascaded H-bridge multilevel inverter using trinary dc input source without transformers [6]. This circuit topology is simple and easy to control. The operational principle and key waveforms are illustrated in detail.This paper presents a single phase Trinary DC source nine level inverter topology for investigation with embedded controller switching technique. Simulations were performed using MATLAB-SIMULINK.

II. BASIC OPERATION OF MULTILEVEL INVERTER

Fig. 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing Trinary DC input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using Vdc and 3Vdc, it can synthesize nine output levels; -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc.The lower inverter generates a fundamental output voltage with three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$V_{out} = V_{1(01)} + V_{1(02)} \qquad (1)$$

In the proposed circuit topology, if n number of H-bridge module has independent DC sources in sequence of the power of 3, an expected output voltage level is given as

$$V_n = 3^n, n = 1, 2, 3.. \qquad (2)$$

TABLE. I
Switching Sequence of Trinary MLI

V_{out}	S11	S12	S13	S14	S21	S22	S23	S24
4Vdc	1	0	0	1	1	0	0	1
3Vdc	0	1	0	1	1	0	0	1
2Vdc	0	1	1	0	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2Vdc	1	0	0	1	0	1	1	0
-3Vdc	0	1	0	1	0	1	1	0
-4Vdc	0	1	1	0	0	1	1	0

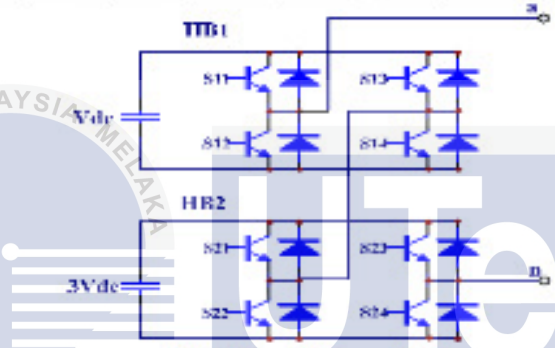

Fig. 1 Trinary DC source MLI.

It is compared with the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H-bridge, and cascaded transformer based multilevel inverter. In the case of diode-clamped, a large number of clamping diodes are a severe drawback. And a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated CML looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF (variable frequency) control scheme because of the saturation of transformer.

III. SWITCHING SIGNAL GENERATION

Switching signal generation for proposed multilevel inverter is generated using embedded controller. Fig 2-9 shows the gating pattern generated using embedded controller.PWM signals are generated using embedded m-file, which significantly reduces the switching stress and it makes the system reliable.

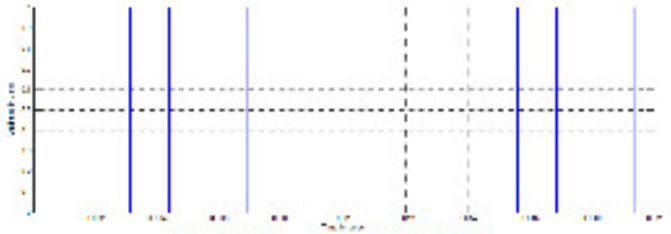

Fig 2: Gating pattern of Switch S11

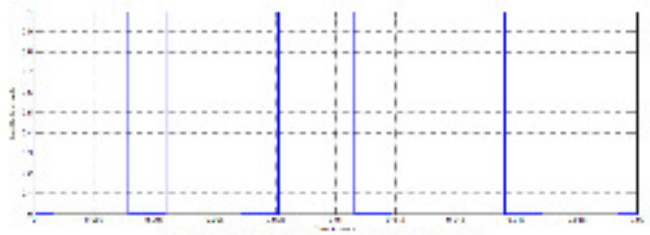

Fig 3: Gating pattern of Switch S12

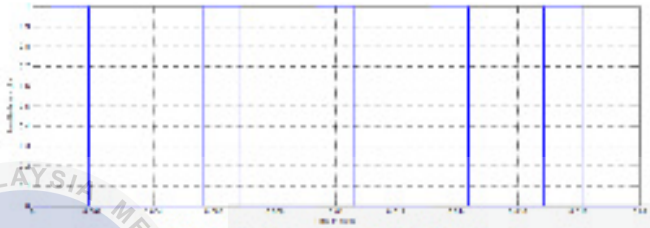

Fig 4: Gating pattern of Switch S13

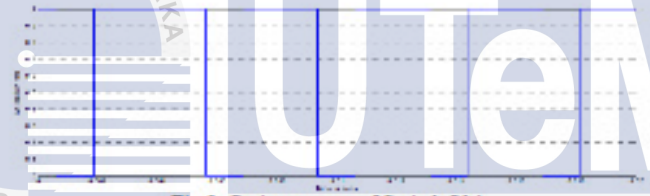

Fig 5: Gating pattern of Switch S14

Fig 6: Gating pattern of Switch S21

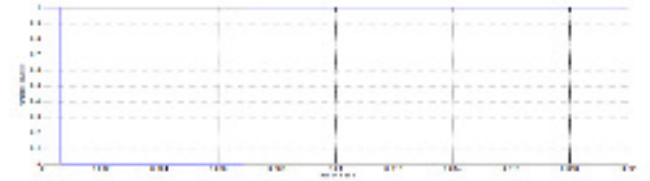

Fig 7: Gating pattern of SwitchS22

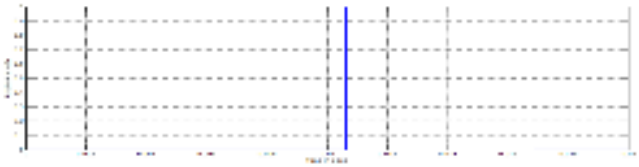

Fig 8: Gating pattern of Switch S23

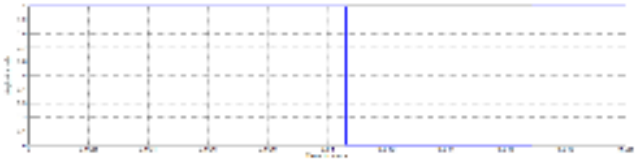

Fig 9: Gating pattern of Switch S24

IV. SIMULATIONS AND RESULTS

We are performed computer-aided simulations to prove availability of the proposed multilevel inverter. The simulations are implemented using Mat lab and it was considered to a pure resistive load. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently, the final output voltage becomes the sum of terminal voltage of H-bridge modules. Fig.13 shows the FFT plot for nine level inverter. We can notice that the lower inverter generates a fundamental output voltage of three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Consequently the final output voltage becomes the sum of output voltage of upper and lower H bridge modules. The following parameter values are used for simulation: V_{dc} =25V, R (load) = 100 ohms

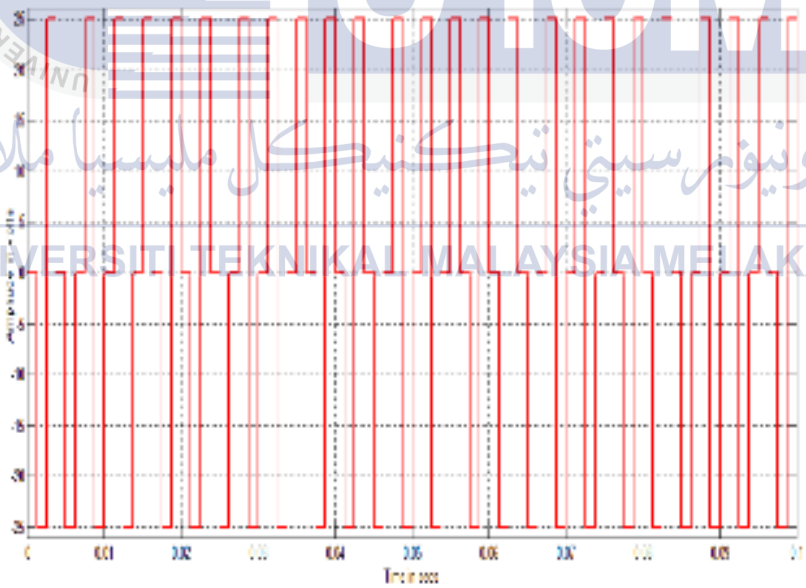

Fig 10: Upper inverter terminal voltage

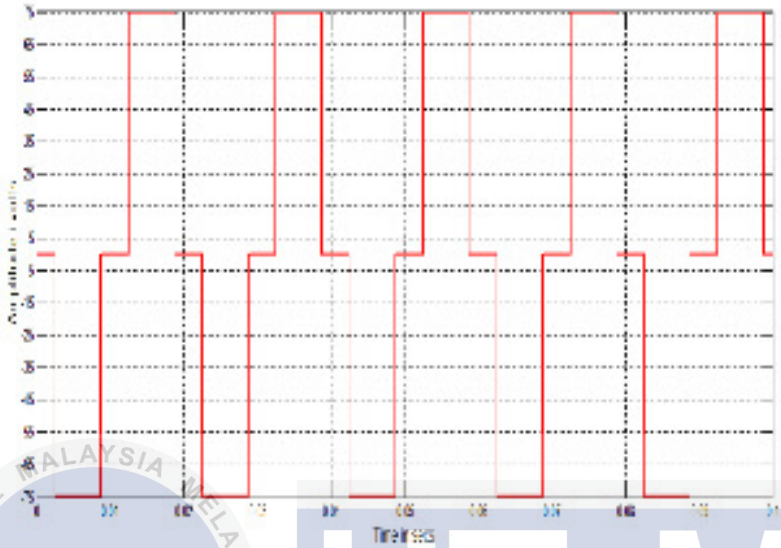

Fig 11: Lower inverter terminal voltage

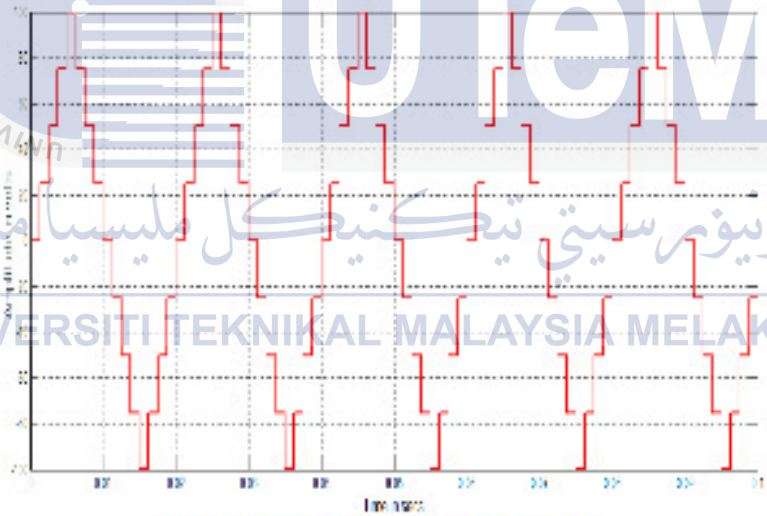

Fig 12: Nine level output voltage of Trinary MLI

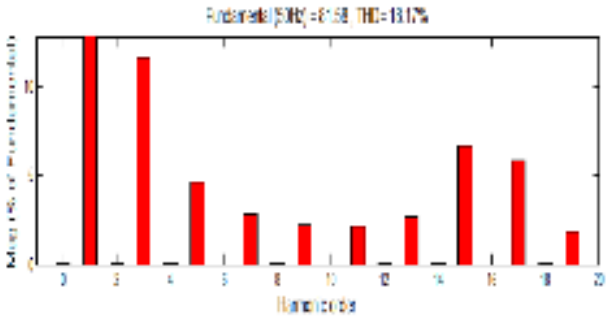

Fig 13: FFT plot for nine level output voltage

V. Conclusion

It proposed a cascaded H-bridge multilevel inverter employing Trinary DC sources to obtain a large number of output voltage levels with minimum devices. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. In this paper embedded switching scheme is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches and switching losses. It is observed that proposed topology produce THD of 18.17% .This proposed system eliminates the complexity of generating gate signals when the stages are added.

Valuable and presentable merits of the proposed approach are summarized as

(1) Economical circuit configuration to produce multilevel outputs by using Trinary input sources.

(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic.

(3) Little transition loss of switches due to low switching frequency and reduced EMI; it is suitable for high voltage applications.

References

[1] L. G. Franquelo, J. Rodriguez, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converter arrives," *IEEE Ind. Electron. Magazine*,pp. 28-39, 2008.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*,vol. 49, no. 4, pp. 724-738, Aug. 2002.

[3] J. S. Lai, and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509-517,May/June, 1996.

[4] M. H. Rashid, Power Electronics Handbook, Academic Press, 2001, pp.539-562.

[5] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Electron.*, vol.35, pp.36-44, 1999.

[6] F. S. Kang, S. J. Park, M. H. Lee, C. U. Kim, "An efficient multilevel synthesis approach and its application to a 27-level inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1600-1606, 2005.

[7] F. S. Kang, S. J. Park, C. U. Kim, T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Conversion*, vol. 20, no. 4, pp. 906-915, 2005.

[8] F.S.Kang, "A modified cascade-transformer-based multilevel inverter and its efficient switching function," *Electric Power Systems Research* ,vol. 79, pp. 1648-1654, 2009.