THE DEVELOPMENT OF PEAK CURRENT MODE CONTROL OF BUCK CONVERTER

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ABSTRACT

One of the reasons why DC-DC converter is widely used in industry nowadays is due to important of stable voltage or regulated voltage because the purpose of DC-DC converter is to stabilize the voltage. The step-down converter or buck converter will produce the output voltage less than the input voltage. As generally, the control topology that commonly used is voltage-mode control and current-mode control. In this project, the control method used is current-mode control of buck converter because this control mode is more accurate than voltage-mode control. The current-mode control is more accurate because it has better response. Current-mode control has better response because in current-mode control the sensor has sense change in load current directly so voltage error amplifier does no need to react and make a correction before producing the control voltage. The main objective and scope of the project is to design peak current-mode control of buck converter. This project also will study on this buck converter peak current-mode control and then it will be simulated using Pspice software. The project is conducted under several phases. Phase 1 is the introduction and understanding about current-mode control with simulation and modelling mathematical equation. Phase 2 is about understanding voltage- mode control with simulation. The comparison will be made between the current-mode control and voltage-mode control and the validation of simulation result is in Phase 3. The last phase is analyzing the result and makes certain conclusion based on the findings. In addition, other control topologies are also compared like the hysteresis controller. Even though hysteresis is advance and complex, this project just put more focus on current-mode control. As a conclusion, the current-mode control is better than voltage-mode control in term of voltage ripple and inductance current ripple.

ABSTRAK

Salah satu sebab mengapa DC -DC penukar digunakan secara meluas dalam industri pada masa kini adalah kerana pentingnya voltan yang stabil atau voltan terkawal bertujuan untuk DC -DC penukar menstabilkan voltan. Penukar langkah-turun (step-down converter) atau penukar buck akan menghasilkan voltan keluaran yang nilainya kurang daripada nilai voltan masukkan. Secara lazimnya , topologi kawalan yang biasa digunakan ialah kawalan voltan mod dan kawalan arus mod. Dalam projek ini , kaedah kawalan yang digunakan adalah kawalan semasa mod penukar buck kerana mod kawalan ini adalah lebih tepat nilai simulasinya berbanding kawalan voltan mod. Kawalan semasa mod adalah lebih baik dan tepat kerana ia mempunyai tindak balas yang lebih baik. Kawalan semasa mod mempunyai tindak balas lebih baik kerana dalam kawalan semasa mod sensor mempunyai perubahan rasa beban semasa terus jadi ralat voltan penguat tidak ada keperluan untuk bertindak balas dan membuat pembetulan sebelum menghasilkan voltan kawalan. Objektif utama dan skop projek ini adalah untuk mereka-bentuk puncak kawalan semasa mod penukar buck . Projek ini juga akan mengkaji mengenai penukar buck puncak kawalan semasa mod dan kemudian ia akan simulasi menggunakan perisian Pspice. Projek ini dijalankan di bawah beberapa fasa . Fasa 1 adalah pengenalan dan pemahaman mengenai kawalan semasa mod dengan simulasi dan pemodelan persamaan matematik . Fasa 2 adalah mengenai pemahaman kawalan voltan mod dengan simulasi. Perbandingan akan dibuat antara kawalan semasa mod dan kawalan voltan mod dan pengesahan keputusan simulasi adalah dalam Fasa 3. Fasa terakhir adalah menganalisis keputusan dan membuat kesimpulan tertentu berdasarkan dapatan kajian. Di samping itu, topologi kawalan lain juga seperto topologi histeresis juga turut sama dibuat perbandingan . Walaupun histerisis adalah lebih moden dan kompleks , projek ini hanya meletakkan tumpuan lebih kepada kawalan semasa mod. Kesimpulannya, kawalan semasa mod adalah lebih baik daripada kawalan voltan mod dari segi riak voltan dan riak semasa aruhan .

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CHAPTER 1

INTRODUCTION

This chapter describes the project background, problem statements, project objectives and project scope. In this project background, it will brief the description of the buck converter, peak current-mode control and voltage-mode control of buck converter as well as the project objectives and project scopes.

1.1 Project Background

The switched mode dc-dc converters are widely used to provide power processing for many applications because of the switched mode dc-dc converters are able to convert one level of electrical voltage into another level by switching action that some of simplest power electronic circuits. For dc-dc converter the main objectives are stability, zero steady-state error, specifies transient response to step change in reference and step change in disturbance inputs which are load and input voltage. There have several dc-dc converter switching controller topologies named as current-mode control and voltage-mode control. Every topology has some advantages and disadvantages, surely the simple, excellent performances under any condition and low cost structure of controller will be chosen.

The main idea of this report is to develop peak current-mode control of buck converter. Current-mode control has a fast response and divided to two types of control mode which are peak current-mode control and average current mode control. Average mode-current control is

better than peak current-mode control in term of accuracy which average current-mode control more accurate. In this project, peak current-mode control will be chosen because of low cost and simple circuit design. To make the controller become more stable, type II compensator has been chosen in circuit structure. To enhance the research, by in the end of project peak current-mode control will be compared with voltage-mode control of buck converter in term of output voltage ripple and inductance output current ripple. Simulation of circuit will be done by using Pspice simulation software.

1.2 Problem Statement

DC –DC converter switching controller consists of many control topologies to generate switching signal. Some of the switching signals incudes of voltage-mode control or current-mode control. Current-mode control has better respond than voltage-mode control because has sense change in load current directly so that voltage error amplifier does no need to react and make a correction. Meanwhile voltage-mode control has slow response because a load current change on the output voltage so that voltage error amplifier can react and make correction. Sensing of voltage-mode control is poorer compare to sensing of current-mode control because in voltage-mode control is only containing single feedback loop from output voltage which is outer loop. This also called single sensing. Current-mode control have double sensing and double loop called outer loop which is slower compare to inner loop. Inner loop is controlled by inductor current in current-mode control which does not exist in voltage-mode control Current-mode control can be divided into two which are peak current-mode control and average current-mode control. Peak current-mode control is easy to design and has low cost implementation compare to the average current-mode control.

1.3 Objectives

The objectives of the projects are:

i. To design peak current-mode control of buck converter
ii. To do the simulation for peak current-mode control of buck converter circuit using Pspice software
iii. To do comparison of performance between peak current-mode control and voltage-mode control in term of voltage ripple and inductance current ripple.

1.4 Scope

i. In this project, the power stage converter that will be designed is buck converter circuit which the input will be 30V and the output is 15V. Controller mode that will be used for the buck converter circuit is peak current-mode.
ii. Type II compensator will be used as error amplifier for the circuit.
iii. The circuit is simulated by using Pspice software and its performance will be compared with voltage-mode control buck converter in terms of voltage ripple and inductance current ripple.

1.5 Report Outline

Chapter 1

This chapter will discuss and explain the background of the project with problem statements, objectives and also the scope. Peak current-mode control, voltage-mode control and Pspice software are the main essential in this project.

Chapter 2

This chapter will focus on literature review for those there parts that have been explain in Chapter 1. All the journals and books that have some attachment to this project are used as a reference to guide and help to completing this project. Each of this part is explained based on this finding.

Chapter 3

This chapter will discuss and explain about the methodology that has been used in order to complete this project. The project activity is to describe the flow of whole project as stated in the project flowcharting. The major part in this chapter which is the software simulation designed. The discussion will be focused on how to design and simulate in Pspice software of the buck converter, using current-mode and voltage-mode control. Another area is the compensator design through Matlab simulation software.

Chapter 4

Discuss about the result obtained and limitation of the project. All discussion are concentrating on the result and comparing with the simulation between current-mode control and voltage-mode control.

Chapter 5

This chapter will discuss about the conclusion of the development of the project. This chapter also discusses the recommendation for this system for future development or modification and discuss about costing and commercialization.

CHAPTER 2

LITERATURE REVIEW

This chapter describes all of the related theories and literature reviews of the buck converter, peak current-mode control and voltage-mode control of the buck converter. This chapter also discuss about previous problem of the current-mode control and voltage-mode control of buck converter.

2.1 Theory and Basic Principle

2.1.1 DC-DC Converter

DC-DC converter is one of electronic devices used to change DC electrical power efficiency from one voltage level to another. DC-DC converter is need because it is not same like AC which DC cannot simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer [1]. Almost DC-DC converters have same function as transformer that essentially just change the input energy into a different impedance level. The output power all comes from the input and there is no energy manufactured inside the

converter no matter what the output voltage level. The converter often includes one or several transistor in order to control the output voltage. The transistor is not operated in its linear interval because the converters are desirably made with low losses. When time the transistor is off, the current through it is low and the power loss is also low. Resistors are avoided in the converters when to obtain low losses.

Capacitors and inductors are used since it ideally does not have any losses. Figure 2.1 shows the DC-DC converter blocks diagram. To step up or stepped down the voltage, the non-isolating type of converter is generally used by a relatively small ration and there is no problem with the output and input having no dielectric isolation. There are five main types of converter in this non-isolating group usually called the buck, boost, buck-boost, and Cuk and charge-pump converters. The buck converter is used for voltage step-down or reduction while the boost converter is used for voltage step-up. The Cuk and Buck-Boost converters can be used for either step-up or step-down but are essentially voltage polarity reverses or inverters as well. The charge-pump converter is used for either voltage inversion or voltage step-up but only in relatively low power applications [1].

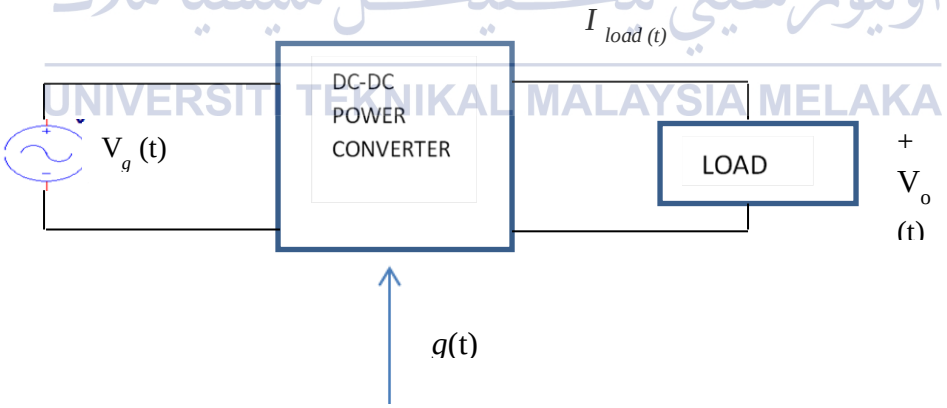


Figure 2.1: DC-DC Converter Block Diagram [1]

2.1.1.1 DC-DC Converter- Buck Converter

The popular non-isolated power stage topology which is buck converter, sometimes called a step-down power stage. Buck power stage is suitable for any design because the required output is always less than the input voltage [2]. The input current for a buck power stage is pulsating or discontinuous because the power switch current that pulses from zero input output every switching cycle. The output current for a buck power stage is non-pulsating or continuous because the output current is supplied by the output inductor or capacitor combination. Figure 2.2 shows a simplified schematic of the buck power stage. Capacitor and inductor, L makes up the effective output filter. The inductor dc resistance and the capacitor equivalent series resistance are included in the analysis. Resistor represents the load seen by the power supply output. The diode is usually called the freewheeling diode or catch diode.

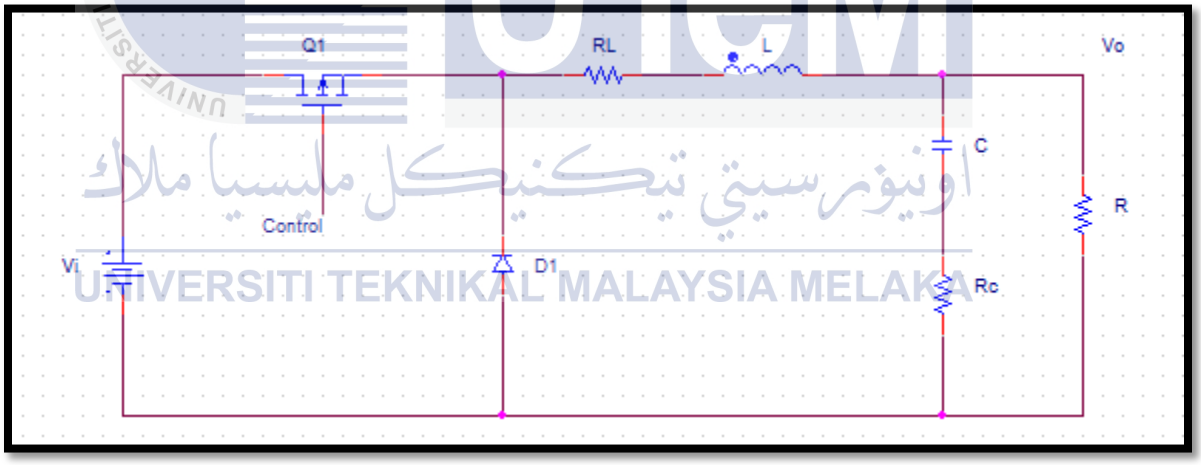


Figure 2.2: Buck Power Stage Schematic [2]

A power stage can operate in discontinuous or continuous inductor current mode [2]. Current flows continuously in the inductor during the entire switching cycle in steady-state operation in continuous inductor current mode. While in discontinuous inductor current mode, inductor current is zero for a portion of the switching cycle. This cycle starts at zero, reaches peak value and return to zero during each switching cycle. It is desirable for a power stage to

stay in only one mode over its expected operating conditions because the power stage frequency response changes significantly between the two modes of operation.

2.1.1.2 Operation of Buck Converter

Buck converter is able to produce a dc output voltage smaller in magnitude than the dc input voltage level with minimal ripple. It is a switched-mode power supply that uses two switches like a diode and transistor as well as a capacitor and inductor. The basic circuit of buck converter shows in Figure 2.3 [3].

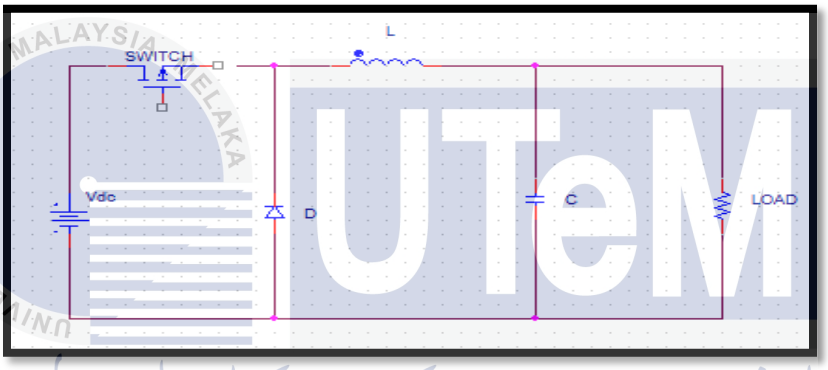
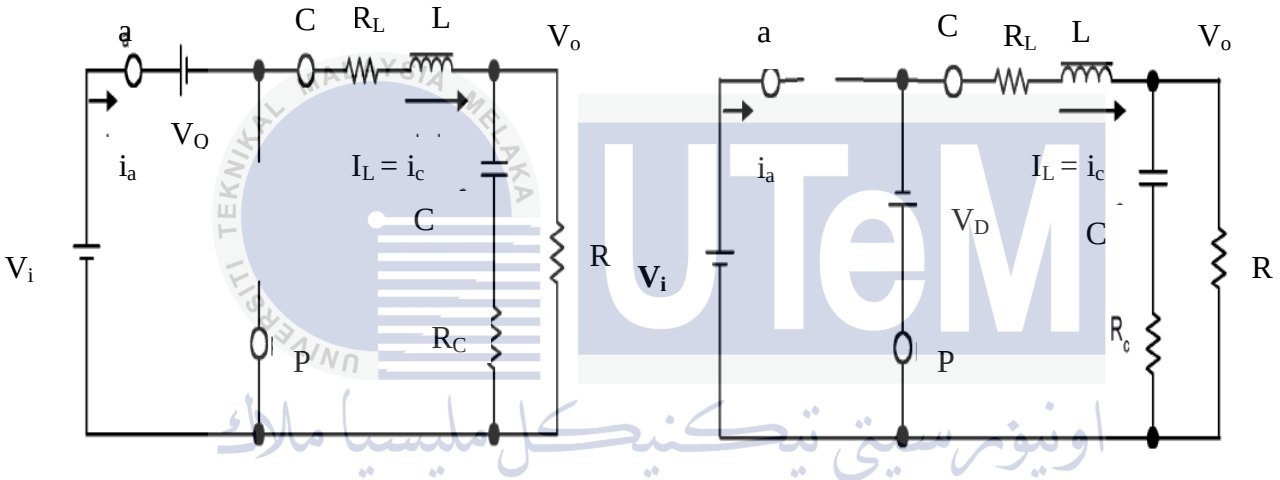


Figure 2.3: Basic circuit of Buck Converter [3]

Current in the circuit is zero at early because of the switch in the circuit in open position. When switch is closed, the current begin increase. During that time the inductor doing its job by storing energy in form of magnetic field, at the same time the inductor decreasing the voltage same as net voltage seen by the load. Then the switch is opened before the voltage drop to zero because of inductor allowed all of the current to pass through. At this time the inductor will be acting like a voltage source in order to maintain the current and also to provide the same net voltage to the load when the input source is not connected into the circuit and current will drop. If the switch is closed again before the inductor fully discharges, the load will not see a non-zero voltage [3].

The operation of buck converter has two modes which is discontinuous and continuous mode. The buck power stage assumes two states per switching cycle in continuous current mode. In the ON state, Q1 is on and D1 is off. In the OFF state, Q1 is off and D1 is on. Each of the two states of buck converter can be representing in a simple linear circuit where the switches in the circuit are replaced by the equivalent circuit during each state. Figure 2.4 shows the linear circuit diagram for each of the two states and Figure 2.5 shows the continuous current mode buck power stage waveforms in terms of voltage and current [3].



2.4 a: ON state of Buck converter in Continuous mode operation [3]

2.4 b: OFF state of Buck converter in Continuous mode operation [3]

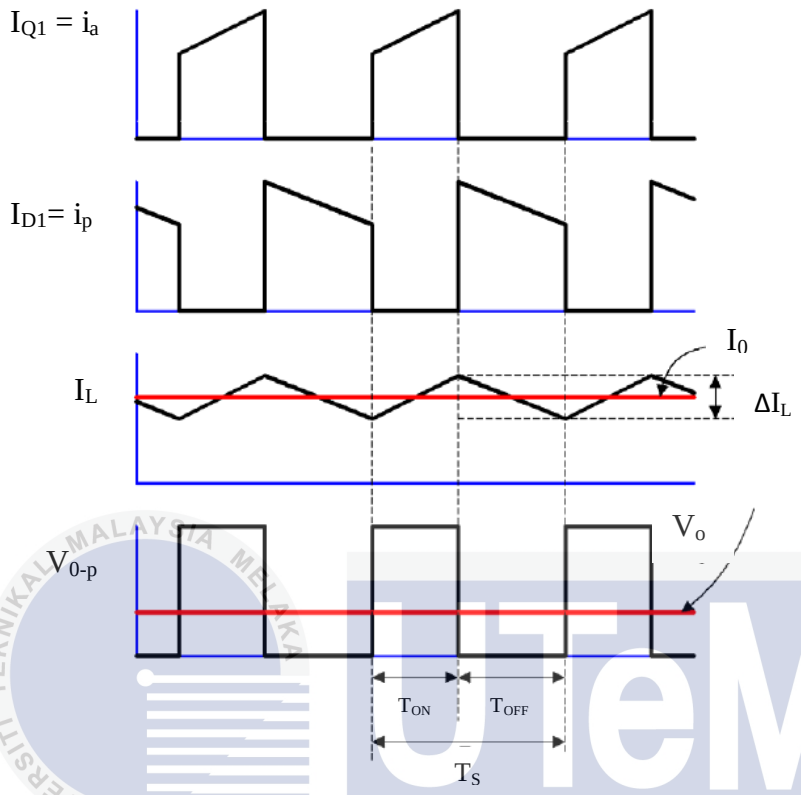


Figure 2.5: Continuous current mode buck power stage waveforms in terms of voltage and current [3]

It occurs for light loads or low operating frequencies where the inductor current eventually hits zero during the switch open state in discontinuous mode. To prevent backward current flow, the diode will open. The small capacitances of the diode and MOSFET, acting in parallel with each other as a net parasitic capacitance, interact with inductor to produce an oscillation. The output capacitor is in series with the net parasitics capacitance but the capacitor is so large. When the capacitor is so large, it can be ignored in the oscillation phenomenon. Figure 2.6 shows the circuit of discontinuous mode of buck power stage converter and Figure 2.7 shows the discontinuous mode buck power stage waveforms in terms of voltage and current [3].

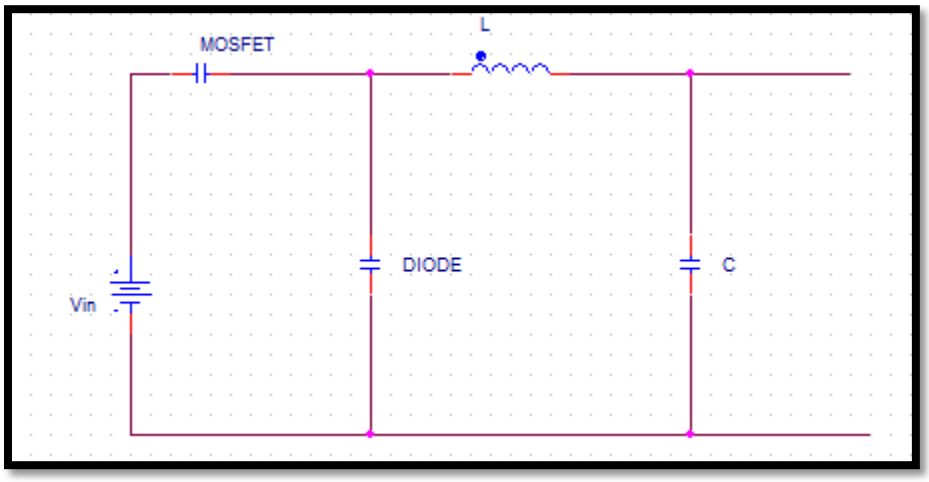


Figure 2.6: Circuit of discontinuous mode of buck power stage converter [3]

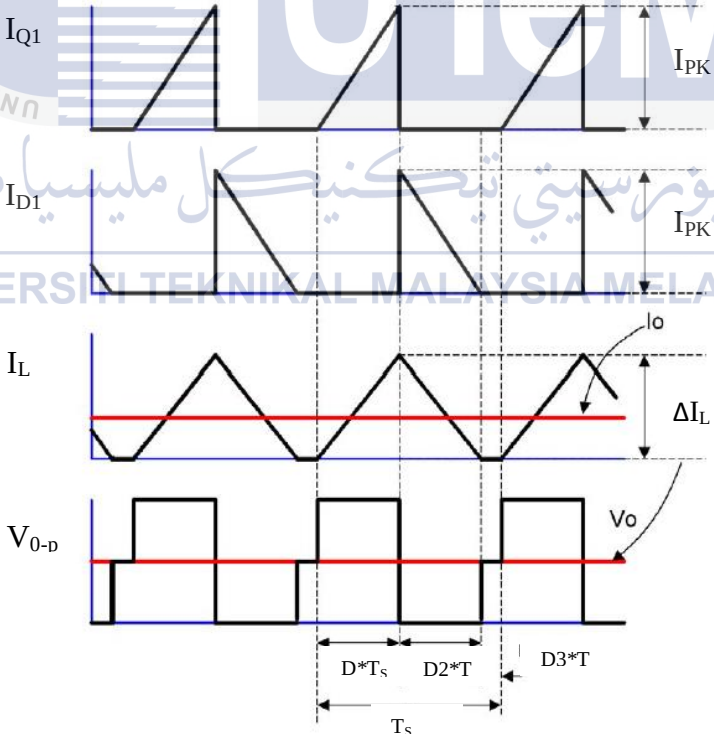


Figure 2.7: The discontinuous mode buck power stage waveforms in terms of voltage and current [3]

2.1.1.3 Design of Buck Converter

A few considerations must be noted in order to design buck converter. Most buck converters are designed for continuous-current operation. When the switching frequency increases, the minimum size of the inductor to produce continuous current and the minimum size of capacitor to limit output ripple both decrease. At the same time, high switching frequencies are desirable to reduce the size of both the inductor and the capacitor. The tradeoff for high switching frequencies is increased power loss in the switches. Increased power loss in the switches means that heat is produced. This heat produced will decrease the converter's efficiency and may require a large heat sink, offsetting the reduction in size of the inductor and capacitor. Typical switching frequencies need to avoid audio noise. For high-current and low-voltage applications, the synchronous rectification is preferred over using a diode for the second switch.

The voltage across the conducting MOSFET will be much less than that across a diode and resulting in lowers losses. To ensure continuous current operation, the inductor value should be larger than minimum inductor. The inductor wire must be rated at the rms current and the core should not saturate for peak inductor current. To the design specification to withstand peak output voltage and to carry the required rms current, the capacitor must be selected to limit the output ripple. The diode and switch must withstand maximum voltage stress when off and maximum current when on. The temperature ratings must not be exceeding often requiring a heat sink. Assuming ideal switches and an ideal inductor in the initial design is usually reasonable. In addition, the equivalent series resistance (ESR) of the capacitor should be included because it typically gives a more significant output voltage ripple than the ideal device and greatly influences the choice of capacitor size [4].

Important part in design this converter is by specify the input and output voltage of converter. Then find the duty ratio, D by using Equation 2.1 [5]

$$V_O = V_S D \tag{2.1}$$

The next step is finding the average inductor current which is same with average current in the load resistor as Equation 2.2 [5]

$$I_L = I_R = \frac{Vo}{R} \tag{2.2}$$

Since the value of inductor current is known at Equation 2.2, the minimum and maximum values of inductor current are calculated as

$$I_{MAX} = I_L + \frac{\Delta i_L}{2} = \frac{Vo}{R} + \frac{1}{2}\left[\frac{Vo}{L}(1\text{-}D)\ T\right] \tag{2.3}$$

$$I_{MIN} = I_L - \frac{\Delta i_L}{2} = \frac{Vo}{R} - \frac{1}{2}\left[\frac{Vo}{L}(1\text{-}D)\ T\right] \tag{2.4}$$

The next step in design buck converter is by calculating the minimum inductance that required for continuous current.

$$L_{MIN} = \frac{(1-D)R}{2f} \tag{2.5}$$

The value of inductance must greater than L_{MIN} because to make sure that continuous current occurred in practical. Value of inductor current must be 25% of value minimum inductor. Assuming all the inductor ripple current flows through output capacitor and equivalent series resistor for output capacitor is zero and the value of capacitor can be calculated by Equation 2.6 [5]

$$C = \frac{(1-D)}{8L\left(\frac{\Delta Vo}{Vo}\right)f^2} \tag{2.6}$$

2.1.2 Voltage-Mode Control

Voltage-mode control is also known as the voltage feedback arrangement when applied to DC-DC converter. Voltage mode control is an easy way to design and implement and has good element to disturbance at the references input and it only contain single feedback loop from output voltage. Figure 2.8 shows the buck converter power and control stage [6].

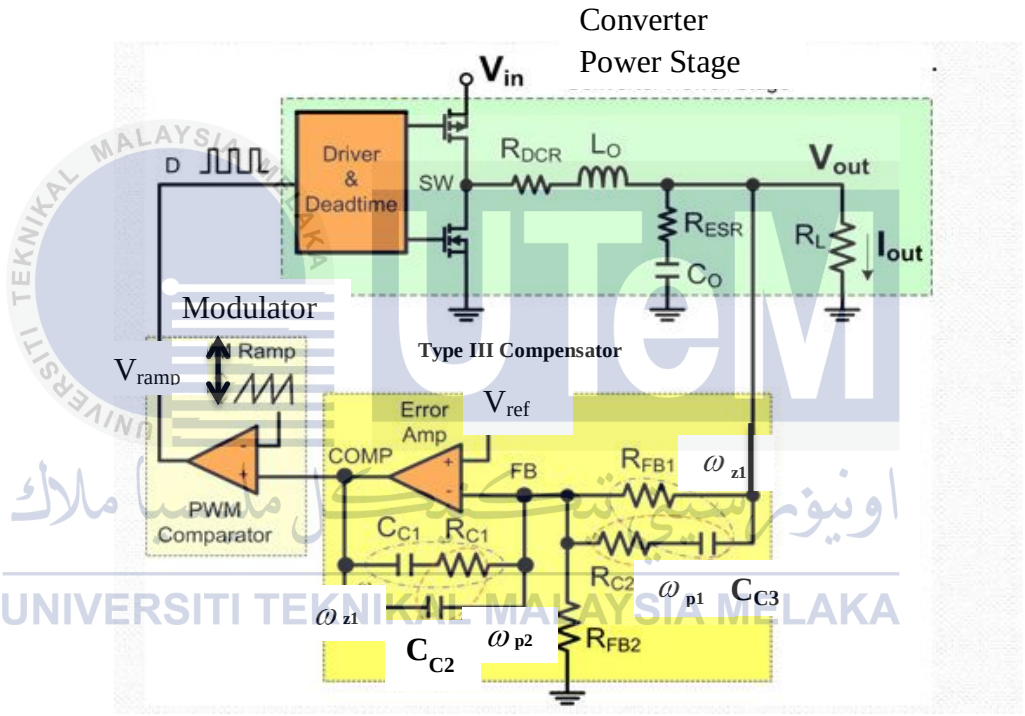


Figure 2.8: The Buck Converter Power and Control Stage [6]

Non-ideal power train components are shown with parasitics such as capacitor equivalent series resistance, R_{ESR} denoted explicitly and inductor DC resistance, R_{DCR}. Second order parasitics such as interconnection impedances and capacitor equivalent series inductance (ESL) are not represented. The high side switch is driven by a PWM signal for time t_{on} in each switching period of duration T_S. The duty cycle ration, D is given by Equation 2.7 [6]

$$D = \frac{t_{on}}{T_S} \approx \frac{V_{out}}{V_{in}} \quad (2.7)$$

The low side switch is driven complementarily with duty cycle D'= 1-D. Both switches of voltage-mode operate at fixed switching frequency $f_s = 1/T_S$. The output filter consists of capacitor, C_o and inductor, L_o. A conventional operational amplifier type voltage error amplifier represents the epicenter of the control loop structure. The divided down output voltage at the error amplifier inverting input is usually termed the feedback node is compared to a fixed reference voltage and a compensated error signal is generated at the compensation node .This error signal is compared to a saw-tooth ramp voltage at the pulse width modulator comparator like an increase in compensation node leads to a commensurate increase in duty cycle command for the power stage. [7].

2.1.3 Current-Mode Control

There are three things to consider which current-mode operation, modulator gain is and slope compensation in current-mode control. Current-mode operation is an ideal current mode converter is only depending on the average or dc inductor current. The inner current loop turns the inductor into a voltage-controlled current source and effectively removing the inductor from the outer voltage control loop at dc and low frequency.

Modulator gain is dependent on the effective slope of the ramp presented to the modulating comparator input. Each modulating gain operating mode will have a unique characteristic equation for the modulator gain. Slope compensation is about the requirement for slope compensation which is dependent on the relationship of the average current to the value of current at the time when every sample is taken. In fixed-frequency operation, if the sampled current were equal to the average current, there would be no requirement for slope compensation.

The current-mode converter which uses peak, valley, average or sampled-and-hold can be categorized as secondary to the operation of current loop. As long as the dc current is sampled, current-mode operation will still maintained. The current-loop gain splits the complex-conjugate

pole of the output filter into two real poles and that the characteristic of the output filter is set by the capacitor and load resistor. Only when the impedance of the output inductor equals, so the current-loop gain does the inductor pole reappear at higher frequencies. Figure 2.9 shows the basic block diagram of current-mode control [8].

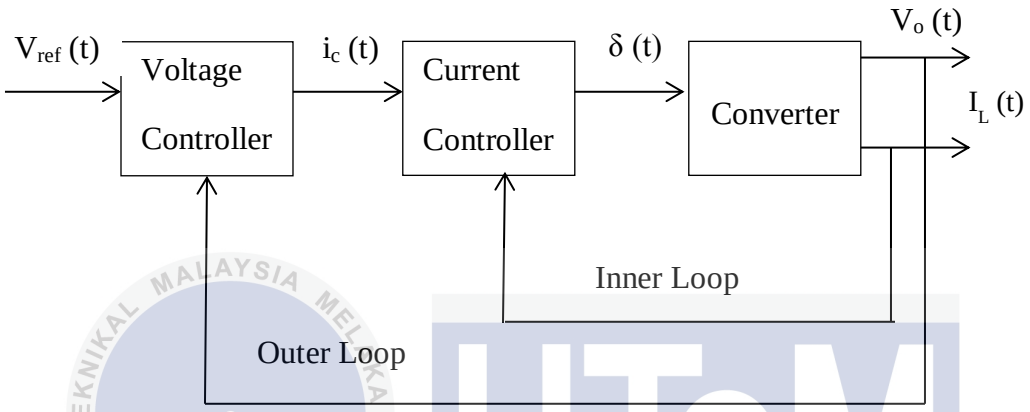


Figure 2.9: Block Diagram of Current-mode Control [8]

From Figure 2.9, there are two loops are used in current-mode control which are outer loop and inner loop. Inner loop controlled by the inductor current, i_L and the this inner loop is fast. Compared to inner loop and outer loop, outer loop slower and this loop are controlled by the output voltage. The most common type of current-mode control is peak current-mode control which is the peak inductor current is controlled. One of the famous control methods in DC-DC converters is peak current-mode control. The main idea behind control-mode current is that the inductor can be turned into a current source thus eliminating the dynamics of the inductor in the loop. The controller sets a current reference and a fast inner-loop following the reference cycle by cycle [8].

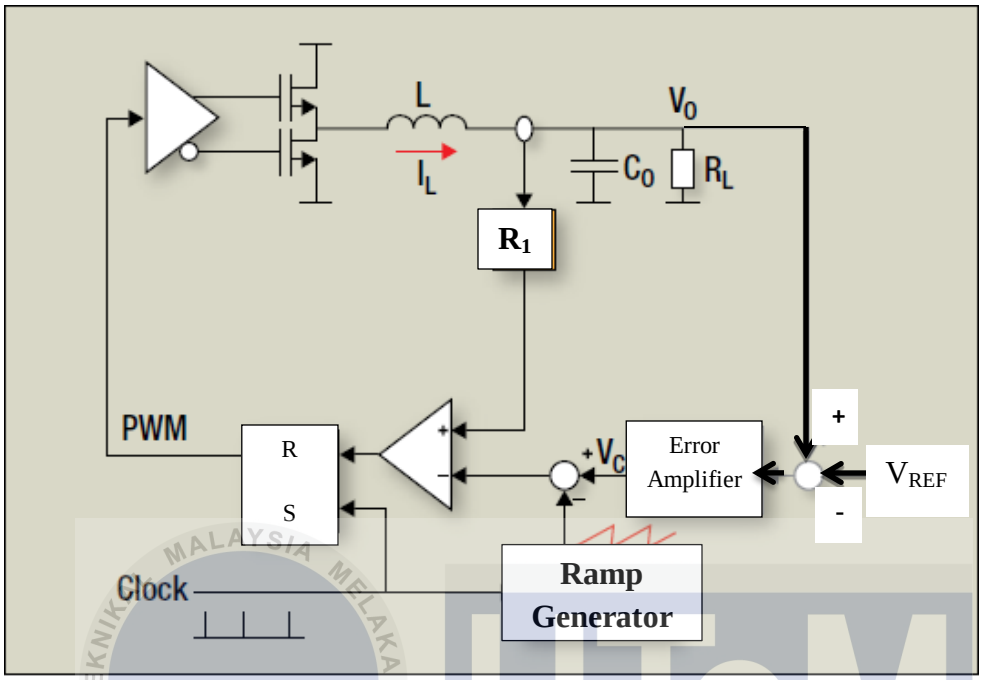


Figure 2.10: Peak Current-Mode Control with Buck Converter [8]

Figure 2.10 shows a typical implementation for a peak current-mode control with buck converter. There is an outer voltage loop with an error amplifier that compensates for the dynamic response of the output voltage. The current loop or inner loop is that provides tight control on the peak inductor current.

Equation transfer function of complete control-to-output for buck converter under peak current mode control is combination of three terms which are a high frequency transfer function (F_H (s)), a DC gain (H_{DC} (s)) and a power stage small signal model (H_B (s)). Equation 2.8 shows the transfer function of complete control-to-output for buck converter under peak current mode control [8].

$$H_c(s) = \frac{V_{out}}{V_{ERR}} = F_H(s) \times H_B(s) \times H_{DC}(s) \quad (2.8)$$

Equation 2.9 shows the equation of a high frequency transfer function of buck converter under peak current mode control.

$$F_H(s) = \frac{1}{1 + \frac{S}{\omega_N} + \frac{S^2}{\omega_N{}^2}} \tag{2.9}$$

Where $\omega_N = \pi F_S$ in rad/sec

Equation 2.10 shows the equation of the DC gain of buck converter under peak current mode control. [9]

$$H_{DC} = \frac{R_L}{R_i} x \frac{1}{1 + \frac{R_L T_S}{\pi L}} \tag{2.10}$$

Equation 2.11 shows the equation of small signal model of the buck converter power stage.

$$H_B = \frac{1 + \frac{S}{\omega_{ESR}}}{1 + \frac{S}{\omega_{OP}}} \tag{2.11}$$

Next equation is about pole equation, ω_{op} and zero equation, ω_{ESR} of the buck converter.

$$\omega_{OP} = \frac{1}{R_L C_O} + \frac{T_S}{\pi L C_O} \tag{2.12}$$

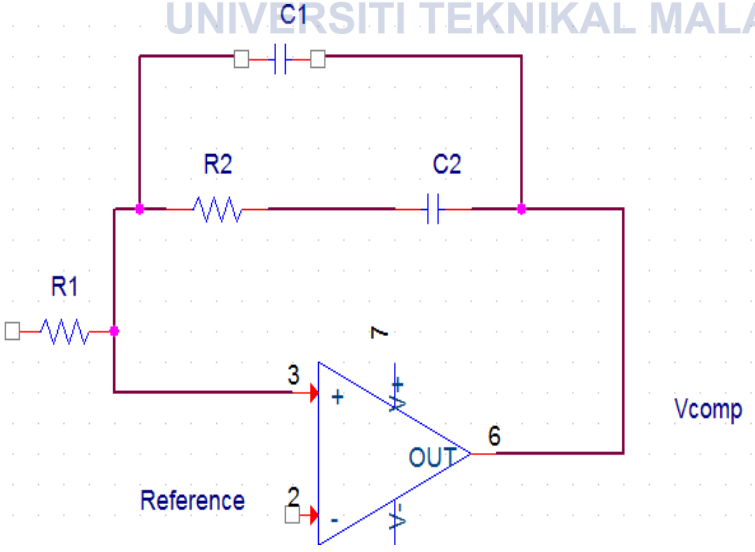
$$\omega_{ESR} = \frac{1}{R_{ESR}} \tag{2.13}$$

2.1.4 Compensator

Closing the control loop always the regulator is to adjust to load perturbations or changes in the input voltage which may adversely affect the output. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a type II and type III compensation network will properly compensate the system. The ideal Bode plot for the compensated system would be a gain that rolls off at a slope of -20dB/decade, crossing 0dB at the desired bandwidth and a phase margin greater than 45^{o} for all frequencies below the 0dB crossing. For synchronous and non-synchronous buck converter, the bandwidth should be between 20% to 30% value of the switching frequency [10].

2.1.4.1 Type II Compensator

The type II network always helps to shape the profile of the gain with respect to frequency and also gives a 90^{o} boost to shape. This boost is necessary to counteract the effects of the resonant output filter at the double pole. Figure 2.10 and 2.11 below shows a generic Type II compensation, its transfer function and asymptotic Bode plot [10].



Gain Type II Compensator:

$$\frac{1}{R_1 x C_1} \text{ X } \frac{(s+\frac{1}{R_2 x C_2})}{sx(s+\frac{C_1+C_2}{R_2 x C_1 x C_2})}$$

Figure 2.10: Type II Compensator Circuit and Transfer Function [10]

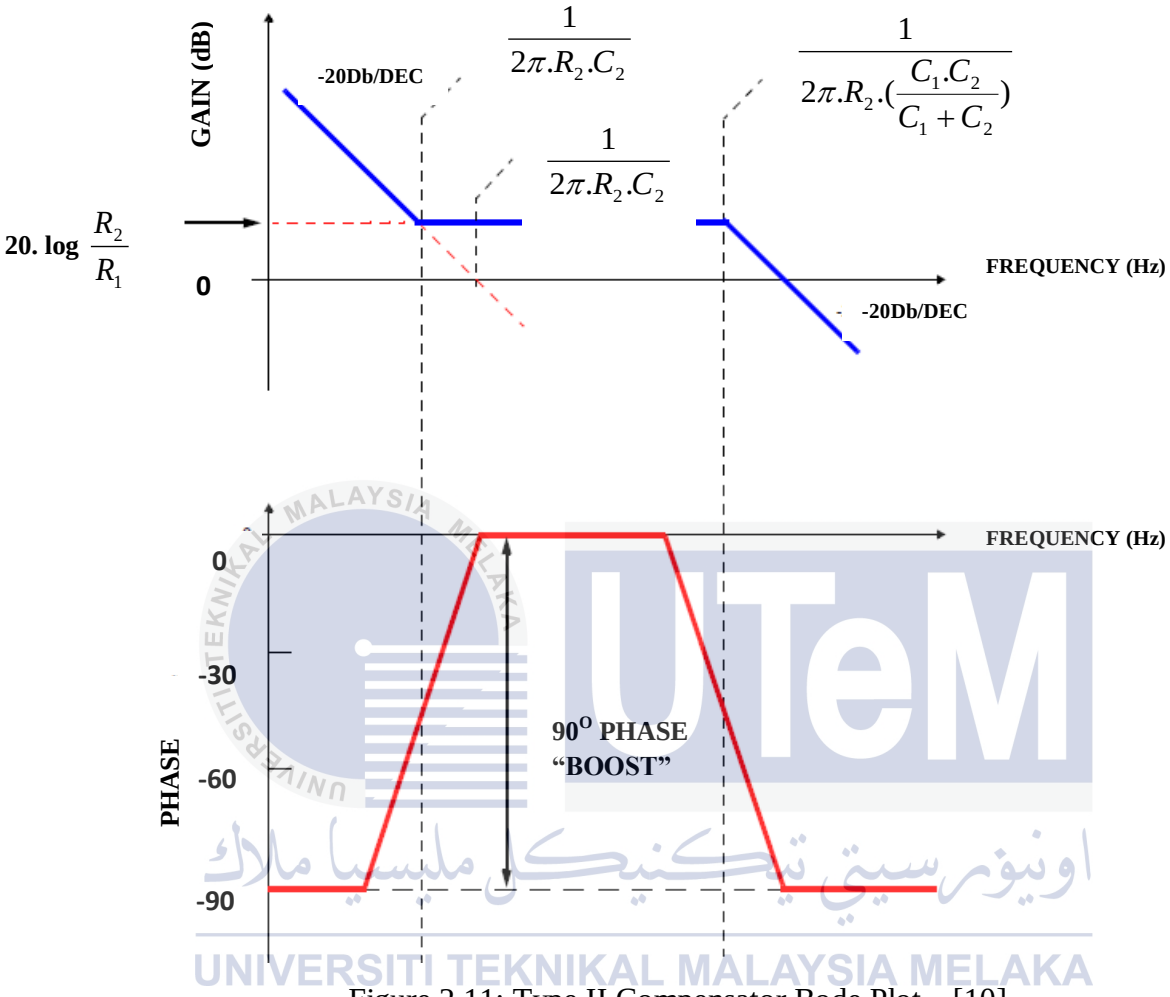
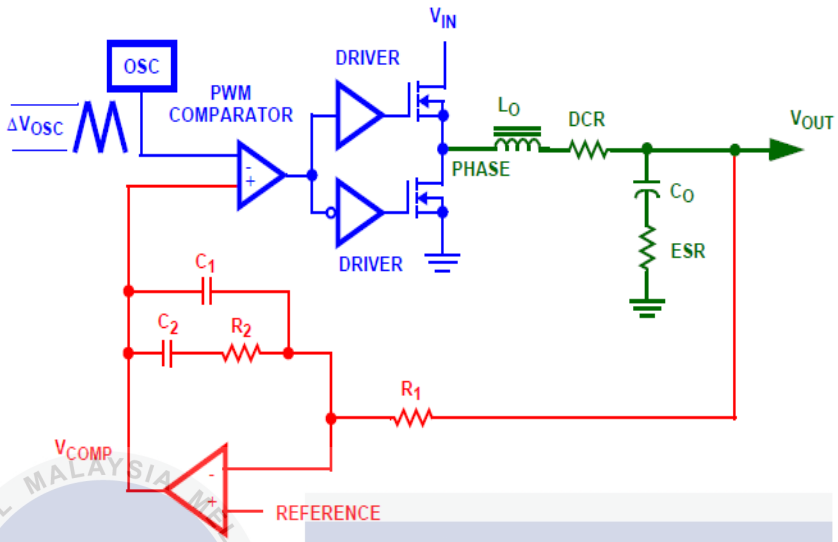


Figure 2.11: Type II Compensator Bode Plot [10]

If the output voltage of the regulator is not the reference voltage then a voltage programming resistor will be connected between the inverting input to the error amplifier and ground. This resistor is used to offset the output voltage to a level higher than the reference. This resistor if present has no effect on the compensation and can be ignored. Figure 2.12 below shows the closed loop system with a Type II compensation network and presents the closed loop transfer function [10].



Gain System:

$$\frac{1}{R_1.C_1} x \frac{(s+\frac{1}{R_2.C_2})}{(s+\frac{C_1+C_2}{R_2.C_1.C_2})} x \frac{V_{IN}}{\Delta V_{OSC}} x \frac{1+s.ESR.C_{OUT}}{1+s.(ESR+DCR).C_{OUT}+s^2.L_{OUT}.C_{OUT}}$$

Figure 2.12: Closed Loop System with Type II Network [10]

There are four guidelines that will help calculate the poles and zeroes and from those the component values for a Type II network which are choose value for R_1, then pick a gain. After that, calculate C_2 and last step is calculate C_1. Figure 2.13 below shows the asymptotic Bode gain plot and the actual gain and phase equations for the Type II compensated system. It is recommended that the actual gain and phase plots be generated through that the actual gain and phase plots be generated through the use of commercially available analytical software. The asymptotic plot of the gain and phase does not portray all the necessary information that is needed to determine the stability and bandwidth [10].

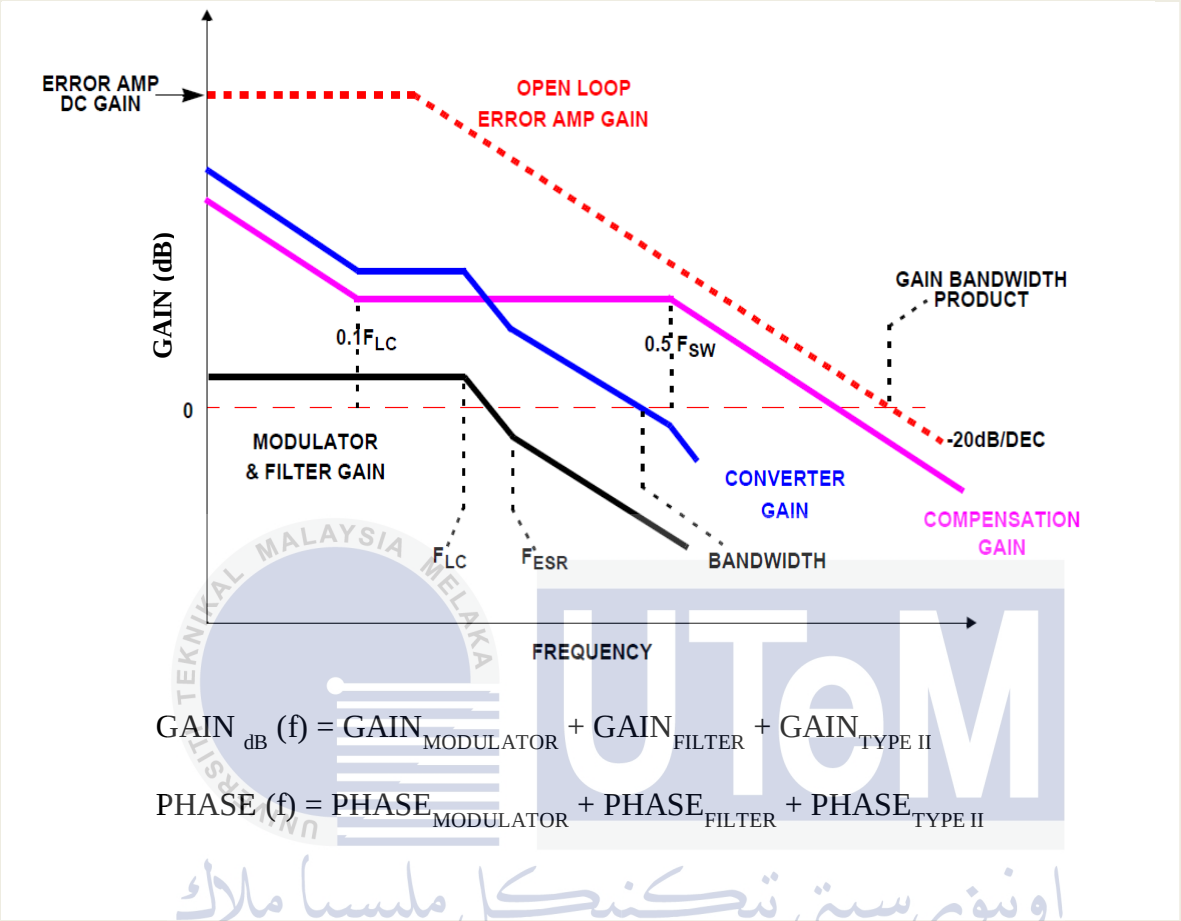
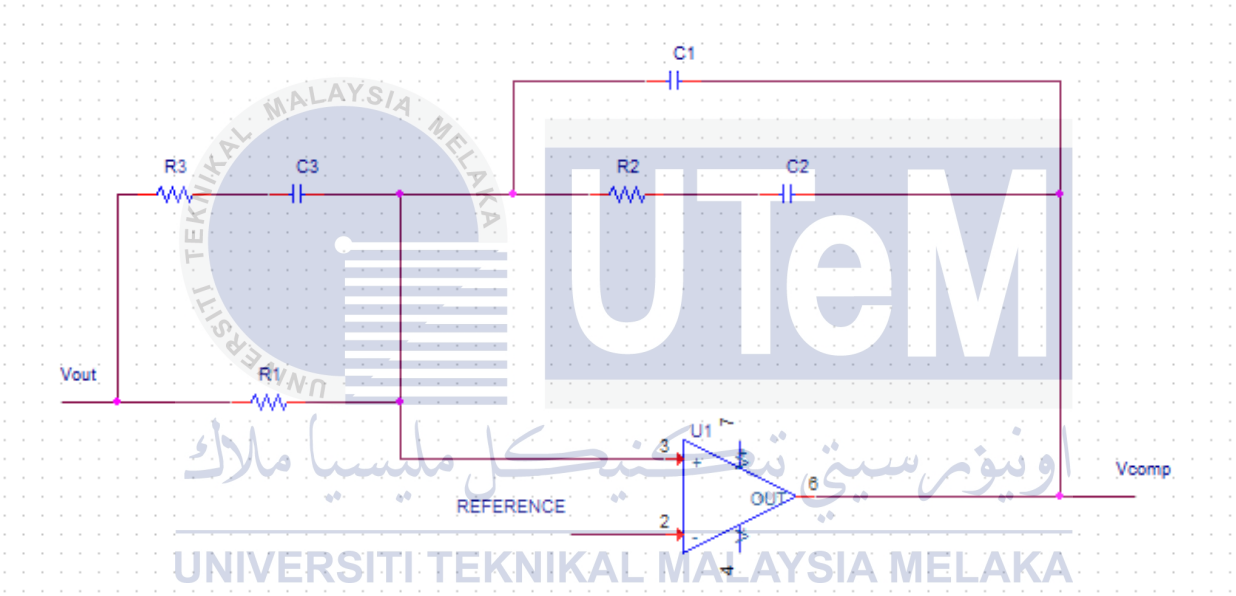


Figure 2.13: The Asymptotic Bode Gain Plot and the Actual Gain and Phase Equations for the Type II Compensated System [10]

The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. Once the phase plots and gain are generated and analyzed, the system may need to be changed somewhat in order adjust the bandwidth or phase margin. Adjust the location of the zero and or pole to modify the profile of the plots. If the phase margin proves too difficult to correct, then a Type III system will be needed [10].

2.1.4.2 Type III Compensator

The Type III network shapes the profile of the gain with respect to frequency in a similar fashion or pattern to the Type II network. The Type III network utilizes two zeroes to give a phase boost of 180^0. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole. Figure 2.14 and 2.15 below show a generic Type III compensation, its transfer function and asymptotic Bode plot [10].



Gain Type III Compensator:

$$\frac{R_1+R_3}{R_1..R_3.C_1} \text{X} \frac{(s+\frac{1}{R_2.C_2})X(s+\frac{1}{(R_1+R_3).C_3})}{sX(s+\frac{C_1+C_2}{R_2.C_1.C_2})X(s+\frac{1}{R_3.C_3})}$$

Figure 2.14: Generic Type III Compensation and Transfer Function [10]

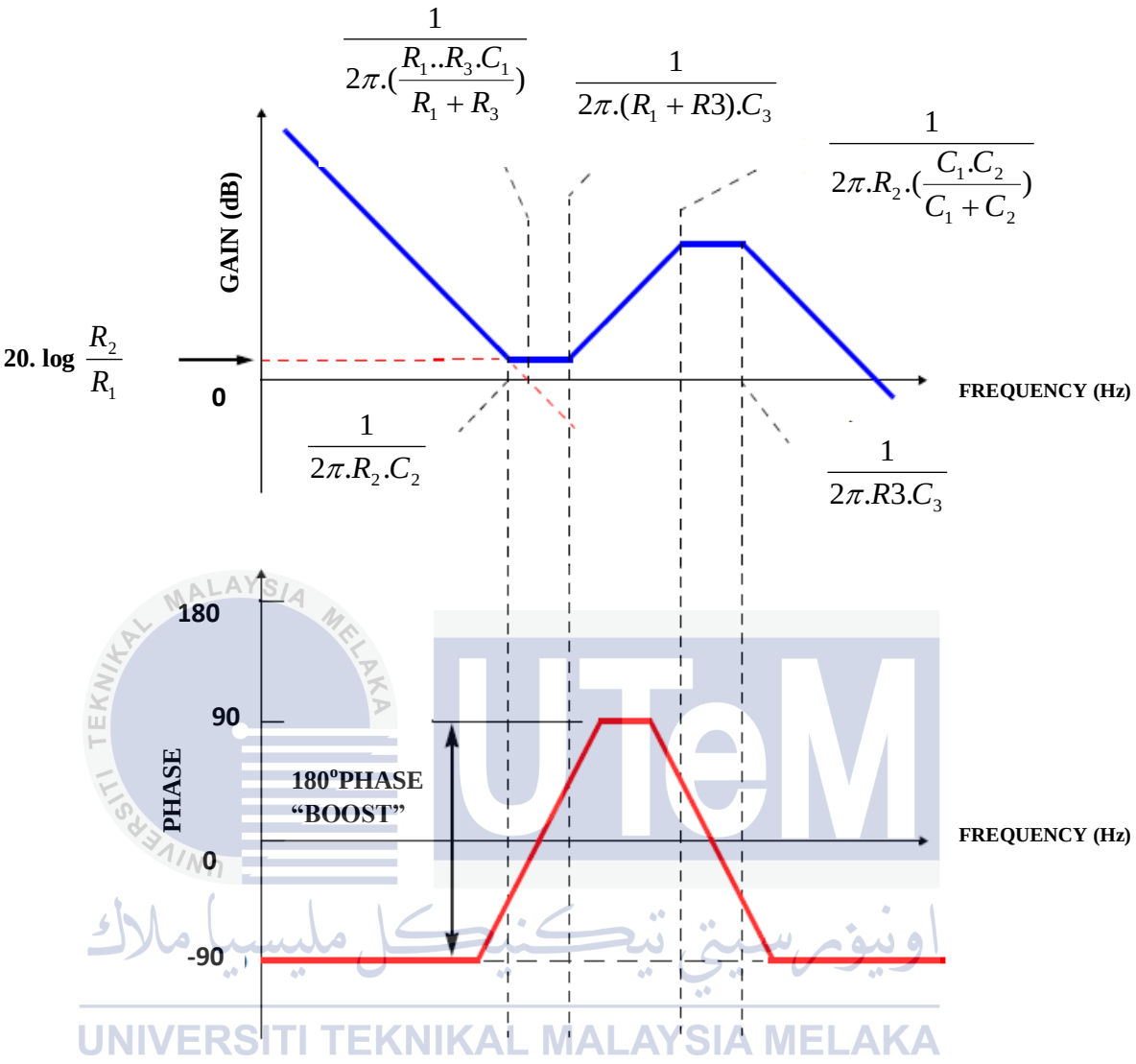
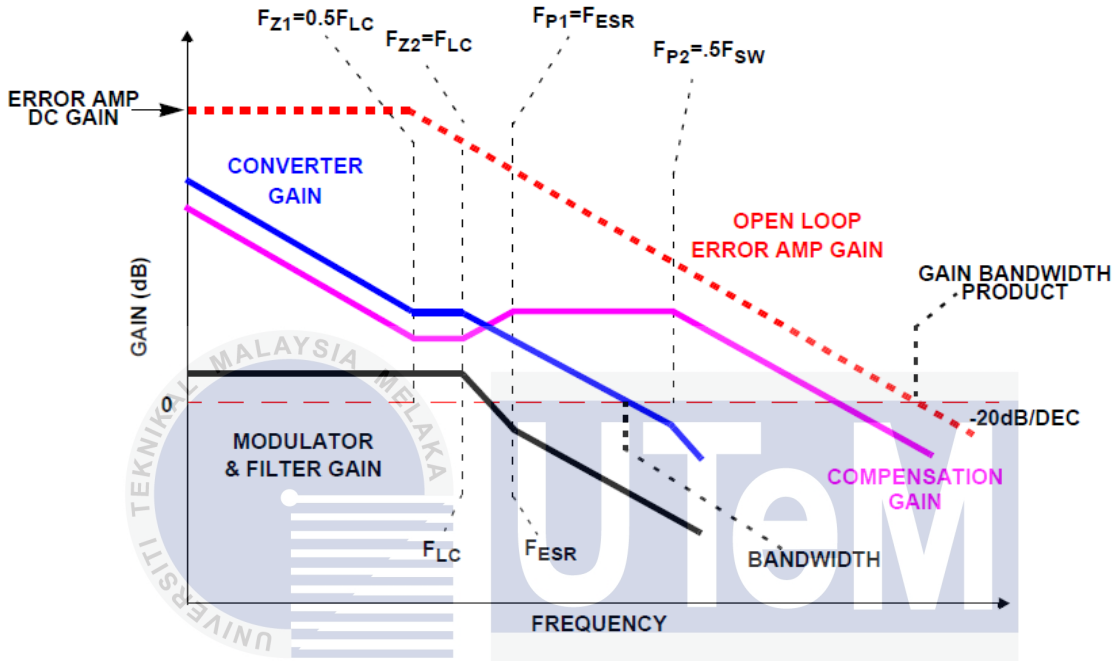


Figure 2.15: Type III Compensator Bode Plot [10]

As with the Type II compensation network, it is recommended that the actual gain and phase plots be generated through the use of a commercially available analytical software package that has the capability to plot. The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. Once the phase plots and gain are generated the system may need to be changed after it is analyzed. Adjust the zeroes and or poles in order to shape the gain profile and insure that the phase margin is greater than 45^{o}. Figure 2.16

below shows the asymptotic Bode gain plot for the Type III compensated system and the gain and phase equations for the compensated system. [10]



$$GAIN_{dB}(f) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPE\ III}$$

$$PHASE(f) = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPE\ III}$$

Figure 2.16: The Asymptotic Bode Gain Plot for the Type III Compensated System and the Gain and Phase Equations [10]

2.1.4.3 The K-Factor Concept

K-Factor is a convenient mathematical tool for defining the shape and characteristics of a transfer function. To reduce phase lag a flat or +1 gain slope are introduce into an amplifier transfer function. This is will result the low and high frequency gain to reduce and increased. The reduction at low frequency is equal to be increase at high frequency by a factor called K. The zero is placed a factor of K below the loop crossover and the pole is place a factor of K above in Type II amplifier [10].

2.2 Previous Problem

For the past few years, current-mode control has been the method of choice for many high-performance power supply applications. Since the technology become greater, it is not just optimum choice for all power supplies. Another choice of method is voltage-mode control. Figure 2.17 shows the plant transfer function for a Buck converter using voltage mode control.

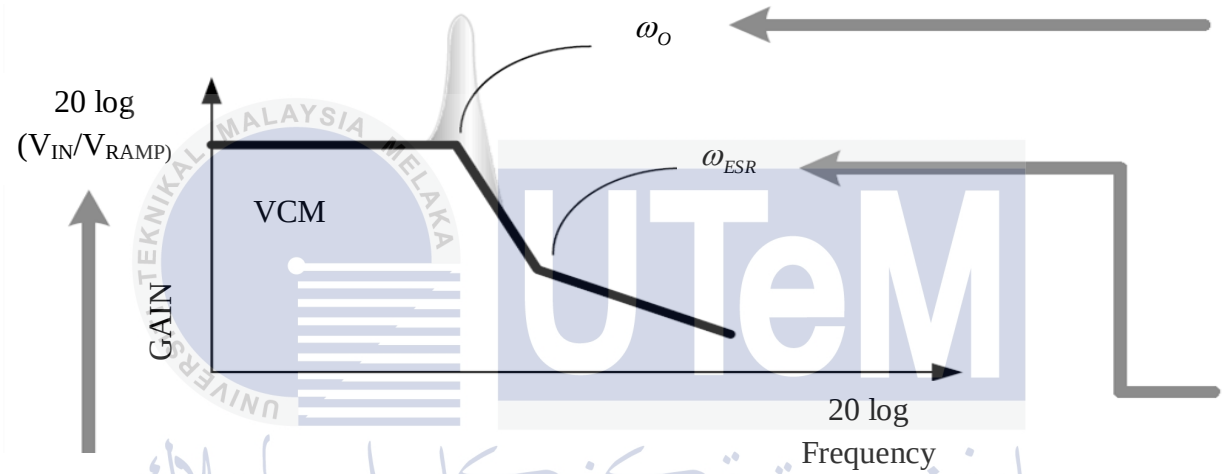


Figure 2.17: Plant Transfer Function for Buck Converter Using Voltage-mode Control [11]

The major characteristics of the design of voltage-mode control are that there is a single voltage feedback path with pulse-width modulation performed by comparing the voltage error signal with a constant ramp waveform. While for current limiting must be done separately. From Figure 2.17, it shows that the VCM of plant varies with the input voltage mode control. This will cause the loop response changes with input. In addition, the line rejection is not good under suddenly changing conditions. This is because of pulse width modulator comparator cannot get the sudden change in line and it continues with the same duty cycle for a while. At ω_o position, the double LC poles occur. This position can serve peaking in the gain plot because of high quality factor, Q with formula stated in Equation 2.14 [11]

$$Q = [Rv(C/L) \tag{2.14}$$

ω_{ESR} is located at ESR zero condition. This position give the ESR a cap has wide tolerance or spread and can vary with frequency and time aging. This position can be roughly cancelled with a pole from the compensator and with very low-ESR caps, this zero moves out to a very high frequency and then is of almost no concern anyway [11]

Voltage-mode control system cannot changing the duty cycle quickly enough leads to an output undershoot or overshoot. This system has to delay or lagging for the output error to be sensed by the error amplifier and that information to be communicated to the pulse width modulation comparator as a change in the control voltage [11]. In this situation, it is corrects the duty cycle and output after swinging back forth ringing around the settling value. If the ramp voltage can change directly and instantaneously respect to input voltage, so no need to wait or delay for the information to return via the control voltage terminal. When the line rejection would be instantaneous and DC gain would not change with input voltage. In addition, to implement the voltage-mode control, line feedforward will be state in Equation 2.15 [11].

$$\begin{aligned} V_{RAMP} &\propto V_{IN} \\ \frac{V_{IN}}{V_{RAMP}} &= \text{Constant} \end{aligned} \tag{2.15}$$

Buck converter current-mode control is difference from voltage-mode control in term of gain which is the DC gain is not function of input voltage. The reason of this is the pulse width modulator ramp is derived from the current ramp and the current swing, Δi_L is a function of the voltage across the inductor during the ON-time. Current-mode control has a single pole at the resonant frequency of the load resistor and the output cap. This is contrast with voltage-mode control which there is two poles at the resonant frequency of the inductor and output cap. This will cause the compensator voltage-mode control more complex if compared to compensator current-mode control.

Current-mode control used Type II compensator and voltage-mode control used Type III compensator. The different between this two is despite cancelation of the double arising the voltage-mode control, where it has a huge residual phase shift in the region around the cancelation frequency [11].

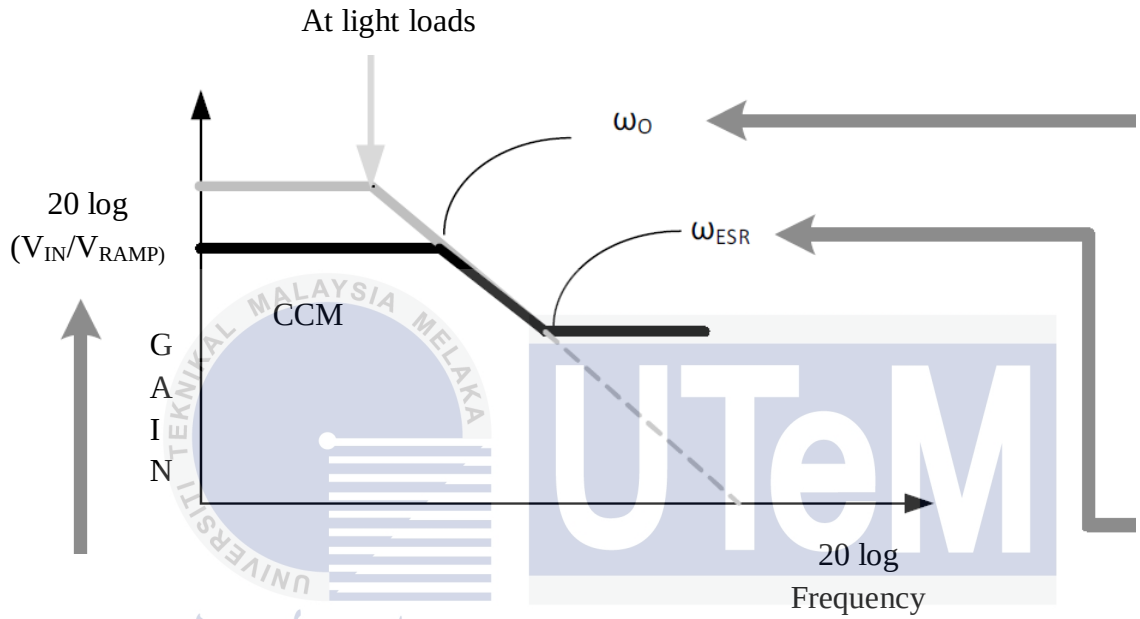


Figure 2.18: Plant Transfer Function for a Buck Using Current-Mode Control

Figure 2.18 shows the DC gain of buck converter using current-mode control which is the plant is not vary with input voltage. This will result loop response is steady with the input and proportional to resistor and load current. At output pole, ω_o position, the single pole is no peaking and inversely proportional to resistor and proportional to load current. Meanwhile at ESR zero, ω_{ESR} position, the ESR of a cap has wide tolerance and varies with frequency and time. In addition, in current-mode control must have pole cancellation in the compensator or pole move out to a very high frequency which is becomes irrelevant.

Hysteresis control is other latest control method. The bandwidth of the loop response is close to the switching frequency and result the no feedback or no zeroes and poles to manipulate.

The mathematical models very complicated because in hysteresis control do not used clock or error amplifier and make this control method very suitable for modern battery-powered applications. Hysteresis control also does not have limitations and this is because of no clock that make hard to assure constant frequency.

2.3 Summary of Review

In brief, this chapter discussed about buck converter, current-mode control, voltage mode control and compensator. Almost type used of current-mode control is peak-current mode control. Comparison between current-mode control and voltage-mode control has included in this project. This two control mode will compare in term of how many poles are use and which control mode more stable. Voltage-mode control is single feedback loop and it is easier to design and analyze. Current-mode control is more predictable and acceptable response in general. Hysteresis is advance and good because no formal clock and error amplifier but the designed very difficult and complex. Accordingly to compensator, Type III compensator more stable because have two poles but hard to designed which compared to Type II compensator more simple and easy to designed the compensator circuit.

CHAPTER 3

DESIGN METHODOLOGY

This design methodology chapter will discuss the methods and procedures, as well as in the entire work process used in simulation computing software like Pspice and Matlab. In this chapter also included the step on how to complete this thesis project in the correct flow. This project has divided into two parts which the first part was called Final Year Project I and the second part is called Final Year Project II. In Final Year Project I, the project work focused in open-loop power stage of the buck converter. As an extension to Final Year Project I, Final Year Project II continue the circuit design and simulation work that focused on closed-loop circuit which called peak current-mode control and voltage-mode control of buck converter.

3.1 Project Activity

Before start do the project title as The Development of Peak Current Mode Control of Buck Converter, at first phase must recognize the main point in the project. After get the main point like buck converter, current-mode control, voltage-mode control and compensator, start do research about literature review. Literature review is mainly based on design issue and technique

for current-mode control, voltage-mode control, buck converter and compensator. Mostly citations in literature review get from IEEE journals, conference paper and journals.

After that, second phase needs proceed to design the simulation of peak current-mode control and simulation of voltage-mode control. Before start design the simulation circuit, mathematical calculation must be done first to make sure the simulation result become smooth and validate. Among the things to do calculations are duty ratio, minimum and maximum inductor current and value of capacitor. Although get the value of inductor and capacitor during the calculation, but in simulation use assumed value to get the better result and less the inductance current ripple. After get both simulation result of control mode, do the validation to make sure the objective and scope of project reached. If both result validate, go the next phase and if not, return back to simulation process to do troubleshoot.

Next phase is result analysis. In this phase, it is discussed about result that gets from simulation process by using Pspice simulation software. At first, the waveform is not so much smooth and the inductance current ripple is too high. After troubleshoot the problem, then identified that problem came from value of inductance and capacitance in simulation circuit. After increase the value of inductance and capacitance, get the better waveform result and also can reduce inductance current ripple. The next phase continues in Final Year Project II in Semester II.

The next phase that continue in Final Year Project II started from cascaded the power stage of buck converter with pulse width modulator (PWM) to simulate the open loop response using Matlab coding. The open-loop response was designed to make sure that the system was stable. Once the system stable, the parameters from the compensator will used in designing peak current-mode control and voltage-mode control closed-loop circuit. After get the value of

parameters from type-II compensator, start the simulation of both type of controller closed-loop circuit.

Once get the result, compare the both type of controller in term of average steady state voltage, inductor current, output voltage ripple, inductor current ripple and output voltage ripple percentages. When both result valid each other in through the comparison, proceed with result analysis. After finish the analysis and get the expected result, means the objectives and goals of this project was achieve.

3.1.1 Flowchart

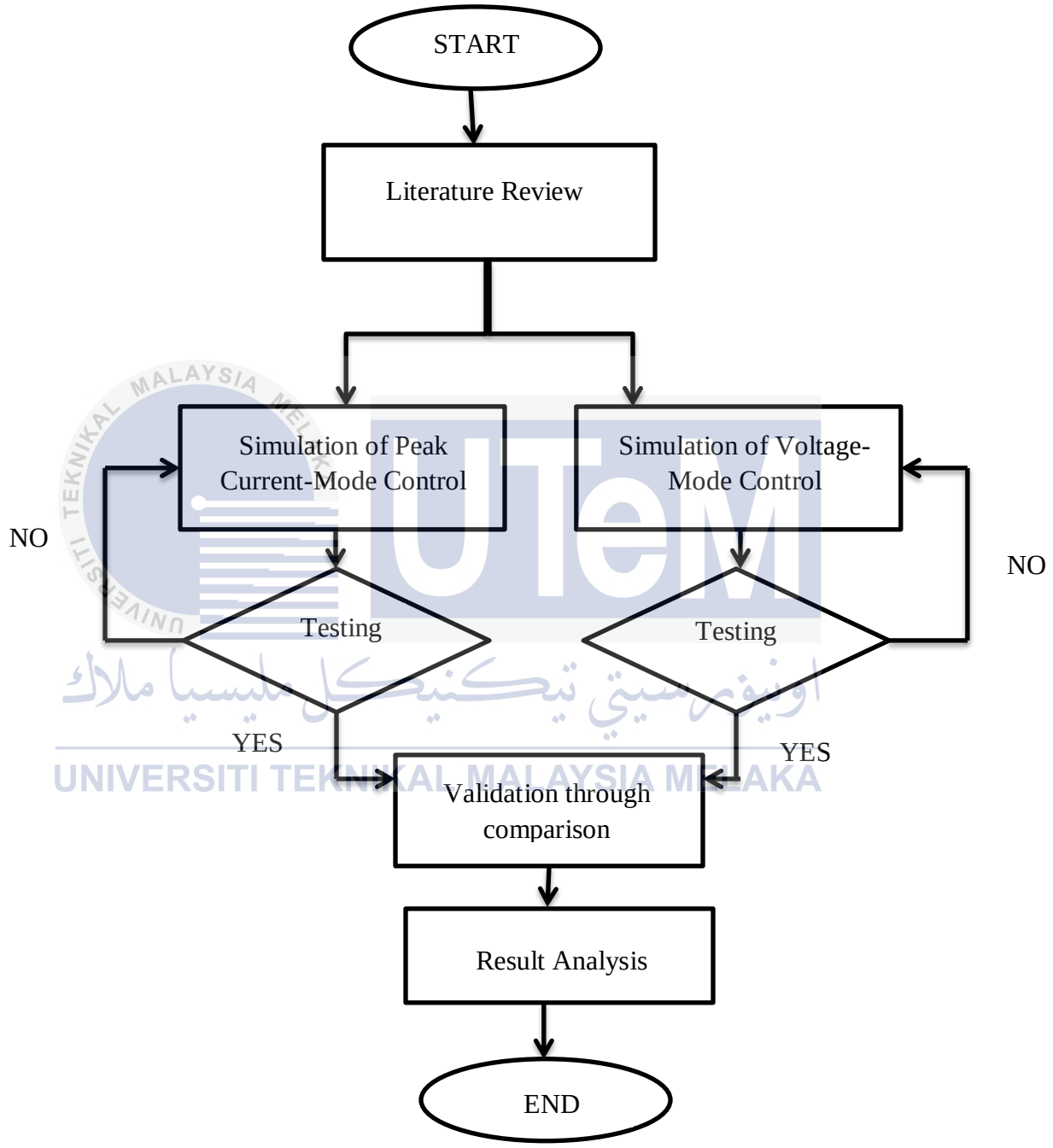


Figure 3.1: Flowchart of Project Activity

3.2 Simulation

3.2.1 Mathematical Modeling

A general method for describing a circuit that changes over a switching period is called state-space averaging. A state-variable description of a system is of the form in Equation 3.1 [5]

$$\dot{x} = A_C + B_v \tag{3.1}$$

$$V_O = C^T x \tag{3.2}$$

When in switched closed condition:

$$\dot{x} = A_{1x} + B_{1v} \tag{3.3}$$

$$V_O = C_1{}^T x \tag{3.4}$$

When in switched open condition:

$$\dot{x} = A_{2x} + B_{2v} \tag{3.5}$$

$$V_O = C_2{}^T x \tag{3.6}$$

The time dT represents the switch closed while $(1\text{-}d)$ T represents the switch open and a weighted average from above equation is given below.

$$\dot{x} = [A_1 d + A_2 (1\text{-}d)]\, x + [B_1 d + B_2 (1\text{-}d)]\, v \tag{3.7}$$

$$V_O = [C_1{}^T d + C_2{}^T (1\text{-}d)]\, x \tag{3.8}$$

Thus general from describe an average state-variable description of the systems are:

$$A = A_1 d + A_2 (1-d) \quad (3.9)$$

$$B = B_1 d + B_2 (1-d) \quad (3.10)$$

$$C^T = C_1^T d + C_2^T (1-d) \quad (3.11)$$

For the steady state, $\dot{X} = 0$ and small-signal values are zero. Then, the equation becomes

$$0 = AX + BV \quad (3.12)$$

$$X = -A^{-1}BV \quad (3.13)$$

$$V_O = -C^T A^{-1} BV \quad (3.14)$$

For small-signal of weighted averaged, it becomes

$$\dot{\tilde{X}} = [A_1 D + A_2 (1-D)]\, \tilde{X} + [(A_1 - A_2) X + (B_1 - B_2) V]\, \tilde{d} \quad (3.15)$$

$$\tilde{V}_O = [C_1^T + C_2^T (1-D)]\, \tilde{X} + [(C_1^T - C_2^T) X]\, \tilde{d} \quad (3.16)$$

The small-signal transfer characteristic is developed, which in the case of the buck converter results in

$$\dot{\tilde{X}} = A\tilde{X} + BV_S \tilde{d} \quad (3.17)$$

Taking the Laplace Transform

$$s\tilde{x}(s) = A\tilde{x}(s) + BV_S \tilde{d}(s) \quad (3.18)$$

Grouping $\tilde{x}(s)$

$$[sI\text{-}A]\,\tilde{x}(s) = BV_S\,\tilde{d}(s) \tag{3.19}$$

Where I is the identify matrix. Solving for $\tilde{x}(s)$

$$\tilde{x}(s) = C^T\tilde{x}(s) = C^T\,[sI - A]^{-1}\,BV_S\,\tilde{d}(s) \tag{3.20}$$

Expressing $\tilde{v_o}(s)$ in terms of $\tilde{x}(s)$

$$\tilde{v_o}(s) = C^T\,\tilde{x}(s) = C^T\,[sI - A]^{-1}\,BV_S\,\tilde{d}(s) \tag{3.21}$$

The transfer function of output to variations in the duty ratio is expressed as

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = C^T[sI - A]^{-1}BV_S \tag{3.22}$$

3.2.1.1 Buck Converter State Equation

State-space averaging is a method for describing a circuit that changes over a switching period. For buck converter state-space averaging it needed two set of state equation which are when switch closed and when switch is open. [5] Figure 3.2 and Figure 3.3 below show the equivalent circuit of switch closed and open of buck converter [5].

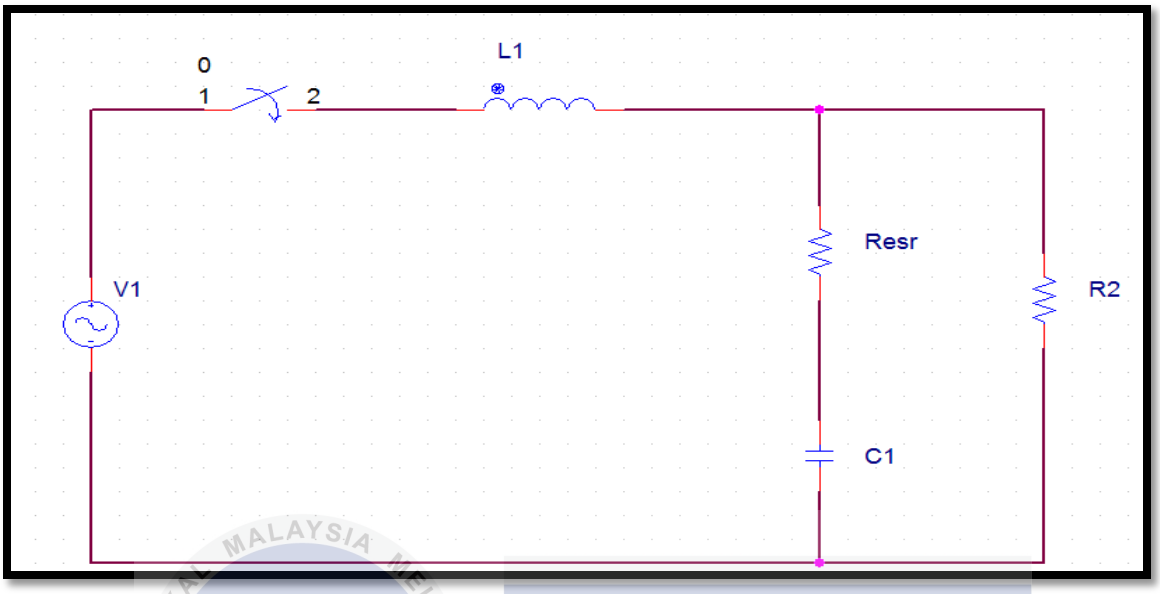


Figure 3.2: Buck Converter Switch Closed Equivalent Circuit [5]

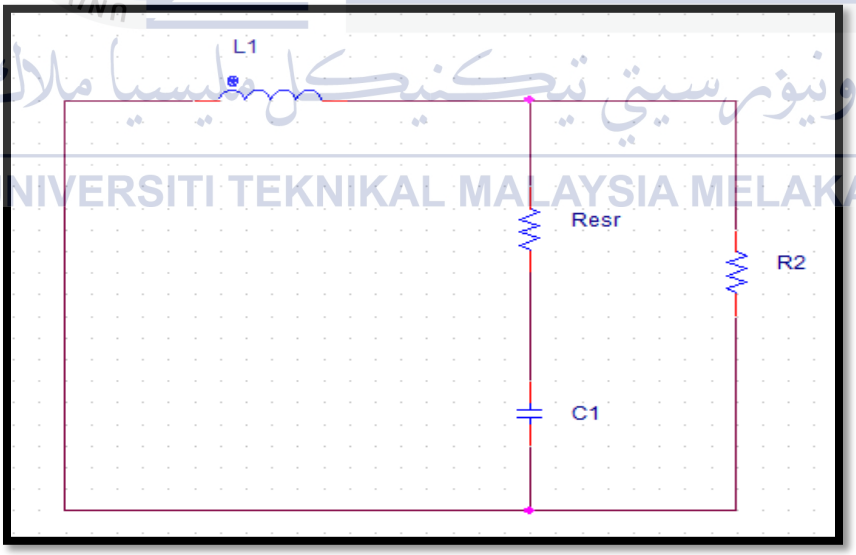


Figure 3.3: Buck Converter Switch Open Equivalent Circuit [5]

In switch closed condition, Kirchhoff's Voltage Law equation is [5]

$$L\frac{d_{iL}}{dt} + i_r R = V_S \tag{3.23}$$

Kirchhoff's Current Law equation is

$$i_r = i_L - i_C = i_L - \frac{d_{VC}}{dt} \tag{3.24}$$

Kirchhoff's Voltage Law around the left inner loop is

$$L\frac{d_{iL}}{dt} + i_c r_c + V_C = V_S \tag{3.25}$$

Which the relation is:

$$i_c = C\frac{d_{vc}}{dt} = \frac{1}{r_c}(V_s - L\frac{d_{il}}{dt} - v_c) \tag{3.26}$$

Sate equation by combining Equation 3.23 and Equation 3.25 become

$$\frac{d_{iL}}{dt} = -\frac{R_{rc}}{L(R+r_c)}i_L - \frac{R}{L(R+r_c)}v_c + \frac{v_s}{L} \tag{3.27}$$

Kirchhoff's Voltage Law around the right inner loop gives

$$-v_c - i_c r_c + i_r R = 0 \tag{3.28}$$

State equation comes by combination Equation 3.27 and Equation 3.24 is

$$\frac{d_{vc}}{dt} = \frac{R}{C(R+r_c)} i_L - \frac{1}{C(R+r_c)} v_c \tag{3.29}$$

Equation 3.28 and equation 3.26 in state variable form is

$$\dot{X} = A_1 x + B_1 V_s \tag{3.30}$$

Where [5]

$$\dot{X} = \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{3.31}$$

$$\begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} 1/L \\ 0 \end{bmatrix} \tag{3.32}$$

$$B_1 = \frac{1/L}{0} \tag{3.33}$$

If in condition $R_c << R$,

$$A_1 \approx \begin{bmatrix} \frac{-r_c}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \quad (3.34)$$

When switch open the filter is the same and a matrix remain unchanged during the switching period

$$A_2 = A_1 \quad (3.35)$$

State Equation 3.25 is modified become

$$B_2 = 0 \quad (3.36)$$

Weighting the state variable over one switching period is gives as

$$\dot{\chi} = A_1 x d + B_1 V_s d \quad (3.37)$$

$$\dot{\chi}\,(1\text{-d}) = A_2 x(1-d) + B_2 V_s (1-d) \quad (3.38)$$

Using $A_1 = A_2$ [5]

$$\dot{\chi} = A_1 + [B_1 d + B_2 (1-d)] V_s \quad (3.39)$$

In expanded form

$$\begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \frac{-r_c}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} d/L \\ 0 \end{bmatrix} \mathrm{V_S} \tag{3.40}$$

The output voltage, v_o is determined from

$$v_o = Ri_r = R(i_L - i_r) = R(i_L - \frac{V_O - v_c}{r_c}) \tag{3.41}$$

Then rearrange the equation become

$$v_o = (\frac{Rr_c}{R + r_c})i_L + (\frac{R}{R + r_c})v_c \approx r_c i_L + v_c \tag{3.42}$$

The above equation is valid for both switch positions, resulting in $C_1^T = C_2^T = C^T$. In state variable form is

$$v_o = C^T x \tag{3.43}$$

Where:

$$C^T = \begin{bmatrix} \frac{Rr_c}{R + r_c} & \frac{R}{R + r_c} \end{bmatrix} \approx \begin{bmatrix} r_c & 1 \end{bmatrix} \tag{3.44}$$

And

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{3.45}$$

The steady state output equation is come from combination of Equation 3.43 and Equation 3.44 [5]

$$v_o = -C^T A^{-1} B V_S \tag{3.46}$$

Where:

$$A=A_2=A_1,\ B_1D \tag{3.47}$$

$$C_1^T = C_2^T = C^T \tag{3.48}$$

$$V_O = V_S D \tag{3.49}$$

$$\dot{\tilde{x}} = A\tilde{x} + BV_S\tilde{d} \tag{3.50}$$

Taking the Laplace Transform

$$s\tilde{x}(s) = A\tilde{x}(s) + BV_S\tilde{d}(s) \tag{3.51}$$

Solving for $\tilde{x}(s)$

$$\tilde{x}(s) = [sI\text{-}A]^{-1}BV_S\tilde{d}(s) \tag{3.52}$$

Expressing $\tilde{v}_o(s)$ term $\tilde{x}(s)$ is

$$\tilde{v}_o(s) = C^T\tilde{x}(s) = C^T[sI - A]^{-1}BV_S \tag{3.53}$$

The transfer function of output to variations in duty ration is expressed as

$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = C^T [sI - A]^{-1} BV_S \quad (3.54)$$

Substituting for the matrix in Equation 3.42, a lengthy evaluation process results in the transfer function is [5]

$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = \frac{V_S}{LC}\left[\frac{1+sr_cC}{s^2+s(\frac{1}{RC}+\frac{r_c}{L})+\frac{1}{LC}}\right] \quad (3.55)$$

3.2.2 Power Stage Design

The analysis design of power stage buck converter was done which the parameters have calculated the duty ratio, maximum and minimum inductor current and the value of capacitor and inductor. Design specifications for buck converter are list in Table 3.1.

Table 3.1: Design Specifications for Buck Converter

Parameters	Value
Input Voltage, V_i	30V
Output Voltage, V_o	15V
Output Current, I_o	0A to 7A
Maximum output voltage ripple, $\Delta V_o(pp)$	0.5%
Switching Frequency, f_s	100KHz
Load Resistor, R	2.5Ω

According to obtained inductor and capacitor value, the first calculation was done by estimate the duty ratio by using input and output voltage based on equation $V_O = V_S D$. The duty ratio was calculated by using formula: [5]

$$D = \frac{v_0}{v_i} = \frac{30}{15} = 0.5 \tag{3.56}$$

After getting the D value, the value of inductor current (i_L) and the value of capacitor (C) and inductor (L) for the buck converter were determined. Based on equation $I_L = I_R = \frac{v_O}{R}$, the inductor current was calculated:

$$I_L = I_R = \frac{v_O}{R} \tag{3.57}$$

$$I_L = \frac{15V}{2.5\Omega} = 6.0 \text{ A}$$

Thus, using Equation 3.58 and Equation 3.59, the value of inductor, L and capacitor, C for the buck converter determined as

$$L_{Min} = \frac{(1-D)R}{2f} \tag{3.58}$$

$$L_{Min} = \frac{(1-0.5)(2.5\Omega)}{2(100KHz)}$$

= 6.25 µH

In simulation part, use inductor value 56µH as assumed value to get better simulation result.

To make sure that continuous current occurred inductance will be assumed 25% greater from L_{Min}. When value of L=56 μH which is equal assumption value, calculated for capacitor is:

$$C = \frac{1-D}{8L(\frac{\Delta V_O}{V_O})f^2} \tag{3.59}$$

$$C = \frac{1-0.5}{8(56\mu H)(\frac{0.5}{100}x\frac{1}{15})(100K)^2}$$

= 334.82 µF

In simulation part, use capacitor value 680 µF as assumed value to get better simulation result.

The maximum and minimum values of inductor current are calculated by Equation 3.60 and Equation 3.61 [5]

$$I_{MAX} = I_L + \frac{\Delta i_L}{2} \tag{3.60}$$

$$= \frac{V_O}{R} + \frac{1}{2}\left[\frac{V_O}{L}(1-D)T\right]$$

$$= \frac{15}{2} + \frac{1}{2}\left[\frac{15}{56\mu F}(1-0.5)10\mu\right]$$

= 8.17 A

$$I_{MIN} = I_L - \frac{\Delta i_L}{2} \tag{3.61}$$

$$= \frac{V_O}{R} - \frac{1}{2}\left[\frac{V_O}{L}(1-D)T\right]$$

$$= \frac{15}{2} - \frac{1}{2}\left[\frac{15}{56\mu F}(1-0.5)10\mu\right]$$

= 6.83 A

3.3 Simulation Design of Buck Converter Power Stage

Figure 3.4 shows the power stage construction circuit of buck converter by using Pspice software.

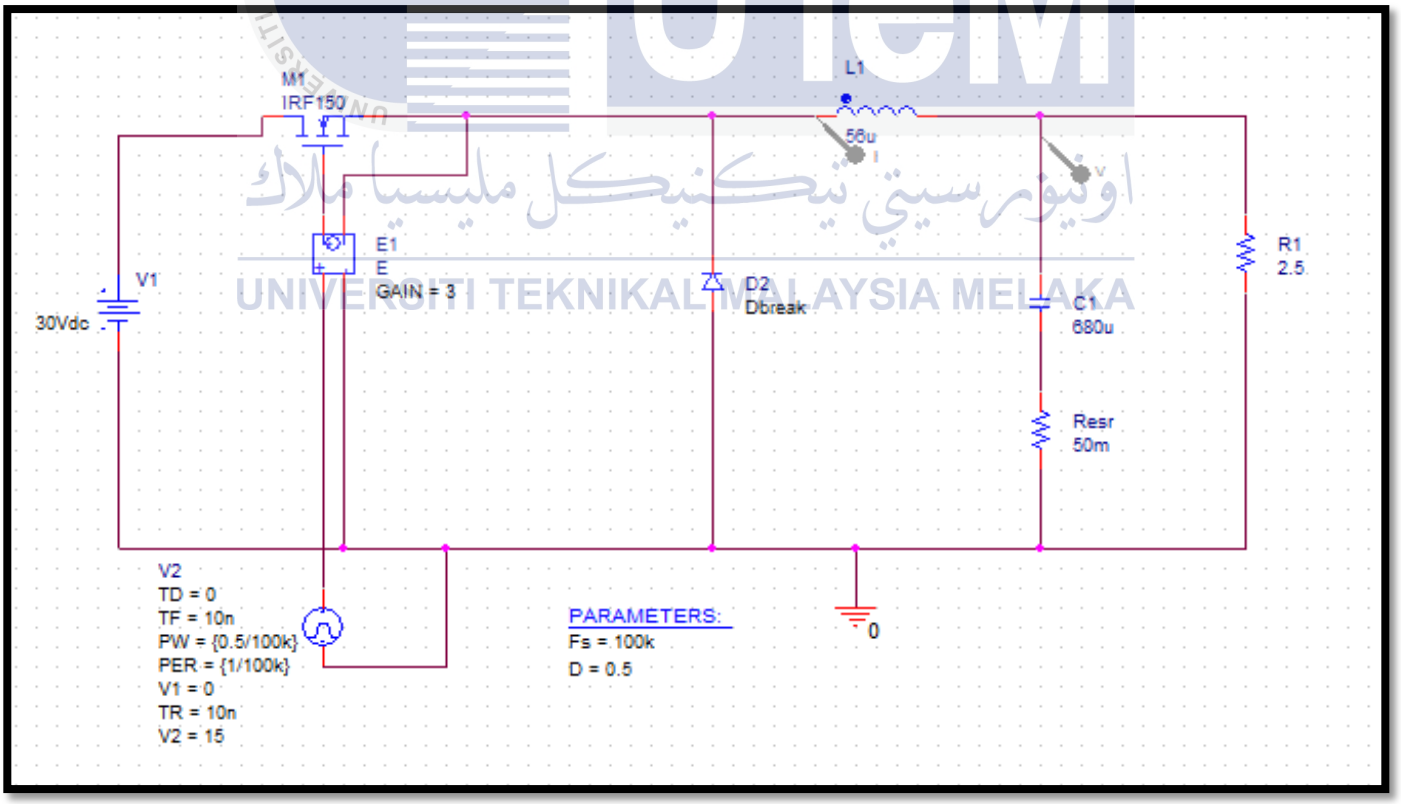


Figure 3.4: Power Stage Construction Circuit of Buck Converter

3.4 Type II Compensator Design Procedure

Type II compensator has two poles, where one pole at the origin and one other pole at zero-pole pair for references. Type II compensator can obtain maximum boost at 90^o, since there is only one zero. K-factor concept is a convenient mathematical tool for describing the shape and characteristics of transfer function. The zero is located a K-factor below loop crossover and the pole is located a K-factor above in type II compensator.

The following steps below are design procedure for type II compensated error amplifier: [5]

1. Generate the open loop bode plot by multiplying the power stage buck converter transfer function with the pulse width modulation (PWM) transfer function.

2. Desired crossover frequency was chosen of the total open-loop transfer function. The crossover frequency was selected 20 KHz or 125.66 K rad/sec. The switching frequency was selected 100 KHz. To reach the high bandwidth, 1/5 of the switching frequency was selected which is equal to 20 KHz.

3. To ensure stability, the desired phase margin was chosen. The phase margin value that has been chooses typically greater than 45^o. In this project, phase margin selected was 55.5^o.

4. From open loop bode plot, the phase shift and gain margin was selected at the crossover frequency.

5. The parameter for type-II compensator will be calculated from the formula below. [5]

a. To find value of K, used formula, $K= \frac{\omega_p}{\omega_{co}}$ (3.62)

i.

$$w_p = (2)x(\pi)x(\frac{1}{2} f_s) \quad (3.63)$$

$$w_p = (2)x(\pi)x(\frac{1}{2} x100KHz)$$

$$w_p = 314.16Krad/\sec$$

ω_{co} = Crossover frequency

ii. (3.64)

$$\omega_{co} = (2)x(\pi)x(\frac{1}{5} f_s)$$

$$\omega_{co} = (2)x(\pi)x(\frac{1}{5} x100KHz) \qquad \omega_{co} = 125.66Krad/\sec$$

iii. $K = \frac{\omega_p}{\omega_{co}}$

$$= \frac{314.66Krad/\sec}{125.66Krad/\sec}$$

$= 2.5$

b. 20 log G = Gain Margin (3.65)

Gain= $10^{(\text{gain margin}/20)}$

c. Assume value of R_1, to calculate value of R_2, C_1 and C_2.

d. $R_2 = \frac{K}{(2)x(\pi)x(f_s)x(c_1)}$ (3.66)

e. $C_1 = C_2 (K^2-1)$ (3.67)

f. $C_2 = \frac{1}{(2\pi)x(f_s)xG)x(K)x(R_1)}$ (3.68)

6. With the calculated values a type-II compensator is build and added to the feedback loop of the buck converter.

Figure 3.5 shows the open-loop response transfer function for buck converter from command window Matlab simulation software. Next figure which is Figure 3.6 shows the open-loop response transfer function was read at crossover frequency from command window Matlab simulation software.

```
R=2.5;
C=680e-6;
L=56e-6;
r=50e-3;
Vs=30;
Vo=15;
D=0.5;
Vp=1.8;

%power stage.....................
stage=tf (Vs*[r*C 1], [L*C L/R+r+C 1])

%pwm.....................................

pwm=1/Vp

%powerstage*pwm.....................
transfer=stage*pwm

bode(transfer)
grid on
title ('Open-Loop')
```

```
Transfer function:
       0.00102 s + 30
-----------------------------
3.808e-008 s^2 + 0.0507 s + 1


pwm =

    0.5556


Transfer function:
     0.0005667 s + 16.67
-----------------------------
3.808e-008 s^2 + 0.0507 s + 1
```

Figure 3.5: Open-loop Response Transfer Function for Buck Converter from Command Window Matlab Simulation Software

```
R=2.5;
C=680e-6;
L=56e-6;
r=50e-3;
Vs=30;
Vo=15;
D=0.5;
Vp=3;
wz=512.5;
wp=314.16e3;

%power stage.............................
stage=tf(Vs*[r*C 1],[L*C L/R+r*C 1])
stage2=tf([1/wz 1], [1/wp 1 0])
%pwm.....................................
pwm=1/Vp

%powerstage*pwm..........................
%transfer=stage
%transfer=stage*pwm
%transfer=13.48*stage*pwm
%transfer=13.48*stage*pwm*stage2
transfer=13.48*stage*pwm*stage2*555.904
bode(transfer)
grid on
title ('Open-Loop')
```

```
Transfer function:
      0.00102 s + 30
-----------------------------
3.808e-008 s^2 + 5.64e-005 s + 1

Transfer function:
  0.001951 s + 1
------------------
3.183e-006 s^2 + s


pwm =

    0.3333


Transfer function:
         0.004971 s^2 + 148.8 s + 7.494e004
-----------------------------------------------------
1.212e-013 s^4 + 3.826e-008 s^3 + 5.958e-005 s^2 + s
```


Figure 3.6: Open-loop Response Transfer Function of Buck Converter was read at crossover frequency from Command Window Matlab Simulation Software

3.5 Simulation Design Peak Current-Mode Control of Buck Converter

Figure 3.7 shows the peak current-mode control of buck converter construction circuit by using Pspice software.

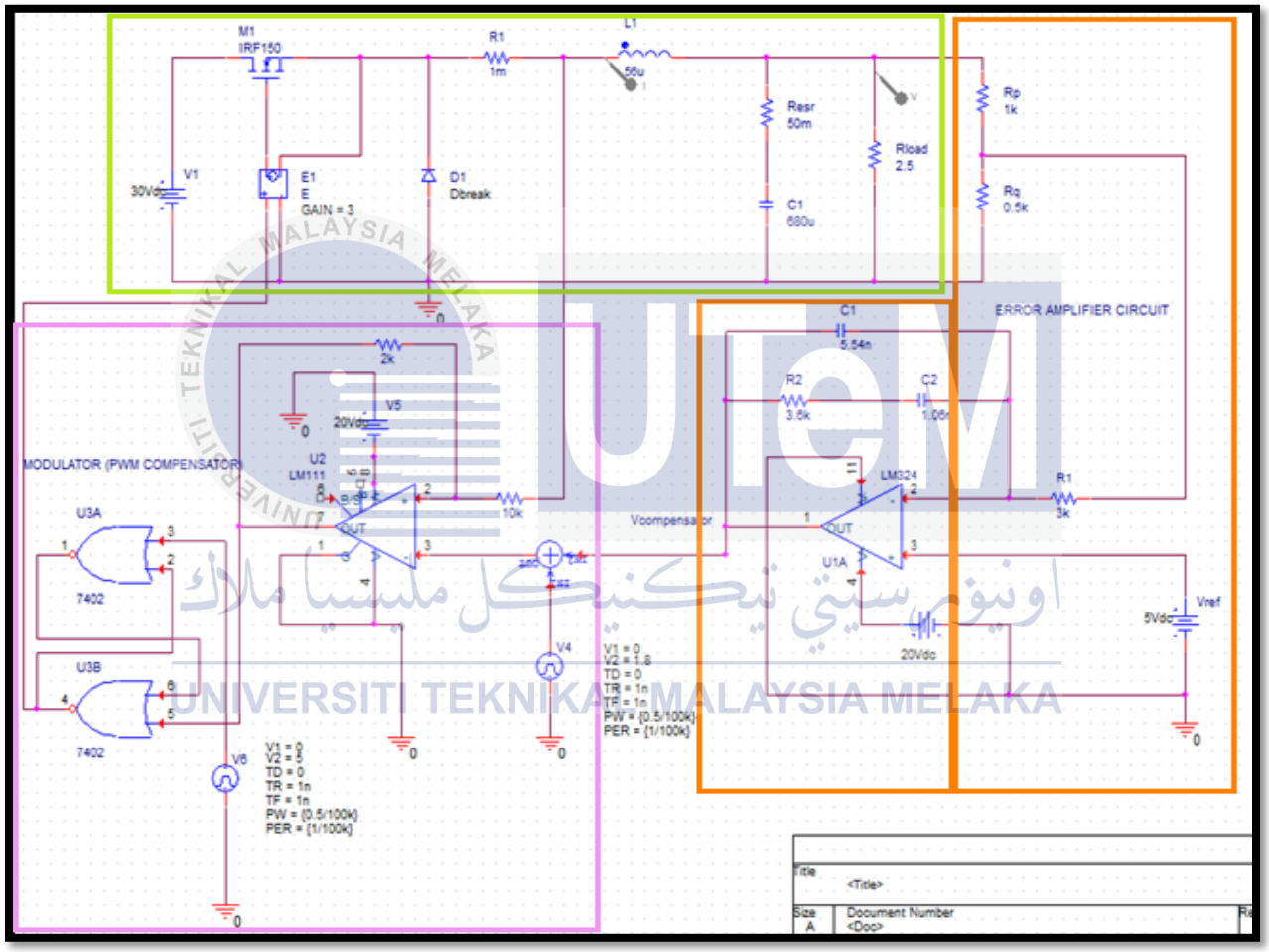


Figure 3.7: Peak Current-Mode Control of Buck Converter Design Circuit by Using Pspice Software

Figure 3.7 shows that circuit peak current-mode control of buck converter. This design circuit divided to three (3) mini circuits by follow the colour division. Circuit in green box is

called as basic circuit of buck converter where also known as power stage. This open-loop circuit can operate in continuous or discontinuous inductor current mode. The input and output voltage of this circuit is stable and fix as input voltage is 30V and output voltage is 15V. This value is fixing because in open-loop circuit, duty ratio determined through calculation.

The circuit in orange box is called error amplifier compensator circuit. This circuit is included in closed-loop circuit and known as outer loop. Outer loop in this circuit means the loop is controlled by voltage controller and this is the reason why this loop slow compared to inner loop. Output voltage that has been sense at R_1 will be compared to reference voltage from 5V dc source. The output from this comparison called compensator voltage and become input modulator-PWM compensator circuit.

The circuit in pink box is called as converter circuit (modulator-PWM compensator). This circuit is included in closed-loop circuit. In this circuit has one part which named as inner loop. This inner loop current, i_L is sense from voltage drop of R_1 at power stage circuit. R_1 is an additional sense resistor which the purpose is to sense the current, i_L pass through the R_1. This inner loop is faster than outer loop because this loop controlled by inductor current, i_L. Voltage drop value in R_1 is called voltage sense resistor. Compensator voltage from error amplifier compensator circuit will compared first with saw-tooth signal from ramp generator before become input to converter circuit.

Next step is voltage sense resistor from inner loop will compare with compensator voltage from outer loop to regulated duty cycle. Duty cycle behavior is depend on PWM comparator that produces a pulse which allow i_L to rise up until hit compensator voltage then it fall down until meet another pulse and continue same step. This routine will produce a duty cycle that will drive up the MOSFET. The period to MOSFET to ON or OFF is depends on width of duty cycle produces that related with input voltage and output voltage value.

3.6 Simulation Design Voltage-Mode Control of Buck Converter

Figure 3.8 shows the voltage-mode control of buck converter construction circuit by using Pspice software.

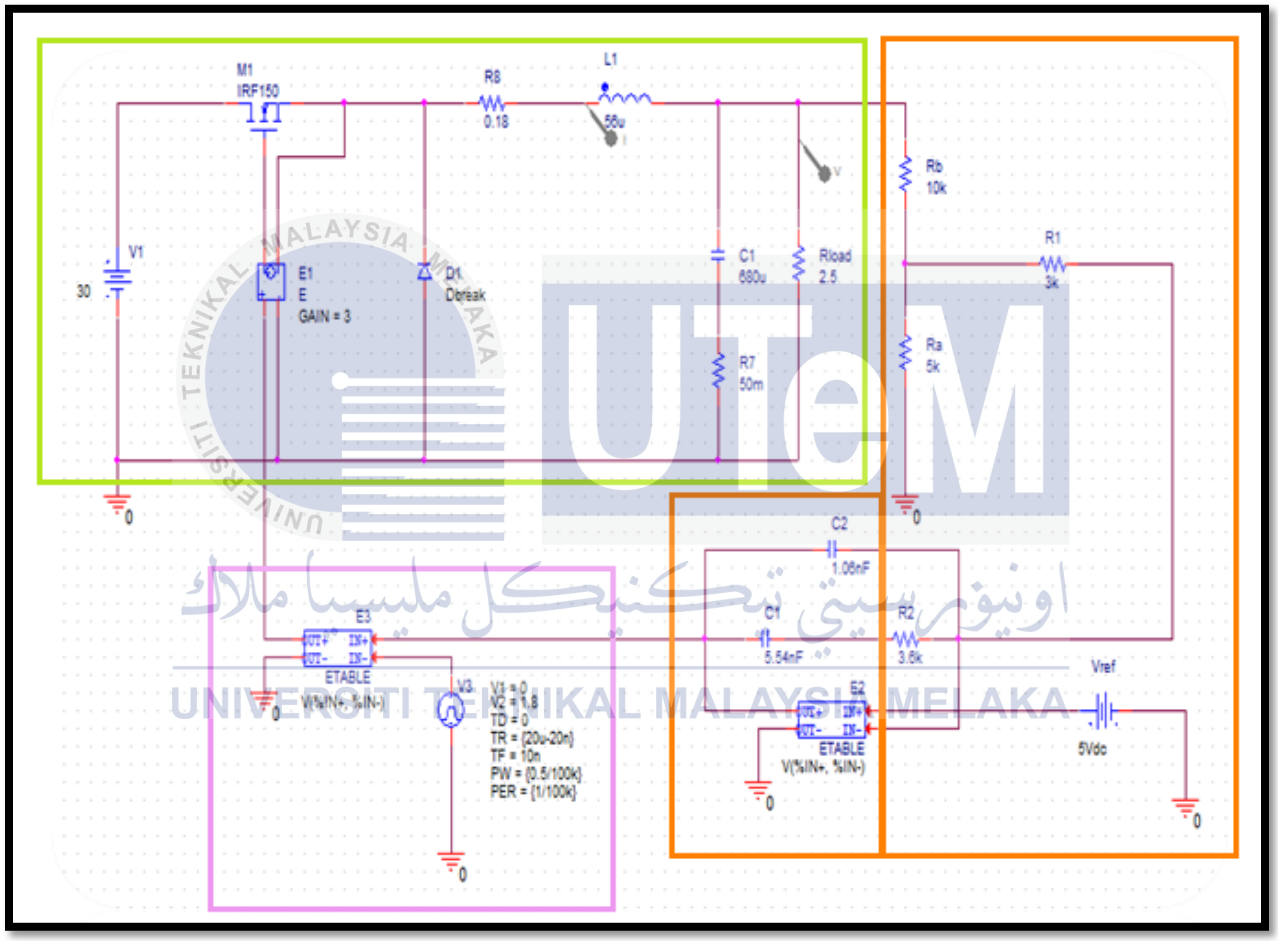


Figure 3.8: Voltage-Mode Control of Buck Converter Construction Circuit by Using Pspice Software

Figure 3.8 shows that circuit voltage-mode control of buck converter. This design circuit divided to three (3) mini circuits by follow the colour division. Circuit in green box is called as

basic circuit of buck converter where also known as power stage. This open-loop circuit can operate in continuous or discontinuous inductor current mode. The input and output voltage of this circuit is stable and fix as input voltage is 30V and output voltage is 15V. This value is fixing because in open-loop circuit, duty ratio determined through calculation.

The circuit in orange box is called error amplifier compensator circuit. This circuit is included in closed-loop circuit. In this circuit, Etable component in Pspice software was used to represent as error amplifier compensator circuit. Etable is a component that purposely to define a voltage-controlled voltage source. This Etable aims to facilitate users to be able to do the simulation proses in simple and convenient way. Output voltage that has been sense at R_1 will be compared to reference voltage from 5V dc source. The output from this comparison called compensator voltage and become input modulator-PWM compensator circuit.

The circuit in pink box is called as converter circuit (modulator-PWM compensator). This circuit is included in closed-loop and it's also uses Etable to represent the converter circuit. Compensator voltage from error amplifier compensator circuit will compared with saw-tooth signal from ramp generator to regulated duty cycle. Duty cycle behavior is depend on PWM comparator that produces a pulse which allow inductor current to rise up and hit voltage compensator then it fall down again until meet another pulse and continue the same step. This routine will produce a duty cycle that will drive up the MOSFET. Output from PWM also produces pulse to the circuit driver. When the circuit driver has got the pulse, it will trigger the pulse to MOSFET. The period to MOSFET to ON or OFF is depends on width of duty cycle produces that related with input voltage and output voltage value.

CHAPTER 4

RESULT, ANALYSIS AND DISCUSSION

This chapter discusses the simulation results of the open-loop power stage buck converter, peak current-mode control and voltage-mode control of the buck converter. All these circuit designs were simulated using Pspice and Matlab simulation software. The objective of the simulation was to make comparison between peak current-mode control and voltage-mode control of the buck converter in term of output voltage ripple and inductor current ripple.

4.1 Power Stage Buck Converter Result

All the parameter for power stage buck converter is state in Table 4.1 with maximum output voltage ripple, $\Delta V_O(pp)$

Table 4.1: Parameters of Power Stage Buck Converter

Parameter	Value
Inductor, L	56 μH
Capacitor, C	680 μF
Maximum Inductor Current, $i_{L,MAX}$	7 A
Duty Ratio, D	0.5
Switching Frequency	100 KHz

Figure 4.1 shows the result simulation of buck converter in terms of voltage and current. From this simulation result, the value of maximum and minimum of inductor current are 6.4292A and 5.3331A. To get the value of average inductor current, the value of maximum inductor current must be minus the value of minimum inductor current. When get the value of minus result, divided that value over 2. The equation is state in Equation 4.1 [5]. Value of output voltage that gets from simulation is 15V from input voltage 30V. Then give value of duty ratio, D as 0.5.

$$I_{L,Average} = \frac{I_{L,Max} - I_{L,Min}}{2} \tag{4.1}$$

Figure 4.1 shows the power stage buck converter result from Pspice simulation software.

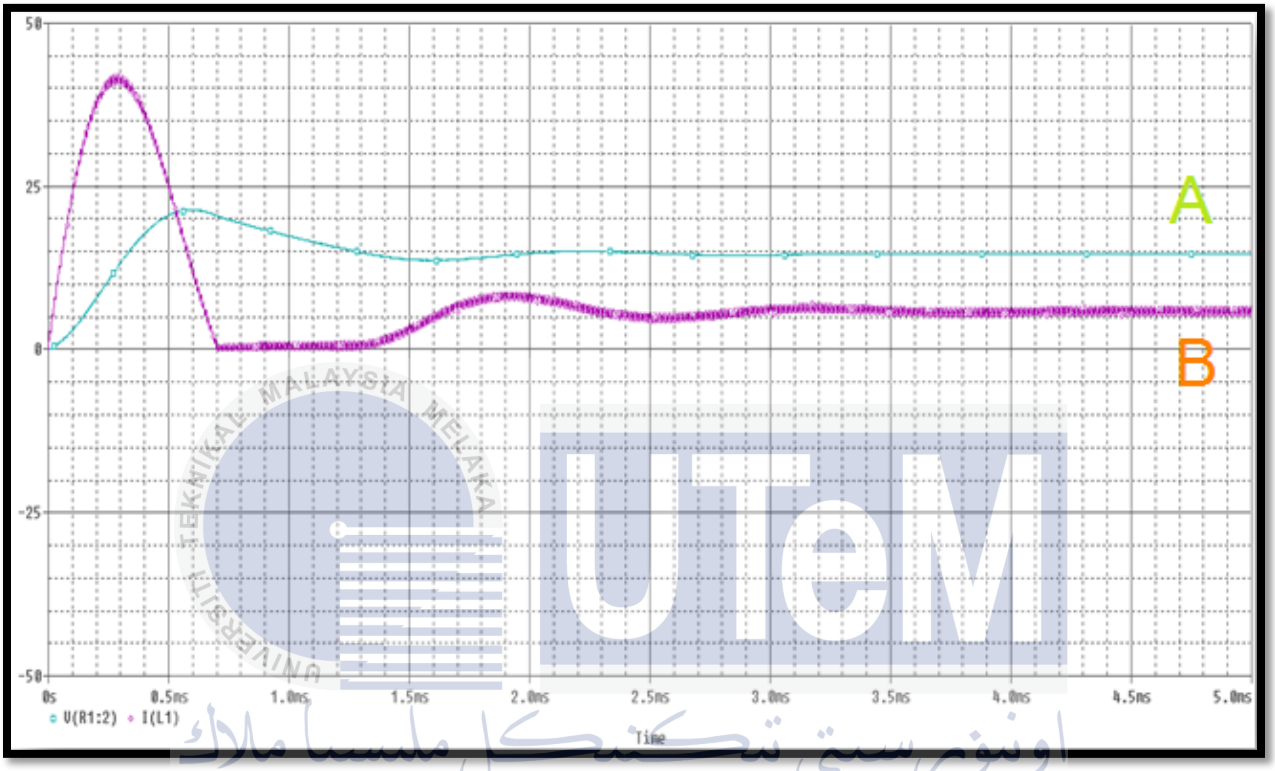


Figure 4.1: Power Stage Buck Converter Result from Pspice Simulation Software

Figure 4.1 shows the power stage buck converter result. The blue line graph with green word A is represent as output voltage of power stage buck converter. While the purple line graph with orange word B is represent as output current of power stage buck converter.

Figure 4.2 shows the output voltage of power stage buck converter result from Pspice simulation software.

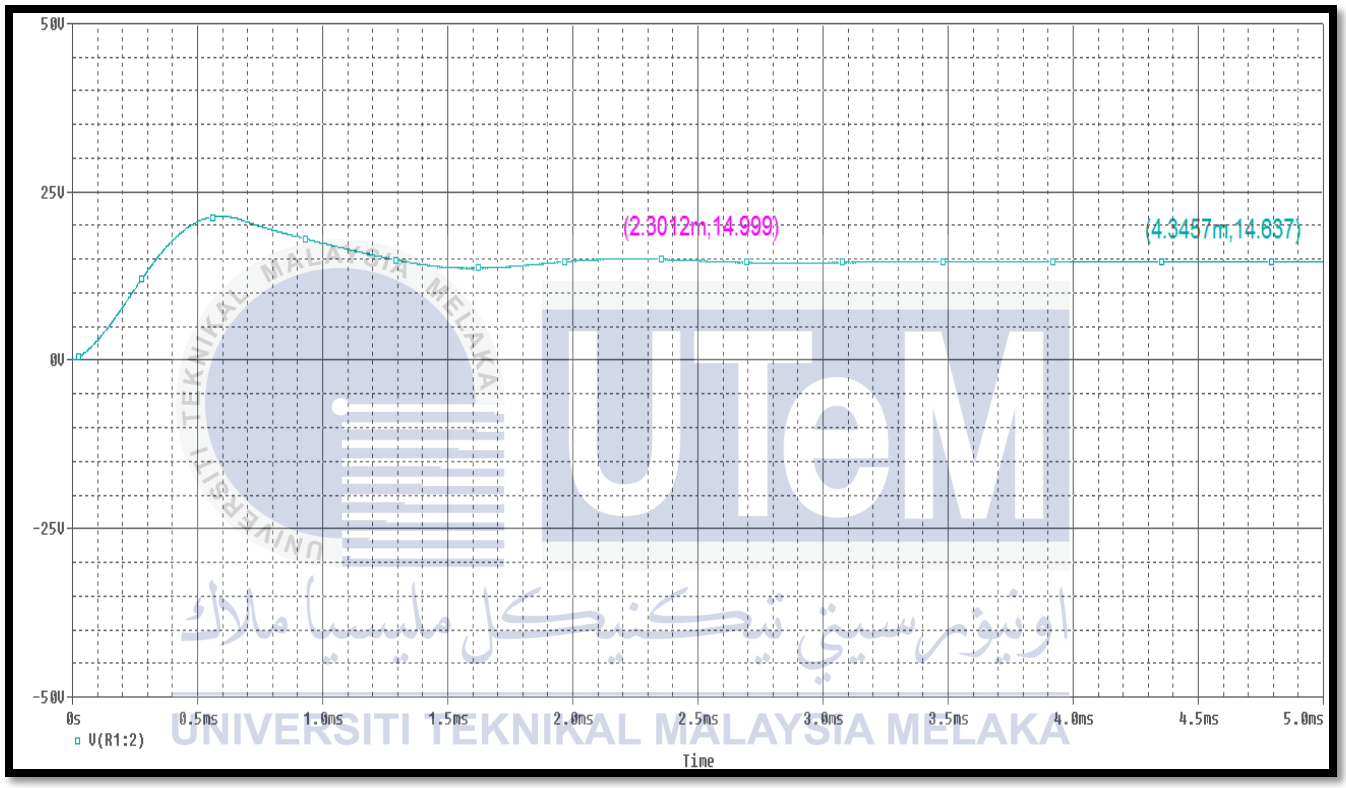


Figure 4.2: Output Voltage of Power Stage Buck Converter Result from Pspice Simulation Software

Figure 4.3 shows the output current of power stage buck converter result from Pspice simulation software.

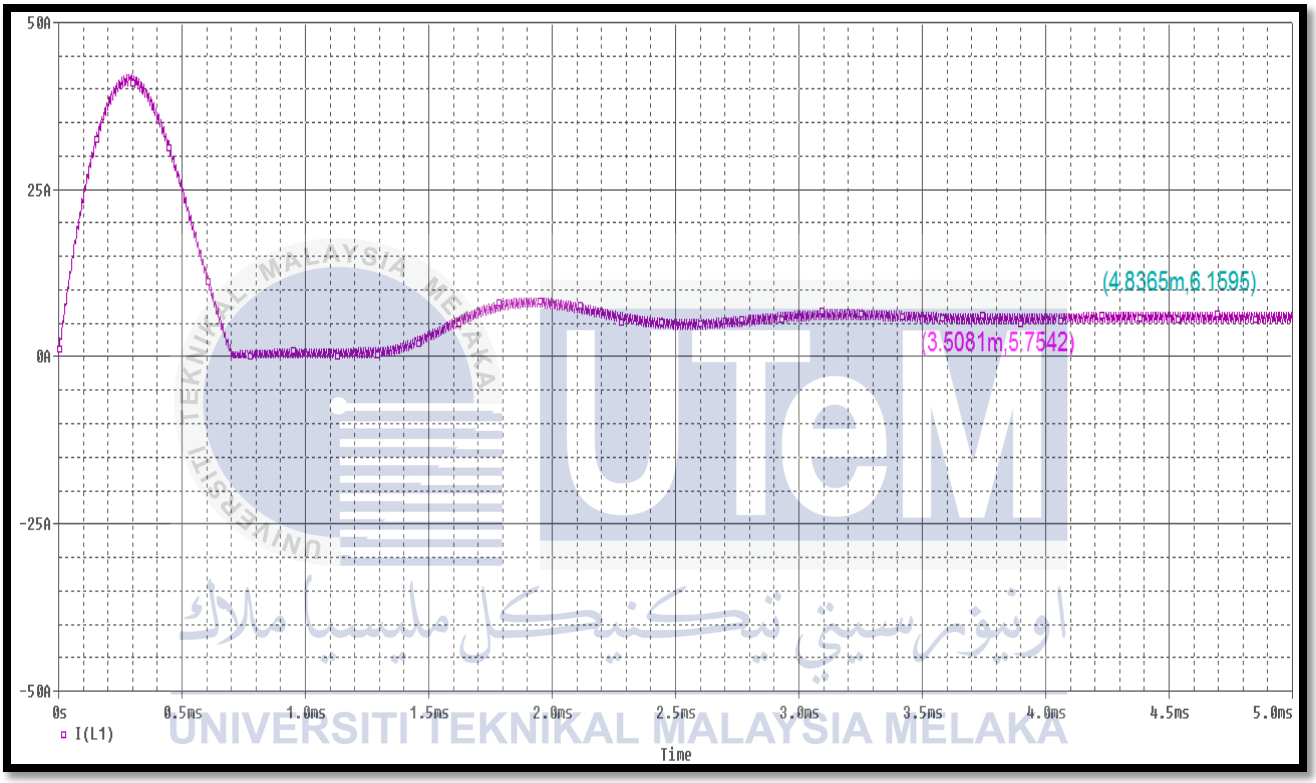


Figure 4.3: Output Current of Power Stage Buck Converter Result from Pspice Simulation Software

4.2 Power Stage Buck Converter Compensator Result

The buck converter power stage was cascaded with pulse width modulation (PWM) to simulate the open-loop response using Matlab coding simulation software. The open-lop

response was designed to make sure the system was stable. When the system has stable, the parameter that has been produced from this type II compensator for closed-loop current-mode control and voltage-mode control of buck converter will more better and realistic.

The transfer of power stage of buck converter was taken from equation:

$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = \frac{v_s}{LC}\left[\frac{1+(r_cC)s}{s^2 + s\left(\frac{1}{RC} + \frac{r_c}{L} + \frac{1}{LC}\right.}\right] \tag{4.2}$$

And the transfer function of pulse width modulation (PWM) was taken from equation:

$$\frac{d(s)}{v_c(s)} = \frac{1}{v_{osc}@v_p} \tag{4.3}$$

The gain and phase plots for open-loop buck converter are obtained by multiplying the power stage of buck converter transfer function and pulse width modulation (PWM) transfer function. The simulation result of open-loop response for buck converter is shown in Figure 4.4.

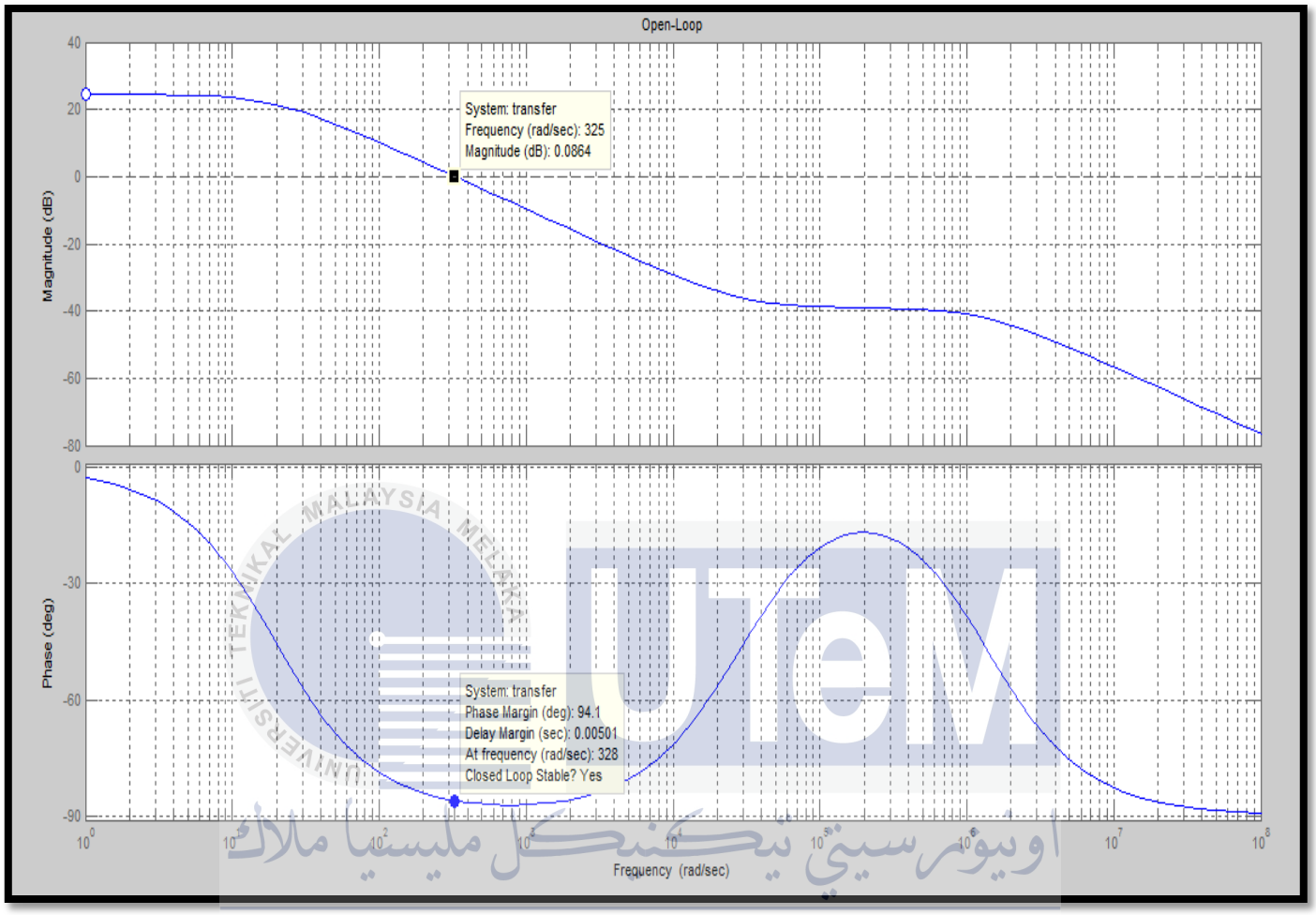


Figure 4.4: Open-Loop Response for Buck Converter Result Bode Plot form Matlab Simulation Software

Since the open-loop bode plot was generated. The crossover frequency was selected 20 KHz or 125.66K rad/sec. The switching frequency was 100K Hz and to achieve high bandwidth, select the $\frac{1}{5}$ of the switching frequency value. The Figure 4.5 shows the open-loop response for buck converter result bode plot that was read at the crossover frequency.

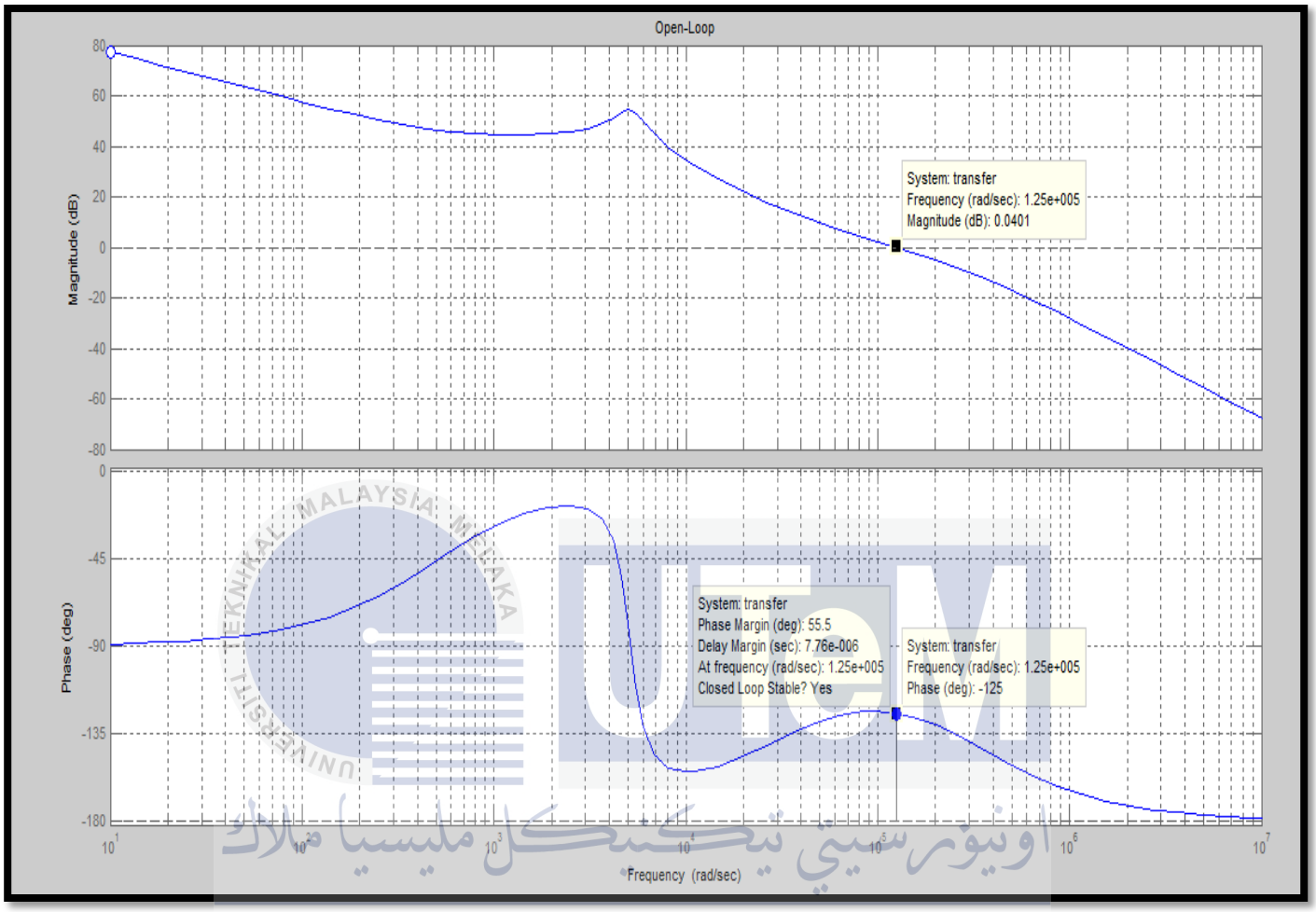


Figure 4.5: The Open-Loop Response for Buck Converter Result Bode Plot Read at the Crossover Frequency

From this open-loop bode plot result, the parameters can be obtained are:

a. Phase Shift: -125^{o}
b. Phase Margin: 55.5^{o}
c. Gain Margin: 0.0401
d. Crossover frequency: 20K Hz

The steps to calculate value of type-II compensator are shown below:

a) K= $\frac{\omega_p}{\omega_{co}}$ (3.62)

b) (3.63)

$$w_p = (2)x(\pi)x(\frac{1}{2} f_s)$$

$$w_p = (2)x(\pi)x(\frac{1}{2} x100KHz)$$

$$w_p = 314.16Krad/\sec$$

c) (3.64)

ω_{co} = Crossover frequency

$$\omega_{co} = (2)x(\pi)x(\frac{1}{5} f_s)$$

$$\omega_{co} = (2)x(\pi)x(\frac{1}{5} x100KHz)$$

d) K = $\frac{\omega_p}{\omega_{co}}$

$$= \frac{314.66Krad/\sec}{125.66Krad/\sec}$$

= 2.5

e) 20 log G = Gain Margin (3.65)

20 log G=0.0401

Gain= $10^{(\text{gain margin}/20)}$

= $10^{(0.0401/20)}$

= 1.005

f . Assume value of R_1, to calculate value of R_2, C_1 and C_2. R_1 assume equal to 3KΩ

g. $R_2 = \dfrac{K}{(2)x(\pi)x(f_s)x(c_1)}$ (3.66)

$= \dfrac{2.5}{(2)x(\pi)x(20K)x(5.544n)}$

$= 3.59\text{K}\Omega$ equal to $3.6\text{K}\Omega$

h. $C_1 = C_2 (K^2\text{-}1)$ (3.67)

$= (1.056\text{n}) \text{ x } [(2.5)^2 - 1]$

$= 5.544\text{nF}$ equal to 5.54nF

i. $C_2 = \dfrac{1}{(2\pi)x(f_s)xG)x(K)x(R_1)}$ (3.68)

$= \dfrac{1}{(2)x(\pi)x(20K)x(1.005)x(2.5)x(3K\Omega)}$

$= 1.06$ nF

With the calculated values a type-II compensator is build and added to the feedback loop of the buck converter.

4.3 Closed-Loop Buck Converter: Peak Current-Mode Control Result

Figure 4.6 shows the output result of peak current-mode control of buck converter from Pspice simulation software.

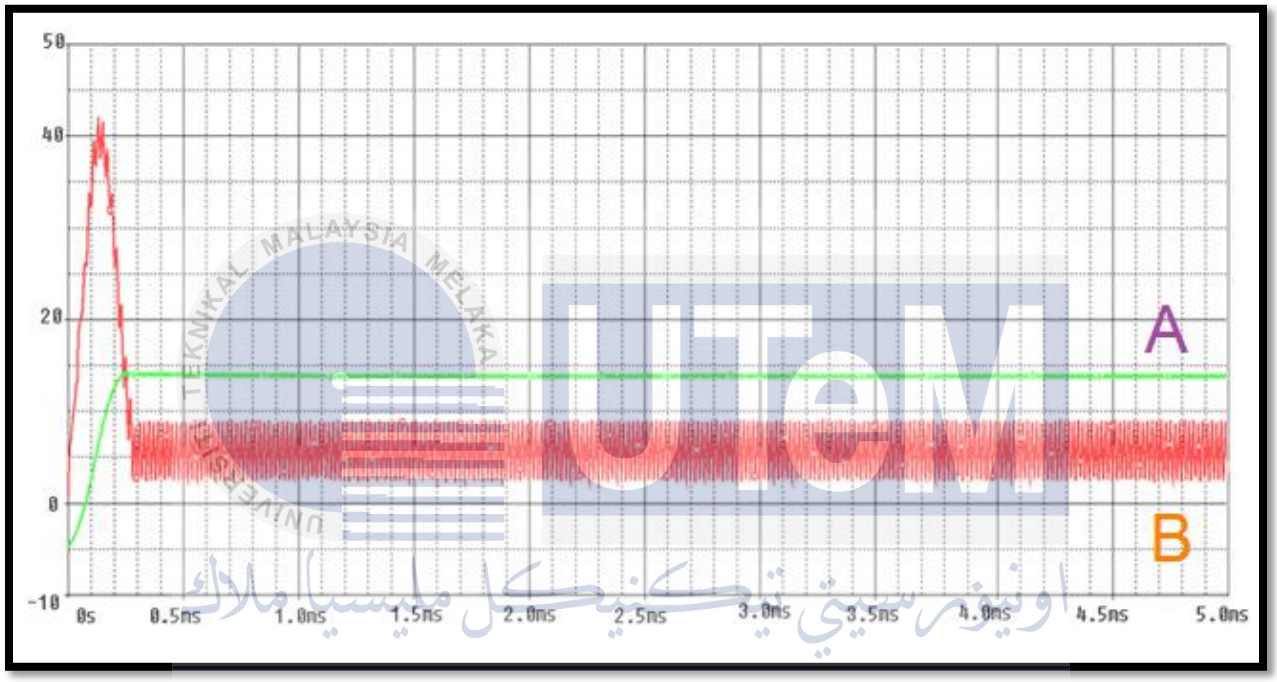


Figure 4.6: The Output Result of Peak Current-Mode Control of Buck Converter

Figure 4.6 shows the output result of peak current-mode control buck converter. The green line graph with purple word A is represent as output voltage of peak current-mode control buck converter. While the red line graph with orange word B is represent as output current of peak current-mode control buck converter.

Figure 4.7 shows the output current result of peak current-mode control of buck converter from Pspice simulation software.

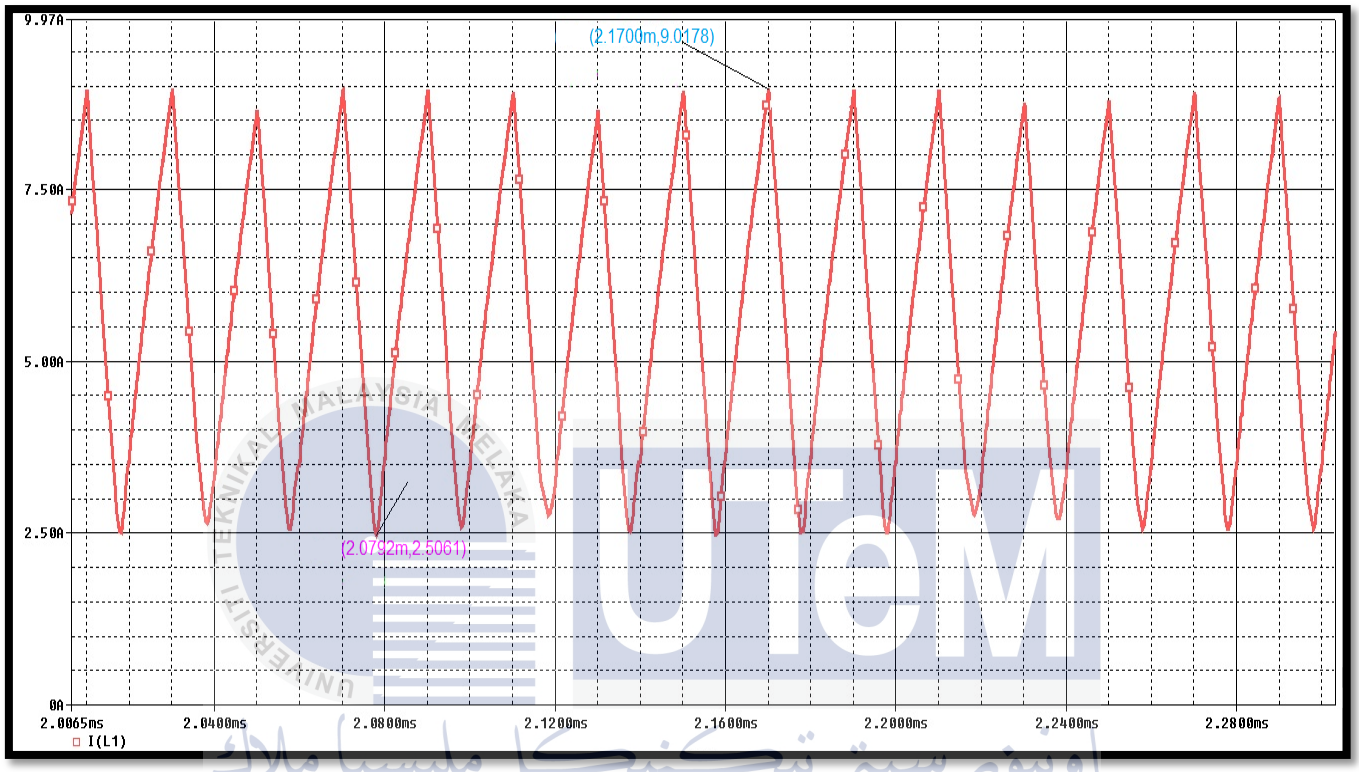


Figure 4.7: The Output Current Result of Peak Current-Mode Control of Buck Converter from Pspice Simulation Software

From Figure 4.7, it shows the maximum value of current and minimum value of current of peak current-mode control buck converter. From that value, the inductor current ripple can be calculated using the formula in equation (4.4): [5]

Inductor Current Ripple, Δi_L = (maximum current value) - (minimum current value) (4.4)

= (9.0178 A) - (2.5061 A)

= 6.5117 A

Figure 4.8 shows the output voltage result of peak current-mode control of buck converter from Pspice simulation software.

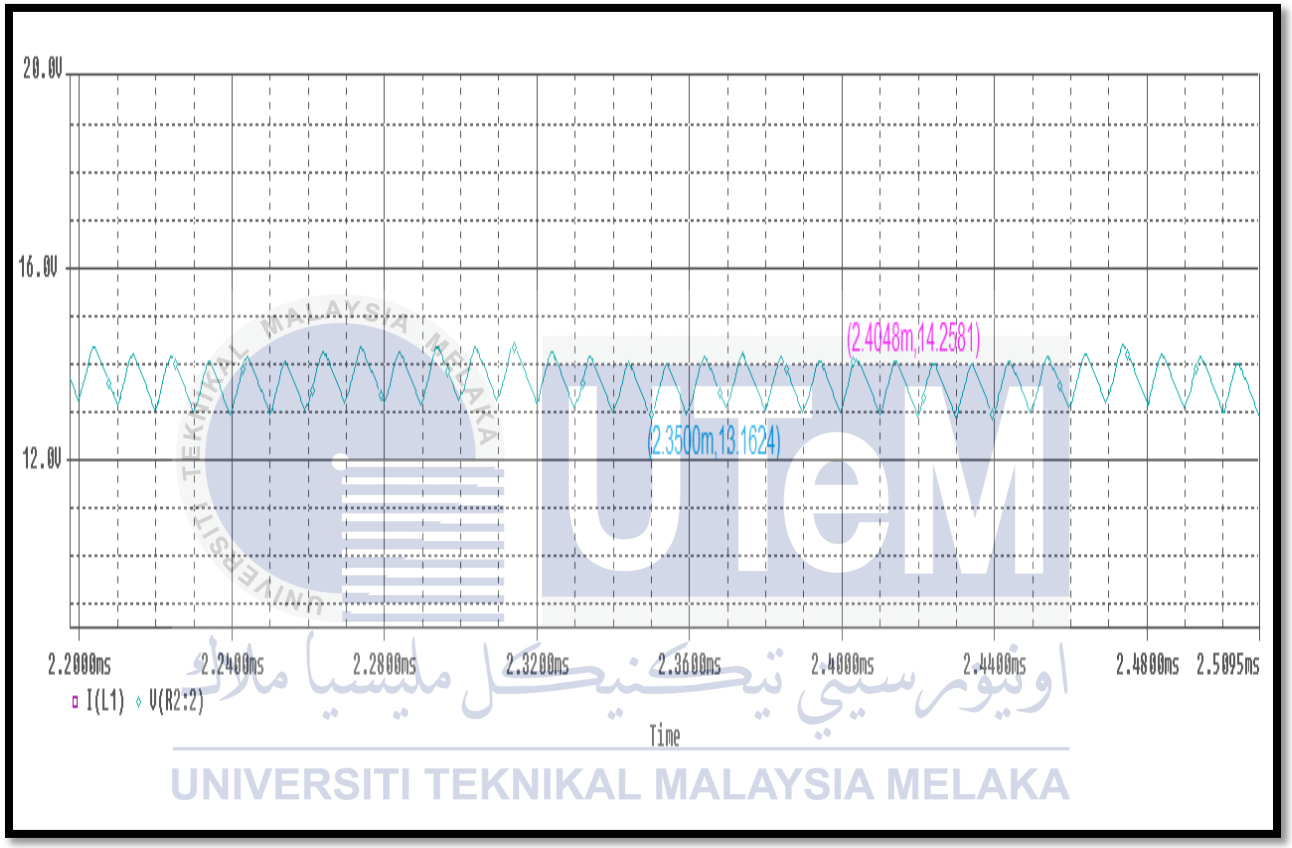


Figure 4.8: The Output Voltage Result of Peak Current-Mode Control of Buck Converter from Pspice Simulation Software

From Figure 4.8, it shows the maximum value of voltage and minimum value of voltage of peak current-mode control buck converter. From that value, the output voltage ripple can be calculated using the formula in equation (4.5): [5]

Output Voltage Ripple, Δv_o = (Inductor Current Ripple, Δi_L) x (ESR Resistance, R_{ESR}) (4.5)

= (6.5117 A) x (50m)

= 0.3256 V

Output voltage ripple percentage of current-mode control of buck converter from equation (4.6): [5]

$$\text{Output Voltage Ripple Percentage} = \frac{\Delta v_o}{(V_{max} + V_{min})/2} x100\% \quad (4.6)$$

$$= \frac{0.3256}{[(14.2581) + (13.1624)]/2} x100\%$$

= 2.37%

4.4 Closed-Loop Buck Converter: Voltage-Mode Control Result

Figure 4.9 shows the output result of voltage-mode control of buck converter from Pspice simulation software.

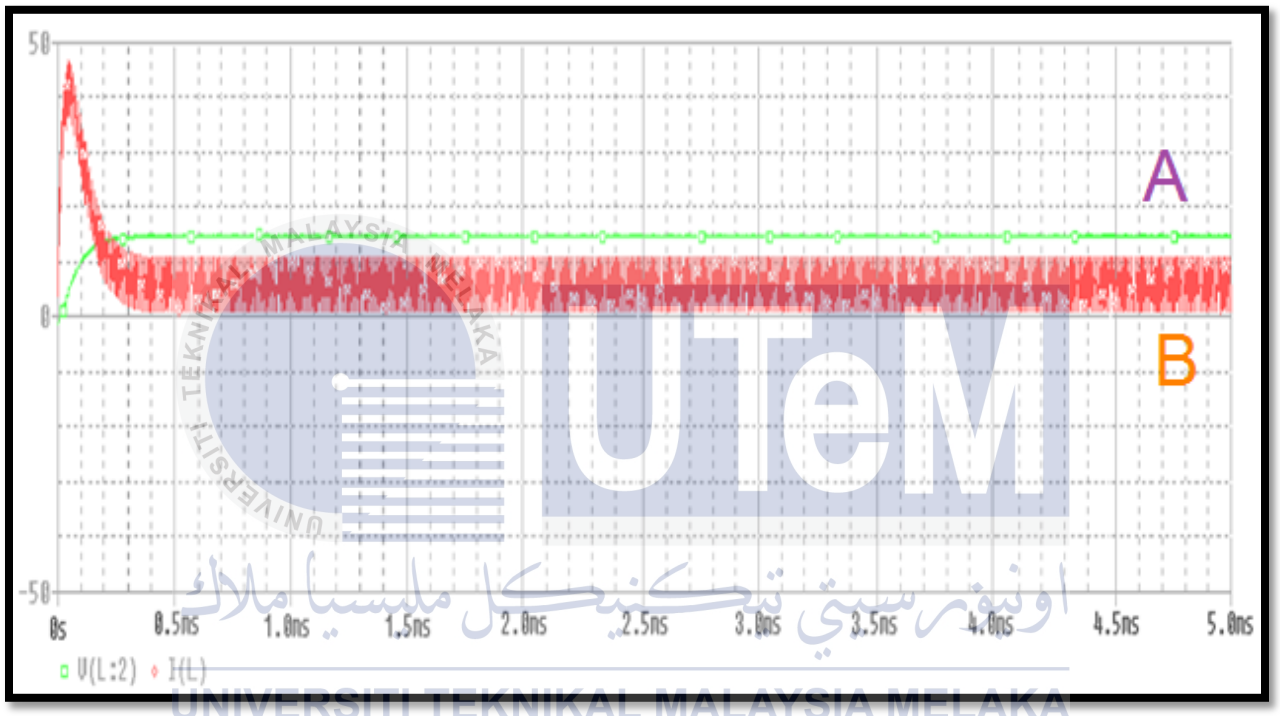


Figure 4.9: The Output Result of Voltage-Mode Control of Buck Converter from Pspice Simulation Software

Figure 4.9 shows the output result of voltage-mode control buck converter. The green line graph with purple word A is represent as output voltage of voltage-mode control buck converter. While the red line graph with orange word B is represent as output current of voltage-mode control buck converter.

Figure 4.10 shows the output current result of voltage-mode control of buck converter from Pspice simulation software.

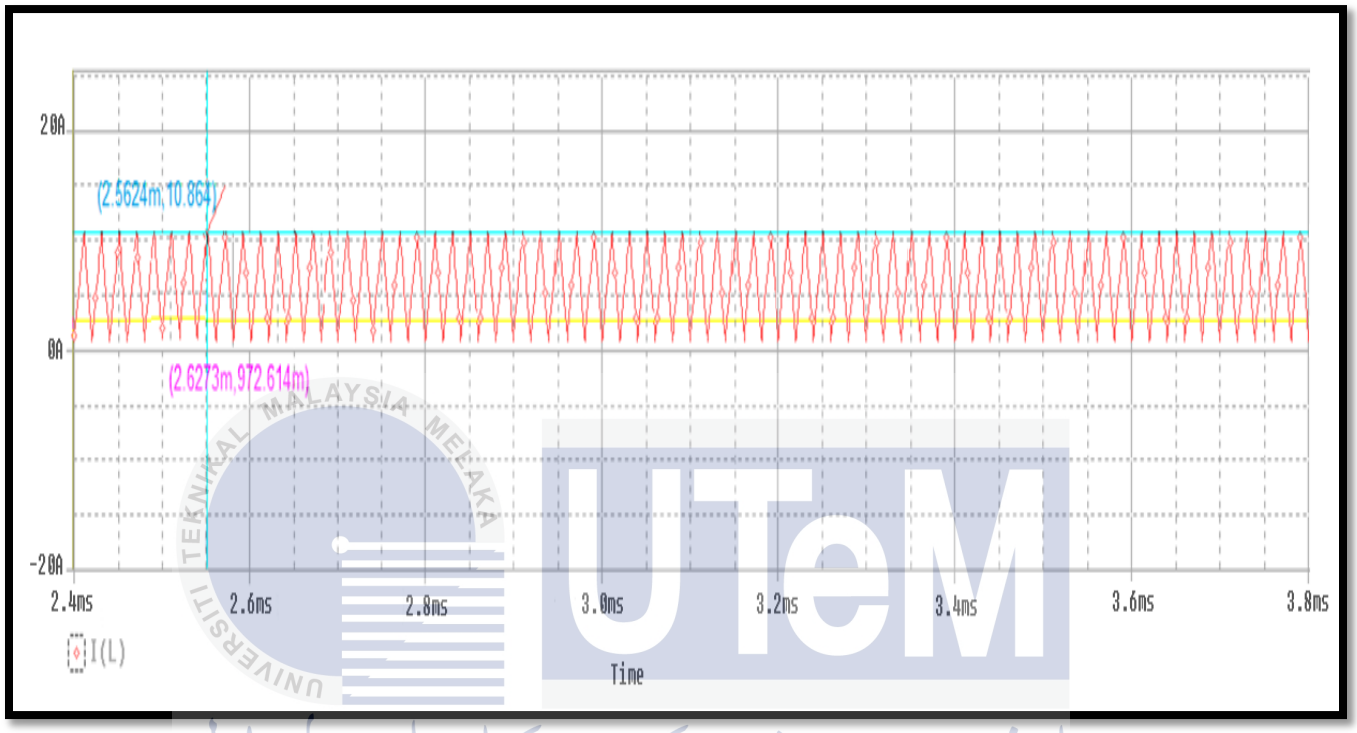


Figure 4.10: The Output Current Result of Voltage-Mode Control of Buck Converter from Pspice Simulation Software

From Figure 4.10, it shows the maximum value of current and minimum value of current of voltage-mode control buck converter. From that value, the inductor current ripple can be calculated using the formula in equation (4.4): [5]

Inductor Current Ripple, Δi_L = (maximum current value) - (minimum current value) (4.4)

= (10.864 A) - (0.973 A)

= 9.891 A

Figure 4.11 shows the output voltage result of voltage-mode control of buck converter from Pspice simulation software.

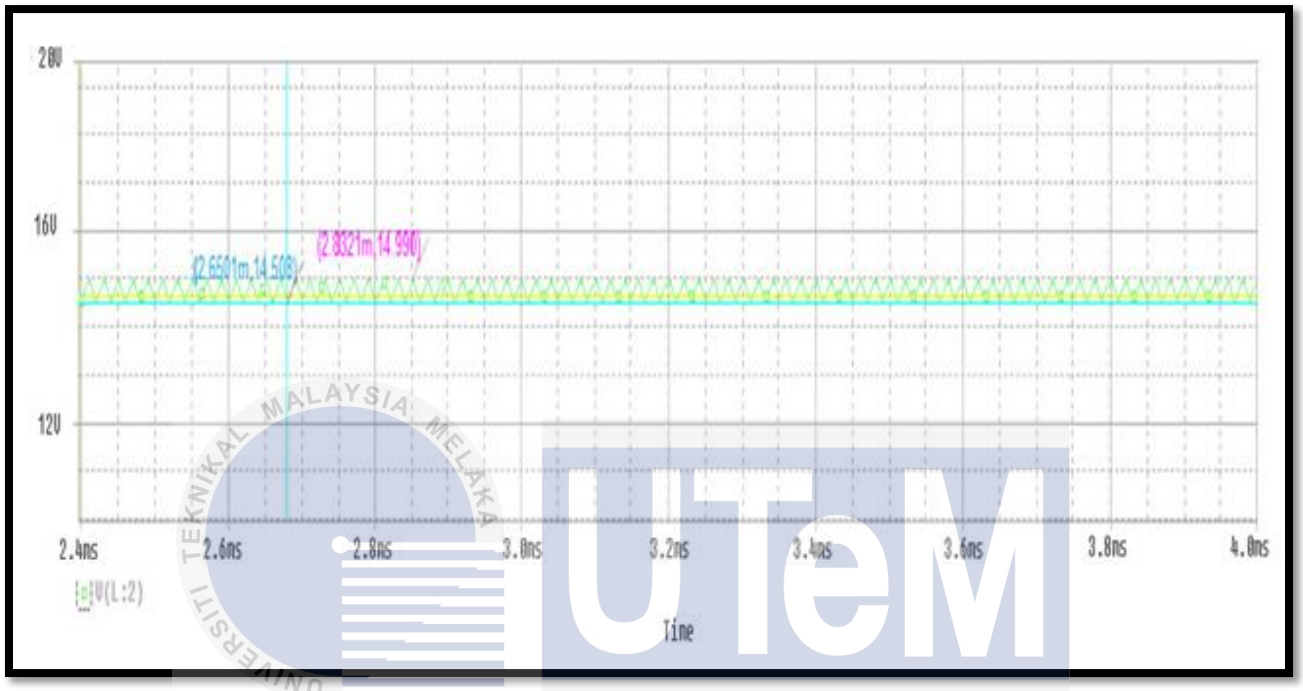


Figure 4.11: The Output Voltage Result of Voltage-Mode Control of Buck Converter from Pspice Simulation Software

From Figure 4.8, it shows the maximum value of voltage and minimum value of voltage of voltage-mode control buck converter. From that value, the output voltage ripple can be calculated using the formula in equation (4.5): [5]

Output Voltage Ripple, Δv_o = (Inductor Current Ripple, Δi_L) x (ESR Resistance, R_{ESR}) (4.5)

= (9.891 A) x (50m)

= 0.4946 V

Output voltage ripple percentage of voltage-mode control of buck converter from equation (4.6): [5]

$$\text{Output Voltage Ripple Percentage} = \frac{\Delta v_o}{(V_{\max} + V_{\min})/2} x100\% \quad (4.6)$$

$$= \frac{0.4946}{[(14.990) + (14.508)]/2} x100\%$$

$$= 3.35\%$$

4.5 Discussion of Buck Converter Simulation Result

After completing all calculation and simulation, the data have been collected from the close loop simulation result and list in Table 4.2.

Table 4.2: Close-Loop Simulation Result

Type Of Controller	Average Steady State Voltage $[(V_{max}+V_{min})/2]$, V	Inductor Current $[(I_{max}+I_{min})/2]$, A	Output Voltage Ripple, ΔV, V	Inductor Current Ripple, Δi_L, A	Output Voltage Ripple Percentage, %
Peak Current Mode Control	13.712	5.762	0.3256	6.512	2.370
Voltage Mode Control	14.749	5.919	0.4946	9.891	3.350

From the simulation result in Table 4.2, it is shown that in all response of the open-loop buck converter had been improved in term of average steady state voltage, inductor current, output voltage ripple, inductor current ripple and output voltage ripple percentage after type-II compensator is added to the closed-loop circuit. With this average steady state voltage result, it can prove that the type-II compensator fully function when the output closed-loop voltage value was rise up closed to output power stage voltage value which is equal to 15V.

For peak current-mode control average steady state voltage result is lower than the power stage design value, this is because of the voltage drop. As mention in theoretical fundamental, current-mode control has two feedback loops which called outer loop and inner loop. In peak current-mode control, either the switch current or inductor current must be sensed accurately. The current sensing must be very wideband to accurately reconstruct the current signal. This is

the reason why voltage drop in current-mode control higher compared to voltage-mode control, where voltage-mode control only have single feedback loop.

The comparison between value of inductor current ripple and output voltage ripple is one of the main objectives in this project. From the simulation result, it is shown that output voltage ripple of peak current-mode control is less compared to voltage-mode control. This result same goes to value of inductor current ripple. The type of controller itself plays a role in determining whether the ripple is low or high. In peak current-mode control looks like a single-pole system at low frequencies since the inductor has been controlled by the current loop. This improves the phase margin and makes the converter much easier to control compared to voltage-mode control.

Output voltage ripple percentage of peak-current mode control is less than voltage-mode control. This is good for peak current-mode control to have small ripple voltage because ripple voltage is a small unwanted residual periodic variation of the direct current output of supply. If the controller have high ripple voltage, that's mean the controller is not good. Peak current-mode control is almost constant in the region of crossover frequency which give this controller major advantage that allowing the power stage to operate much efficiency. From this advantage, peak current-mode control gets more stable compared to voltage-mode control, where cause the inductor current ripple and output voltage ripple in voltage-mode control is higher than peak current-mode control.

This project only focuses on the close-loop circuit with the stable and fixes input voltage and output voltage. Although the purpose of close-loop circuit is to regulate the unstable input voltage and stable output voltage, it was not testing in this project as the objective focus on to do comparison of performance between peak current-mode control and voltage-mode control in term of output voltage ripple and inductance current ripple.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

This chapter is the final chapter that has summarized all the topics that have been realized in the previous chapters. In addition to this chapter, some recommendation for future on this project is also included.

5.1 Conclusion

In a nut shell, this project had successfully achieved its main objective which is to study about buck converter, compare the inductor current ripple and output voltage ripple between two types of controllers which are peak current-mode control and voltage-mode control. The main activity in Final Year Project I is to design the buck converter circuit. Buck converter concept can be concluded as buck converter generally drops the value of output voltage against the value of given input voltage. Next activity is to simulate the buck converter circuit under open loop condition without compensator or also known as power stage circuit. To design and do simulation, knowledge about buck converter, current-mode control, peak current-mode control, voltage mode control and the compensator are required. All the theory was gained from process called literature review. Upon completing the chapters on introduction and literature review, proceed to designing buck converter circuit by using mathematical solution.

The next step is to get all value of suitable parameters, start designing buck converter circuit by using Pspice simulation software. The preliminary result detected a high inductance current ripple. To overcome the high inductance current ripple, value of the inductor and capacitor has been changed. An assumed value (derived from other sources) was used instead of the calculated to obtain a better result within the theoretical limit. It can be concluded for the above that inductance current ripple can be controlled by the inductor current which was controlled by the inductor value. Finally in the open loop condition, the output could not function automatically because value of the duty ratio is fix which was derived from the mathematical calculation.

In closed loop circuit, it is required to have a compensator circuit. This is because the original filter buck converter must be increased cause of it has very low phase margin. In this project, type-II compensator has been selected because this compensator is less complex in designing the circuit. Type-II compensator also gives a 90^{o} phase increased to the phase which placed symmetrically around the poles and zero of the desired loop crossover frequency.

The objectives of this project has been achieved by designing the peak current-mode control of buck converter, simulation of the peak current-mode control and voltage mode control of buck converter and by comparing the performance between peak current-mode control and voltage-mode control in term of voltage ripple and inductance current ripple. As a conclusion, inductor current ripple and output voltage ripple of peak current-mode control is less than voltage-mode control and proved that the peak current-mode control is more stable and accurate compared to voltage-mode control.

5.2 Recommendation

For peak current-mode control and voltage-mode compensator design, it was difficult to find the optimize crossover frequency value. In order to get crossover frequency value, it must assume a value of switching frequency. In this project, the chosen value of switching frequency is 100 KHz. In try and error process, frequency response of 100 KHz and 50 KHz does not have much different. It is recommended that to produce one method to find the optimize crossover frequency without need to assume switching frequency value. In this project, it was only focus on stable and fix input voltage and output voltage of buck converter. It was not focus on testing the circuit under unstable condition. It is recommended to continue this close-loop circuit operates under unstable input condition. As in this project only focus simulation analysis on peak current-mode control and voltage-mode control of buck converter, it is recommended to continue and proving the peak current-mode control is better than voltage-mode control in term of output voltage ripple and inductor current ripple through the hardware in future.

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