COMPARATIVE EVALUATION OF MODULATION ALGORITHMS FOR THREE-PHASE NEUTRAL POINT CLAMPED (NPC) MULTILEVEL INVERTER

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COMPARATIVE EVALUATION OF MODULATION ALGORITHMS FOR THREE-PHASE NEUTRAL-POINT-CLAMPED (NPC) MULTILEVEL INVERTER

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A report submitted in partial fulfilment of the degree of Electrical Engineer (Industrial Power)

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2013/2014

"I declare that this report entitle "Comparative evaluation of modulation algorithms for three-phase neutral point clamped (NPC) multilevel inverter" is the result of my own research except as cited in the references. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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ABSTRACT

This project gives a comparative evaluation of modulation algorithms for neutral point clamped (NPC), which is a multilevel inverter topology which converted DC sources to AC sources. Neutral point clamped topology is progressively applied in motor drive applications due to their low harmonic output and low switching losses. Nevertheless, higher number levels of NPC multilevel inverter topology and increasing number of semiconductor devices promotes the difficulty to balance capacitors' potential and raise the complexity of switching techniques involved. The important parameters of inverter such as total harmonic distortion (THD) measurements and voltage balancing are controlled by the adopted switching technique. Two switching modulation techniques have been proposed in this study, which are sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM), but the selection of switching technique is based on several key properties which are simple, flexible, and produce low harmonic output. Besides that, this project also presents comparisons between two-level conventional inverter, three-level NPC and five-level NPC. The simulation will done using MATLAB/Simulink. Maintaining the THD level as low as possible is very crucial, because it would cost less effort on filtering. The percentages of voltage THD can be lessened by increasing the modulation index. Besides that, the implementation of SPWM is easier but the THD level is higher, than SVPWM.

ABSTRAK

Projek ini adalah perbandingan penilaian algoritma modulasi untuk titik neutral diapit (NPC), ia merupakan topologi penyonsang bertingkat yang menukar sumber arus terus kepada sumber arus ulang-alik. Kebanyakkan aplikasi topologi titik neutral diapit digunakan dalam aplikasi-aplikasi pemacu motor disebabkan oleh harmonik keluaran yang rendah dan kehilangan pensuisan yang rendah. Walau bagaimanapun, pertambahan tingkat bagi topologi titik neutral diapit dan peningkatan jumlah peranti semikonduktor akan menghadapi masalah keseimbangan potensi kapasitor dan meningkatkan kerumitan teknik pensuisan. Parameter penting dalam penyongsang bertingkat adalah jumlah herotan harmonik (THD) dan keseimbangan voltan adalah dikawal oleh teknik pensuisan yang digunakan. Dua teknik modulasi pensuisan telah dicadangkan dalam kajian ini, iaitu modulasi bentuk lebar denyut sinus (SPWM) dan modulasi lebar denyut vektor ruang (SVPWM). Pemilihan teknik pensuisan adalah berdasarkan beberapa ciri-ciri iaitu kesederhanaan, fleksibiliti, dan menghasilkan keluaran harmonik yang rendah. Selain itu, projek ini juga akan menunjukkan perbandingan antara penyongsang dua tingkat konvensional, tiga tingkat NPC dan lima tingkat NPC. Simulasi tersebut akan dilakukan dengan menggunakan MATLAB/Simulink. Mengekalkan tahap THD yang serendah yang mungkin adalah sangat penting, kerana ia akan mengurangkan kos yang melibatan penapis. Peratusan voltan THD boleh dikurangkan dengan meningkatkan indeks pemodulatan. Di samping itu, pelaksanaan SPWM adalah lebih mudah namun mempunyai tahap THD yang lebih tinggi daripada SVPWM.

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NOMENCLATURE

DC	Direct current
AC	Alternative current
MLI	Multilevel inverter
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
NPC	Neutral point clamped multilevel inverter
FC	Flying capacitor multilevel inverter
CHB	Cascaded H-bridge multilevel inverter

CHAPTER 1

INTRODUCTION

1.1 Motivation

The applications of the inverter have become widely used in all aspects during this modern generation, including home appliances, renewable energy field, and industry field. Due to advance of science and technology, emphasizes on green technology had grown rapidly. Hence, more research has been focused on renewable energy. The renewable energy gained from natural environment is needed to transmit back to national grid; inverter plays a very important role to convert the DC renewable source to AC grid source. Currently, engineers have to work harder on the investment of the high efficiency and low harmonic distortion inverters. The design of inverters involved many circuit theory, switching control theory, control processors, and knowledge on power electronics. Advances in power electronics elements with the suitable switching control method will come out desired outputs that guarantee the efficiency and performance of the inverter. It ensures encourages fast growing on good performance technology.

In this study would mainly concentrate on multilevel inverter neutral point clamped (NPC) topology. Operation and performance of every kind of inverter depend on the switching control modulations that been adopted. The switching control modulation that proposed in this study to control the three-phase NPC multilevel inverter are sinusoidal pulse width modulation (SPWM) and space vector pulse-width modulation (SVPWM).

1.2 Problem Statement

Inverters are electronics device that converts the DC source to AC source. Inverters have proven their great benefits on industrial field such as in power grid system to convert renewable source to power grid AC source. Without a doubt, applications of inverter had experienced rapid growth in the past few decades.

However, due to higher harmonic contents and switching losses of conventional inverter, three main multilevel inverter topologies have been widely reviewed, which are neutral point clamped inverter (NPC), cascaded H-bridge inverter and flying capacitor inverter. Neutral point clamped particularly adopted in motor drive application.

The main advantages of the NPC inverter are improving output voltage waveform quality and less output current ripple, which mean less effort required for filtering. The major drawbacks of NPC are increasing number of switches and semiconductor, and thus increase overall costs and control complexity.

The biggest concern of neutral point clamped inverter is the capacitor voltage imbalance problem, which may cause over-voltages of the switches and increase overall harmonic content and switching losses. Suitable control algorithms have to imply to balance the capacitor DC voltage.

1.3 Objectives

The objectives of this project are:

1) To study modulation methods based on multicarrier pulse-width modulation and space vector pulse-width modulation.
2) To solve the neutral point clamped (NPC) voltage imbalance problem.
3) To compare the adopted performances of inverter (in terms of THD) with two-level conventional inverter.

1.4 Scope

- Analysis performance of conventional inverter and neutral point clamped inverter in term of their voltage imbalance problem, and THD by using MATLAB/Simulink.
- Simulation and modelling process by using MATLAB/Simulink with using different switching techniques to obtain inverters output waveforms
- Performance of inverters with different switching techniques will be analyses and compared with varied switching frequency from 1 kHz to 5 kHz and modulation index from 0.5 to 1.0

CHAPTER 2

LITERATURE REVIEWS

2.1 Introduction

Multilevel inverters having an unshakable position in this industrial field and become an inevitable equipment in most of the applications. This chapter would discussed about the general inverter topologies, such as two-level conventional inverter, neutral point clamped (NPC) multilevel inverter, flying capacitor (FC) multilevel inverter, cascaded H-bridge (CHB) multilevel inverter and asymmetric hybrid multilevel inverter. Asymmetric hybrid multilevel inverter having unique characteristics, as it will combine the advantages of each combine topologies. Besides that, this chapter would also discussed relevant control switching modulation for these inverter topologies; sinusoidal pulse-width modulation (SPWM), space vector pulse-width modulation (SVPWM), and selective harmonic elimination (SHE). Different control switching modulation with different topologies would produce different output power quality. Finally, in this chapter extra attention would pay on the latest application of the multilevel inverters technologies, such as application of inverter in renewable energy field, and adjustable speed device.

2.2 Inverters

Nowadays, multilevel inverters are gained intense attention in the electrical field due to its advantages of lower power dissipation in power switches, low harmonic and low electromagnetic interference outputs [3]. Inverters are the devices used to generate AC voltage from constant DC voltage. Multilevel inverter is the circuit can produce more output voltage

level compare with the conventional inverter. An additional voltage levels is to smoother the output waveform, thus lower the total harmonic distortions [4]. In other words, multilevel inverters are categories as the output levels that are more than two. There are several famous multilevel inverters topologies that are used in industry, which are neutral point diode clamped multilevel inverter (NPC-MLI), flying capacitor multilevel inverter (FC-MLI), cascaded H-bridge multilevel inverter (CHB-MLI) and asymmetric hybrid multilevel inverter. The first three types are the most common inverter; meanwhile the asymmetric hybrid multilevel inverter is the combination of various types of inverter. The applications of the inverters have enhanced tremendously especially in the field of renewable energy sources and motor drives applications. For example, the original energy that being collected from PV solar cells is in the DC sources form, but the energy feed into national grid must in AC sources form [1].

2.2.1 Two-Level Conventional Inverter

Nowadays, due rapid develop in power electronics field, multilevel inverters which being led to higher-level are available in market. The origin design of these multilevel inverters is based on two-level conventional inverter as shown in Figure 2.1. This topology has two advantages compared to multilevel inverter. The first advantage that is very obvious and can be easily observed in two-level conventional inverter is less switching devices needed, thus easier control the switching modulation. The second advantage is conventional inverter does not facing any DC-link voltage imbalance problem as faced by multilevel inverter [5]. However, this topology has a defeat which is higher harmonic content and makes it less suitable to sensitive devices. Two-level conventional inverter can only generate two output stages, ½ V_{dc} and – ½ V_{dc} as can be seen in Figure 2.2 [6]. With multilevel inverter, the output can be three level, five level or other higher levels. The phase output of three levels is + ½ V_{dc}, 0, - ½ V_{dc}, meanwhile the output of the five levels is + ½ V_{dc}, + ¼ V_{dc}, 0, - ¼ V_{dc}, and – ½ V_{dc} as illustrated in Figure 2.3. The upper switch and lower switch in one leg are work in complementary manner, which is when the lower switch is turned on and the upper switch must in turned off modes. There are no a single moment for both of switches in one leg are turned on or turned off, or else the DC supply would be shorted [7].

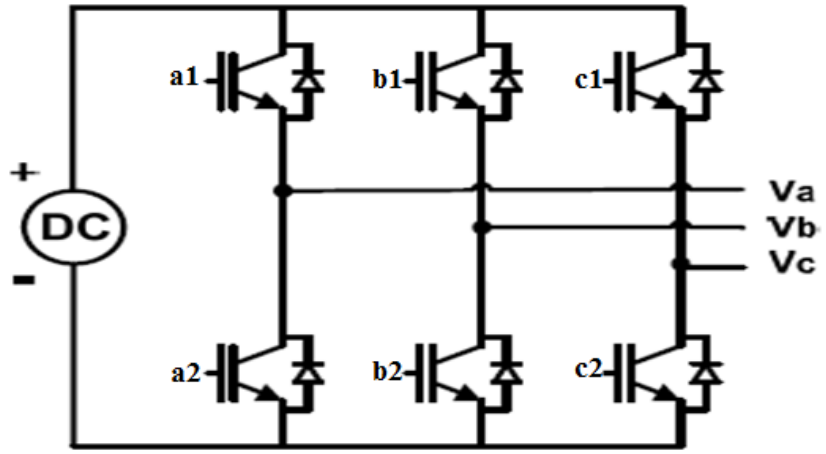
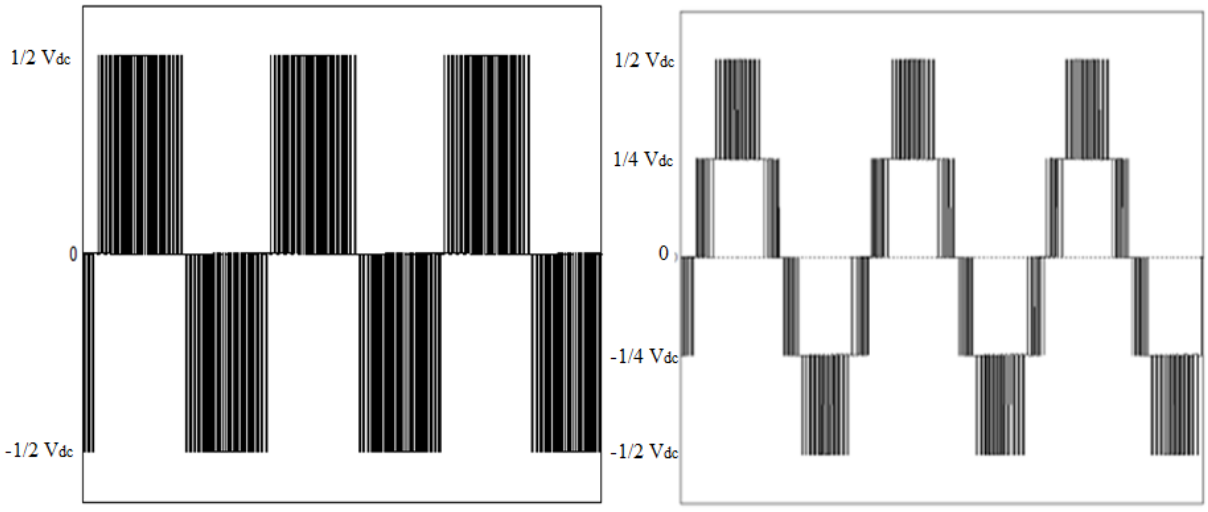


Figure 2.1: Schematic diagram of two-level conventional inverter

Figure 2.2: Phase voltage of two-level conventional inverter



(a) Three-level (b) Five-level

Figure 2.3: Phase voltage output waveform of multilevel inverter

2.2.2 Neutral Point Clamped Multilevel Inverter

Neutral point clamped (NPC-MLI) multilevel inverter was introduced by A. Nabae, I. Takahashi and H. Akagi in 1980 [3]. Multilevel inverters have become common and popular in medium voltage high-power applications. The NPC-MLI utilized several DC capacitors and clamping diodes to produce AC waveforms with multiple levels. Major advantages of NPC-MLI compared to two-level conventional inverter are improving power quality in terms of THD, and reduce the switching losses [9]. However, NPC-MLI still received a lot of attention from researcher due to the dc-link voltage imbalance problem. The DC input sources must divide equally between the series DC capacitors; the imbalance voltage between series DC capacitors would increase distortion of output waveforms. Figure 2.4 shows the three-level NPC inverter. Three-level NPC inverter consists of two series dc-link capacitors, four IGBTs connected in series and two clamping diodes in one phase [31].

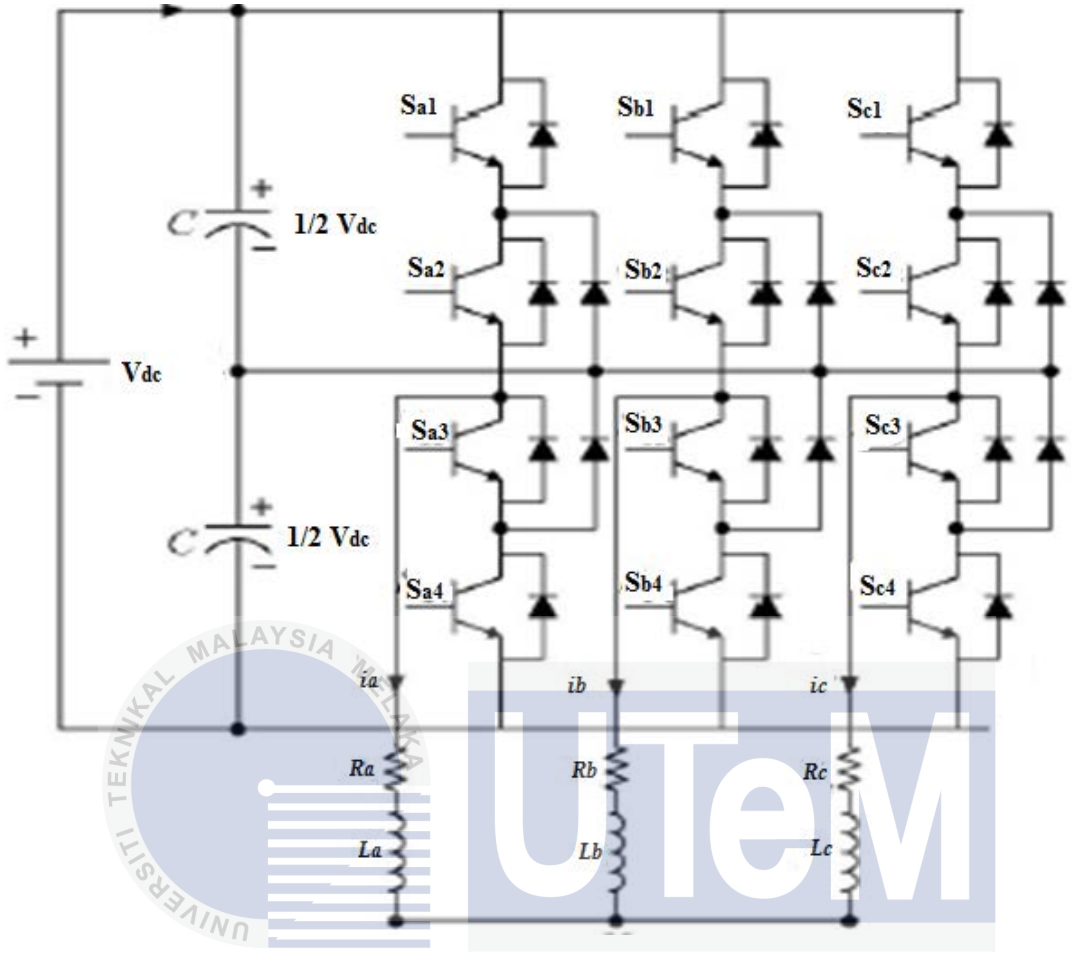


Figure 2.4: Schematic diagram of three-level NPC-MLI

The number of capacitors, N_c used depends on the number of output voltage levels of the inverters as given in Equation (2.1), where n is number of voltage level. The voltage across each capacitor, V_c must be balanced according to Equation (2.2).

$$\text{Number of capacitor in NPC, } N_c = (n - 1) \tag{2.1}$$

$$V_c = \frac{V_{dc}}{N} \tag{2.2}$$

As illustrated in Table 2.1, three possible switching states, P, O, N can occurs in each phase. When the upper two IGBTs, S_1 and S_2 are switched ON, the switching state is P. Then, when the middle two IGBTs, S_2 and S_3 are switched ON, the switching state is O. Later, when the lower two IGBTs, S_3 and S_4 are switched on, the switching state is N. Switches S_1 and S_3 are work in complementary manner. With one switched ON, the other switched must be switched OFF. Same operations work on switches S_2 and S_4 [32].

Table 2.1: Switching state of three-level NPC-MLI

Switching state	S_1	S_2	S_3	S_4	Output voltage
P	On	On	Off	Off	½ V_{dc}
O	Off	On	On	Off	0
N	On	On	Off	Off	-½ V_{dc}

The schematic diagram of five-level NPC-MLI is shown in Figure 2.5. In five-level NPC-MLI, each capacitor is rated at $\frac{V_{dc}}{4}$, and the phase output has five voltage levels; $\frac{V_{dc}}{4}$, $\frac{V_{dc}}{2}$, 0, $-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{4}$, depending on the combinations of switches operation. With increases in voltage levels, the complexity of the switching control would also be increases, due to the number of semiconductor and switches required increased [3].

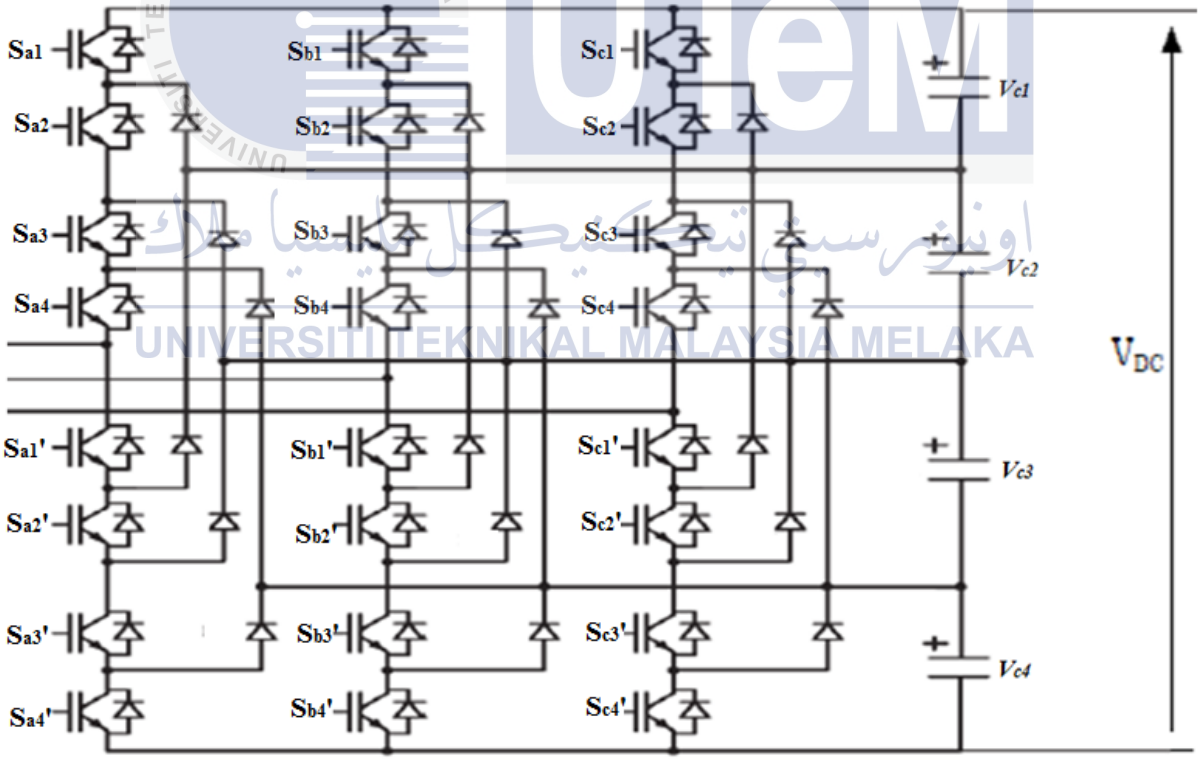


Figure 2.5: Schematic diagram of five-level NPC-MLI

The upper and lower switches of five-level NPC are work in complementary manner, which is when the S_1 in the upper side is switched on, the S_1' in the lower side is switched ON, the same operations of complementary manner would goes ON in other switches as illustrated in Table 2.2. The switches operation of five-level NPC-MLI is shown in Figure 2.6.

Table 2.2: Switching states of five-level multilevel NPC-MLI

S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	Output voltage
1	1	1	1	0	0	0	0	$\frac{V_{dc}}{2}$
0	1	1	1	1	0	0	0	$\frac{V_{dc}}{4}$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-\frac{V_{dc}}{4}$
0	0	0	0	1	1	1	1	$-\frac{V_{dc}}{2}$

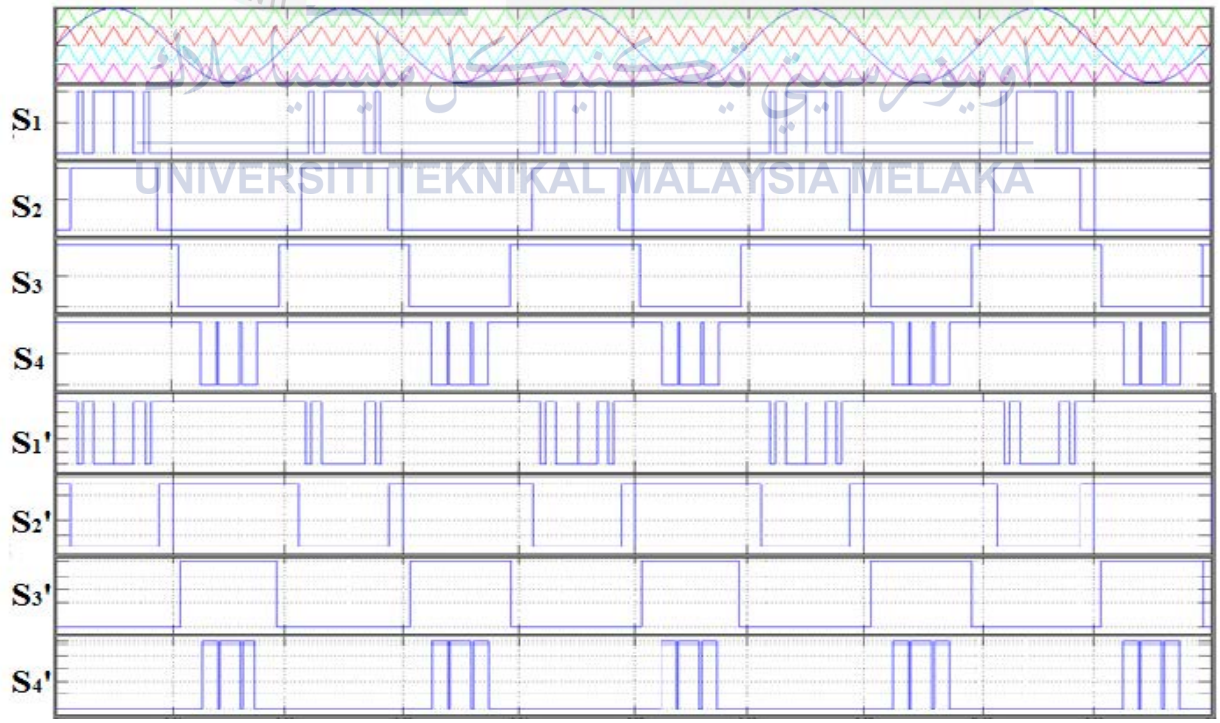


Figure 2.6: Switches operations of five-level NPC-MLI

The output voltage of five-level NPC-MLI are involved in more staircase form and the harmonics content of the five-level NPC-MLI is said to be minished. Though the harmonic content is being minished but a large number of IGBTs switching devices is needed and thus directly increase the design cost.

2.2.3 Flying Capacitor Multilevel Inverter

Flying capacitor inverter (FC-MLI) is introduced by Meynard during 1992. This type of inverter is almost similar with NPC-MLI, just the clamping diode of the NPC-MLI replaces with DC capacitors in FC-MLI as shown in Figure 2.7 [3].

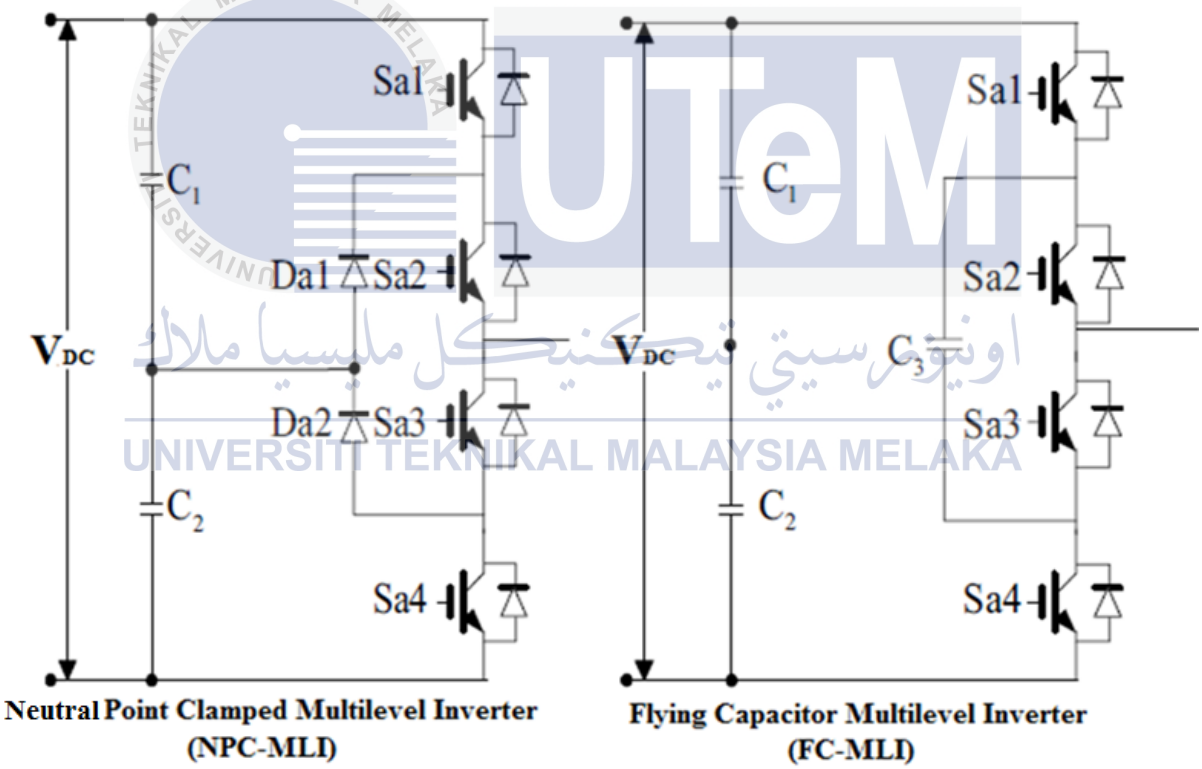


Figure 2.7: Difference between FC-MLI and NPC-MLI

Hence, capacitors in this topology can be categories into two parts, first part is the DC-link capacitors and second part is the auxiliary capacitors. The number of DC-link capacitor needed in *n*-level FC-MLI multilevel inverter can be calculated by using formula (*n* - 1). In the

other hand, the number of auxiliary capacitors, N_c need in m-level FC-MLI multilevel inverter can be calculated by using Equation (2.3).

$$N_c = (n - 1)(n - 1) / 2 \quad (2.3)$$

This topology do not involves in any serious problem that faced by other multilevel inverter, such as the voltage sharing problem in cascaded H-bridge multilevel inverter and DC-link imbalance problem in NPC-MLI [15].The most important advantages of this topology are provided with phase redundancies ability that can balanced the capacitor voltage by selecting suitable charging and discharging switching states, and the second advantage is reduced the filter requirement. However, the increase in output voltage levels would require additional great amount of capacitors and restrain the accurate of capacitor charging and discharging [18]. The major drawback of this topology is the cost of the inverter will increase due to the number of capacitors used increases and directly influenced the size of the device is become larger [3]. Figure 2.8 shows the topology of single-phase five-level FC-MLI. Similar to NPC-MLI, the upper and lower switches are work in complementary manner, which is when the S_1 in the upper side is switched on, the S_1' in the lower side is switched on, and the same operations of complementary manner would goes on in other switches [17]. The charging and discharging of auxiliary capacitors (C_1, C_2, and C_3) are used to change the voltage levels into ¼ V_{dc}, ½ V_{dc}, and ¾ V_{dc}[18].

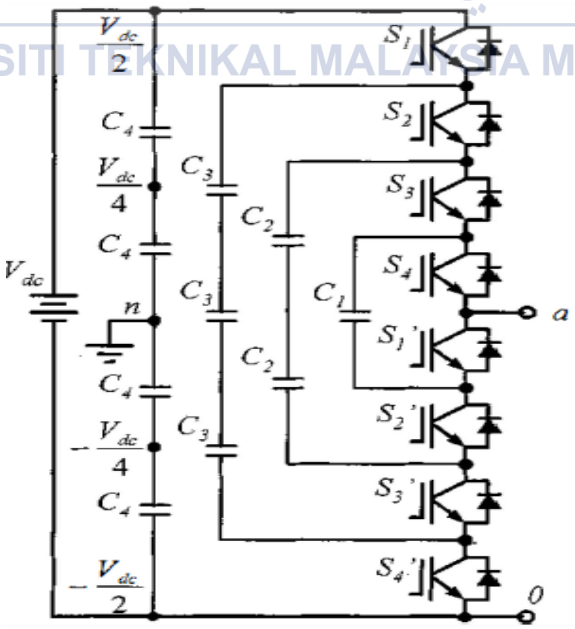


Figure 2.8: Single-phase of five-level FC-MLI

2.2.4 Cascaded H-Bridge Multilevel Inverter

Cascaded H-bridge (CHB-MLI) is the topology that required less power to operate compared with the NPC-MLI and FC-MLI. The basic significance of CHB-MLI that differs from other inverter topologies is the DC input sources must be separated from one another but having redundant switching combinations in order to produce high quality multilevel output voltage. CHB-MLI has been widely used in applications with input sources is coming from several energy resources. (i.e. fuel cells, photovoltaic arrays) and transmitting AC electricity to national grid or AC load CHB-MLI can produce a more staircase form output with low switching losses and high conversion efficiency by using low power semiconductor devices [19-22]. The cells contained in a phase depend on the design of inverter. A cell is combination of four switch, S_{11}, S_{12}, S_{21} and S_{22} as seen in Figure 2.9. To obtain V_{dc}, switch S_{11} and $S_{22}$are turned on, to obtain 0V, switch S_{11} and S_{21} or switch S_{12} and S_{21}. The switching states of the inverter can determine by Equation (2.4). Where l is the number of output levels [3].

$$\text{Switching state, sw} = 3^{l} \tag{2.4}$$

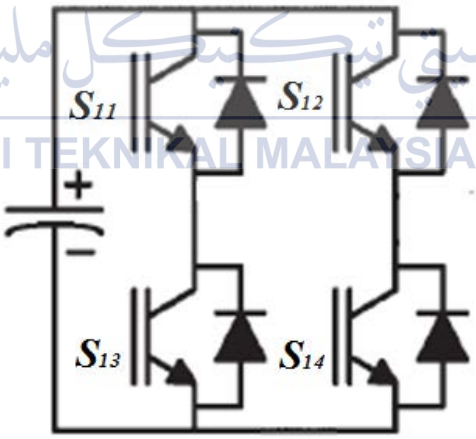


Figure 2.9: Single cell of H-bridge inverter

Figure 2.10 shows a diagram schematic of three-phase five-level CHB-MLI. Each cell in the inverter having a separated DC-link voltage source, the total output that generated is sum of the separated DC-link voltage sources. The number of level, l can be calculated by using Equation (2.5), where c is the number of cell existed in CHB-MLI.

Number of levels, $l = 2c + 1$ (5)

However, there are still a lots of problem need to be overcome in this topology. When the number of output levels voltage is increases, the number of switches required is increases and thus increases the complexity of switching and conduction loss of devices. This will have negative impact on cost, efficiency and reliability, since reliability is inversely proportional to number of components existed in inverter.

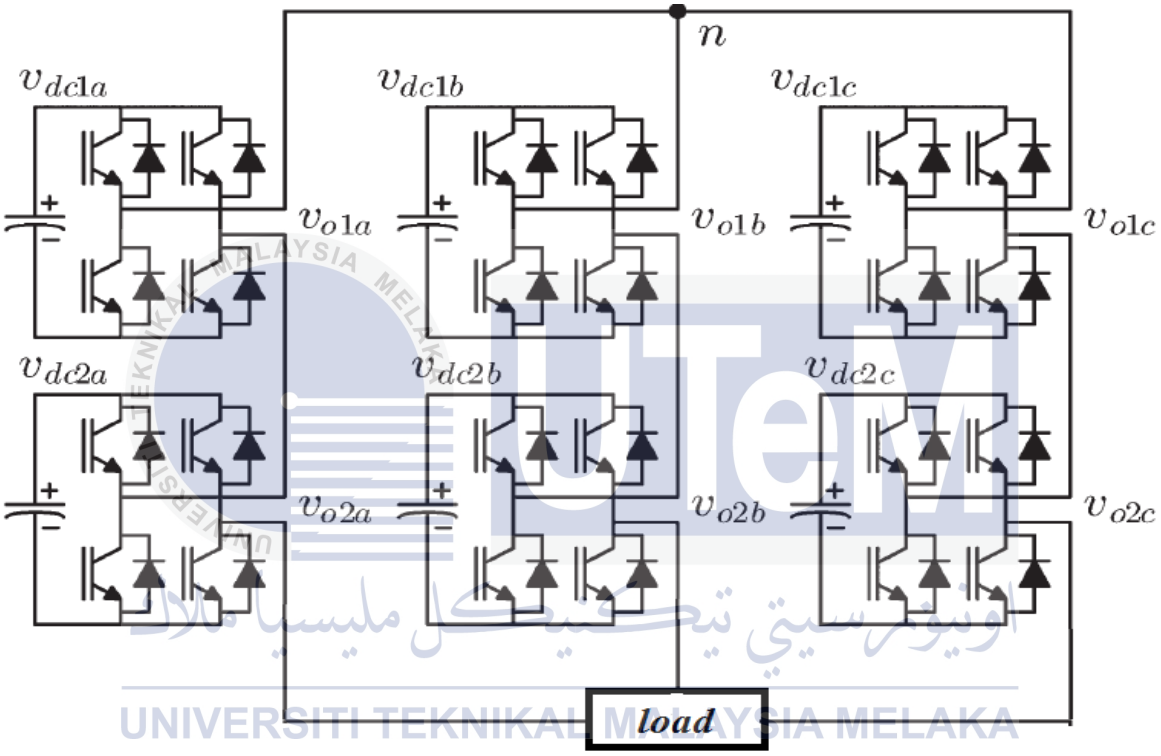


Figure 2.10: Schematic Diagram of three-phase five-level CHB-MLI

2.2.5 Other's Multilevel Inverter Topologies

The meaning of hybrid MLI is the combinations of the conventional multilevel inverter topologies, such as NPC-MLI, FC-MLI and CHB-MLI, to form a new type multilevel inverter topology [3]. Nowadays, many combinations have been proposed, such as NPC-CHB inverter, ANPC-CHB inverter, and FC-CHB inverter. Increase in output voltage levels of conventional MLI would involve in the problem of DC-link balancing problem in NPC-MLI, capacitors size

of FC-MLI, and increase number of separated input sources in CHB-MLI. The advantage of this combination is to combine different advantages of the common inverter topologies in order to reduce the harmonic content and switching losses of the MLI. Normal sinusoidal pulse-width modulation is not suitable for hybrid MLI, the suitable switching modulation are able to provide higher power switching at low frequency and low power switching at high frequency [26].

2.2.5.1 Hybrid Cascaded H-Bridge Multilevel Inverter (HCHB-MLI)

To reduce the required number of DC supplies when CHB-MLI is applied to an induction motor, a hybrid MLI design topology has been proposed. The hybrid MLI uses a single source and capacitors for the remaining sources in CHB-MLI topology. The proposed hybrid cascaded H-bridge multilevel inverter (HCHB-MLI) topology is shown in Figure 2.11. This proposed hybrid MLI is constructing from a three-phase conventional inverter by cascading with single-phase H-bridge inverter in each phase. This topology using the concept of replacing the isolated input source with capacitors and the operating sources is feeding from the legs of two-level conventional inverter [25].

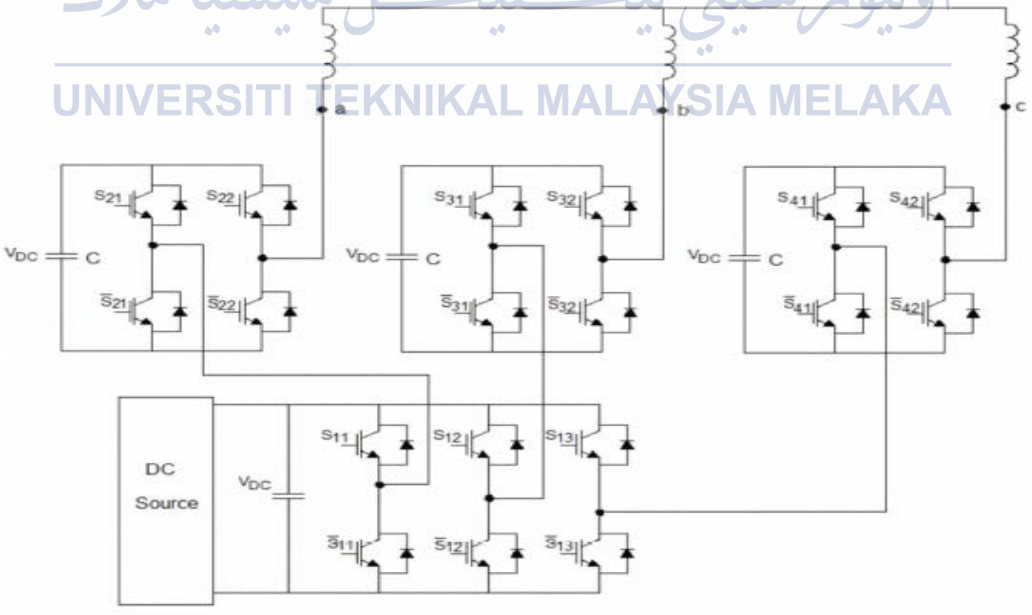


Figure 2.11: HCHB-MLI with single input sources

2.2.5.2 Active Neutral Point Clamped (ANPC)

FC-MLI and NPC-MLI are the types of topologies that used in motor application due to its characteristics of single input sources. NPC-MLI is more widely in high power industrial field compared with FC-MLI due to its size. However NPC-MLI has a major drawback of imbalanced DC-link distribution. In order to resolve this defect, a new multilevel inverter topology called active neutral point clamped has been proposed as shown in Figure 2.12 [85]. The two clamp diodes in NPC-MLI are replaced by IGBT switching devices [84-88]. Due to the increases in switching devices thus the switching states are increased to allow more than one switch state to have zero states. The advantage of ANPC is having benefits of FC-MLI but is in NPC-MLI form, hence the size is reduced because does not involve any capacitor [84].

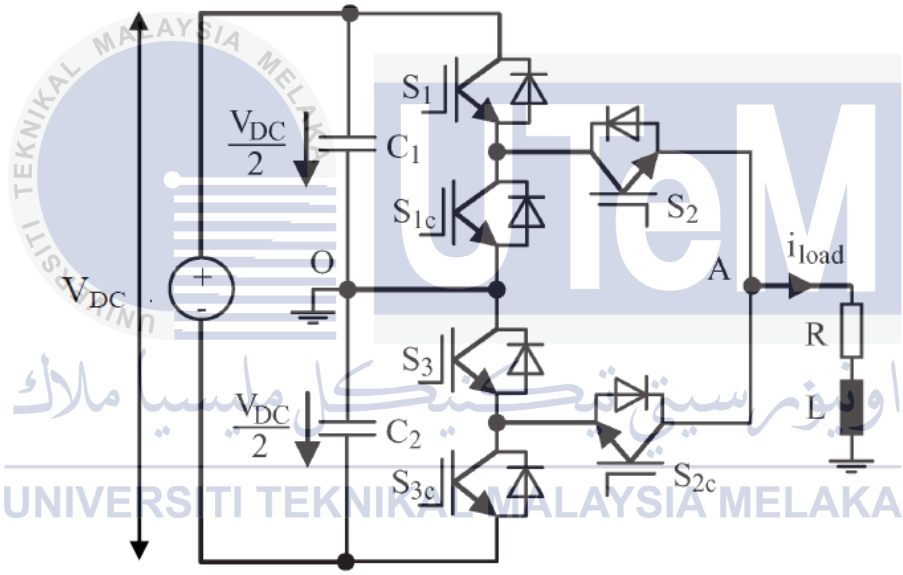


Figure 2.12: Single-phase three-level ANPC converter

2.2.5.3 Hybrid Five-level Multilevel Inverter

Every multilevel inverter has its own merit and demerit. FC-MLI do not involved in DC-link imbalanced problem but involved in large number of capacitors required. NPC-MLI do not involved sizing problem but do involved in balancing problem. CHB-MLI has the advantages of minimum size compared to FC-MLI and NPC-MLI, but faced the problem of isolated DC-input sources. A new multilevel inverter named hybrid five-level multilevel inverter has been

proposed as shown in Figure 2.13, cascading a three-level FC-MLI with CHB-MLI. The main advantage of this topology is improved the reliability of the circuit, since the whole circuit still functions, even one of the H-bridge is fail [89].

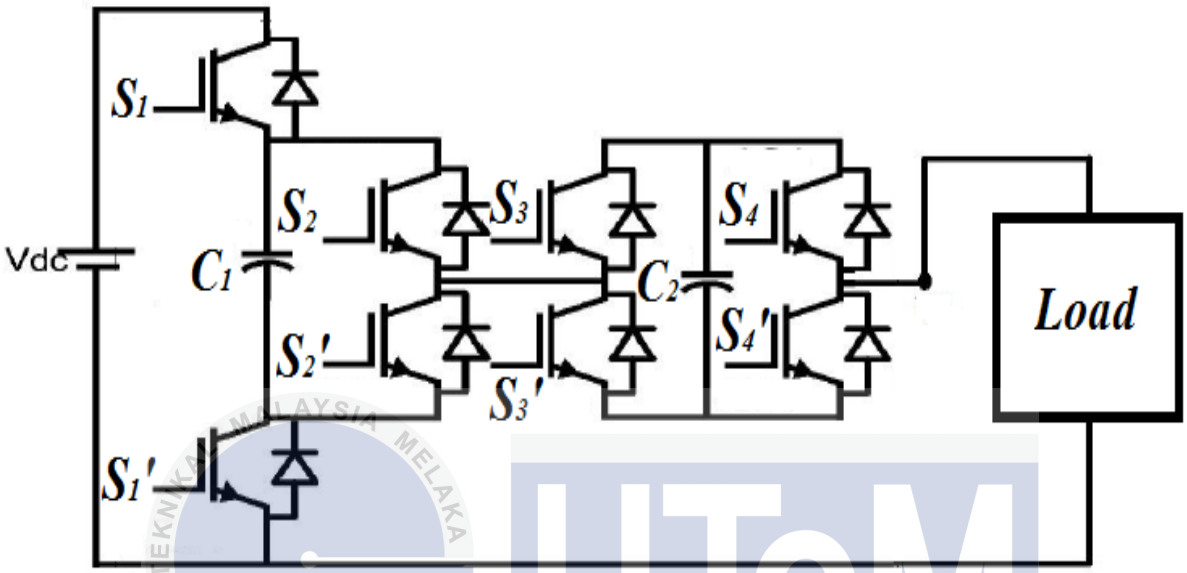


Figure 2.13: Hybrid five-level multilevel inverter

2.3 Control Switching Modulation

The important parameters of the inverter, such as switching losses, harmonic content and balancing are depend on the adopted switching modulation. There are three basic switching modulation that have been widely used are space vector pulse-width modulation (SVPWM), selective harmonic elimination (SHE-PWM) and sinusoidal pulse-width modulation (SPWM). SVPWM, and SPWM are belong to open-loop switching modulation. SPWM and SVPWM are belong to high switching frequency methods which is switching frequency higher than 1 kHz; while the SHE-PWM is low switching frequency methods which is lower than 1 kHz and normally range in 50 Hz and 60 Hz. Among these three types switching modulation, SPWM is the most ordinarily and simplest switching modulation. Meanwhile, SVPWM is considered as most complex switching modulation.

2.3.1 Sinusoidal pulse-width modulation (SPWM)

Sinusoidal pulse-width modulation (SPWM) is the switching modulation that has been attracts general attention due to its simplicity. This switching modulation would not increase the complexity of the switching even the number of level output is increase. SPWM is a type of signal that used to control the switching in inverter. The basic concept of sinusoidal pulse width modulation is to compare a desired output frequency sinusoidal waveform (modulation signal) with high frequency triangular waveform (carrier signal). Comparator is a device used to compare the modulation signal with carrier signal, and the output is used to control inverter switches. In hardware practical, the comparator used can based on basic single-ended op-amp circuit, which has one inverting input, one non-inverting input and an output. In two-level inverter comparator shown in Figure 2.14, the modulation signal is fed to the non-inverting input terminal and the carrier signal is fed into the inverting terminal [43].

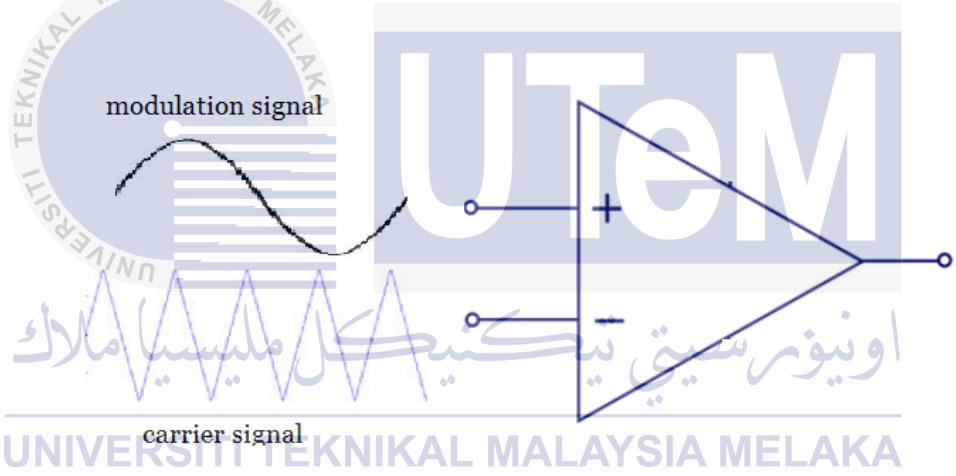


Figure 2.14: Comparator of two-level inverter

Comparator of two-level inverter above compares the sinusoidal signal to triangular signal and controls upper legs switch and lower legs switches based on the results of the test. The comparator's output will be turned on if the sinusoidal signal is exceeds the triangular signal and the upper leg switch is turn on and lower leg switch is turn off [44]. The upper leg and lower leg of inverter operates in complementary method to avoid possible short circuit during switching transients and thus when upper leg switch is turned on, then lower leg is turned off. Figure 2.15 shows the operation of sinusoidal wave and triangle wave works with a comparator. When $V_{sin} > V_{tri}$, output is '1', when $V_{sin} < V_{tri}$, output is '0'.

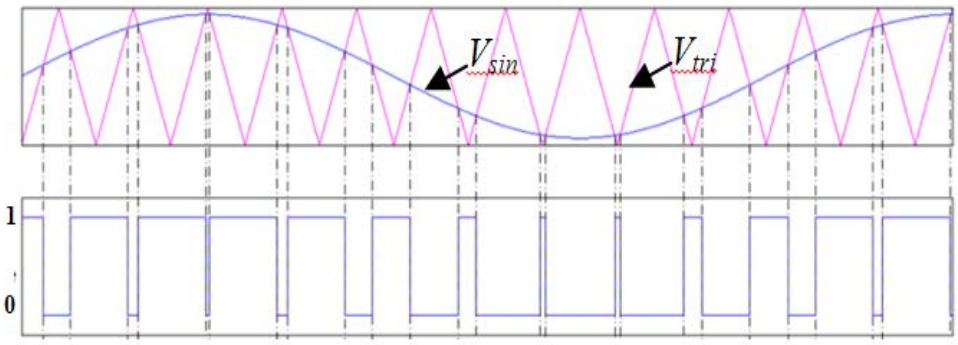


Figure 2.15: Operation of sinusoidal wave and triangle wave

The output of the inverter can be controlled by amplitude modulation, m_a and frequency modulation m_f. Amplitude modulation is the ratio of amplitude of modulating signal, V_{sin} to amplitude of carrier signal, V_{tri}as shown in Equation (2.6); while frequency modulation is the ratio of modulating frequency, f_{sin} to carrier frequency, f_{tri} as shown in Equation (2.7) [31].

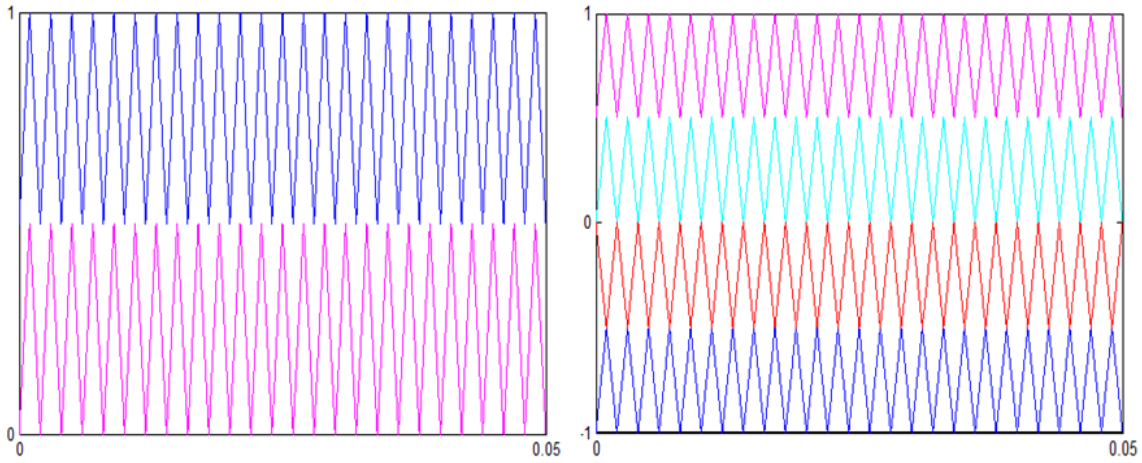
$$\text{amplitude modulation}, m_a = \frac{V_{sin}}{V_{tri}} \quad (2.6)$$

$$\text{frequency modulation}, m_f = \frac{f_{sin}}{f_{tri}} \quad (2.7)$$

The number of carrier signal, *l* adopted depends on the number of level output voltage that designed as given in Equation (2.8), where *n* is number of voltage level. Two-level of SPWM used only one carrier triangle signal, three-level of SPWM used two carrier triangle signals, and five-level of SPWM used four carrier triangle signals as shown in Figure 2.16.

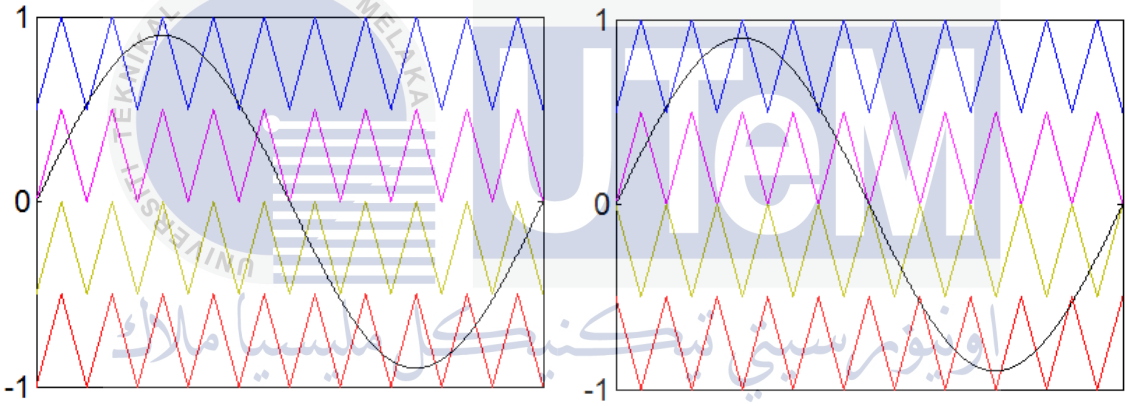
$$\text{Levels of carrier signal required, } l = (n - 1) \quad (2.8)$$

Multicarrier sinusoidal pulse-width modulations (MSPWM) are the method that derived from two-level version and used in the over than two-level multilevel inverter. The common used of MSPWM are phase disposition (PD), phase opposition disposition (POD), alternative phase of disposition (APOD) and phase shift (PS) as shown in Figure 2.17 [8].

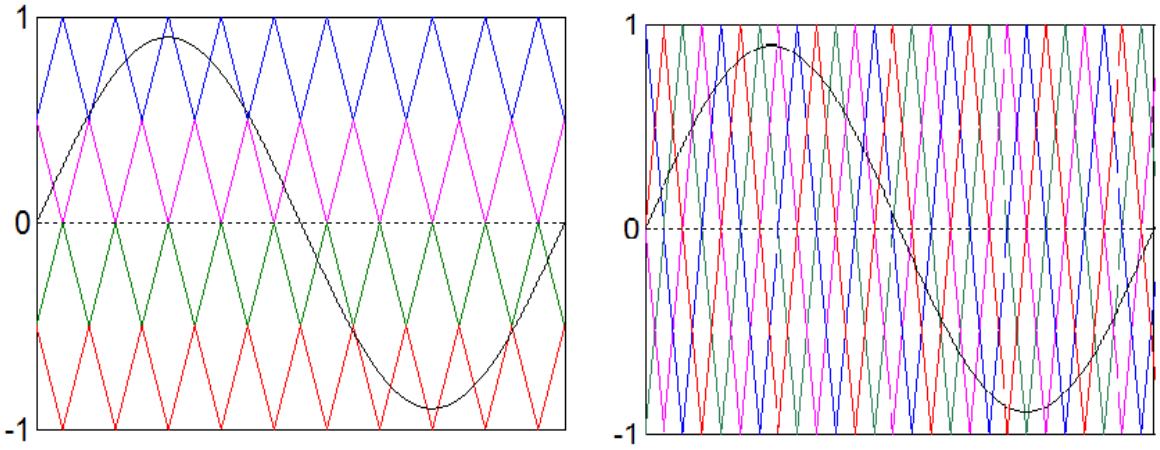


(a) Three-level SPWM (b) Five-level SPWM

Figure 2.16: Number of level of SPWM



a) PD b) POD



c) APOD d) PS

Figure 2.17: MSPWM control strategies

Multicarrier sinusoidal pulse-width modulation (MSPWM) been widely adopted in NPC-MLI, due to their simplicity. For *n*-level NPC-MLI, with MSPWM, the amounts of (*n*– 1) triangular carrier with the same amplitude and frequency have been used. By referring to Figure 2.16 (a), the operation of switches 1 and 3 of three-level NPC-MLI, depends on the comparison between upper carrier signal and the modulation signal. While, the operation of switches 2 and 4 are depends on the lower carrier signal.

2.3.2 Space Vector Pulse-Width Modulation (SVPWM)

The space vector pulse-width modulation (SVPWM) is the combinations of different switching states that based on the sector and vector existed. SVPWM is one of the famous switching modulations to control the switching of inverter, due to its efficiency and low harmonic content. The disadvantage of the SVPWM is when the required output level designed is increases; the complexity of the switching modulation SVPWM will also increase. The general idea of all level for SVPWM is the same, which is divided the hexagon into six equal areas called sector. However, with the number of output level increase, the number of small triangle is also increase as shown in Figure 2.18, and thus the selection of the switching states becomes more complex.

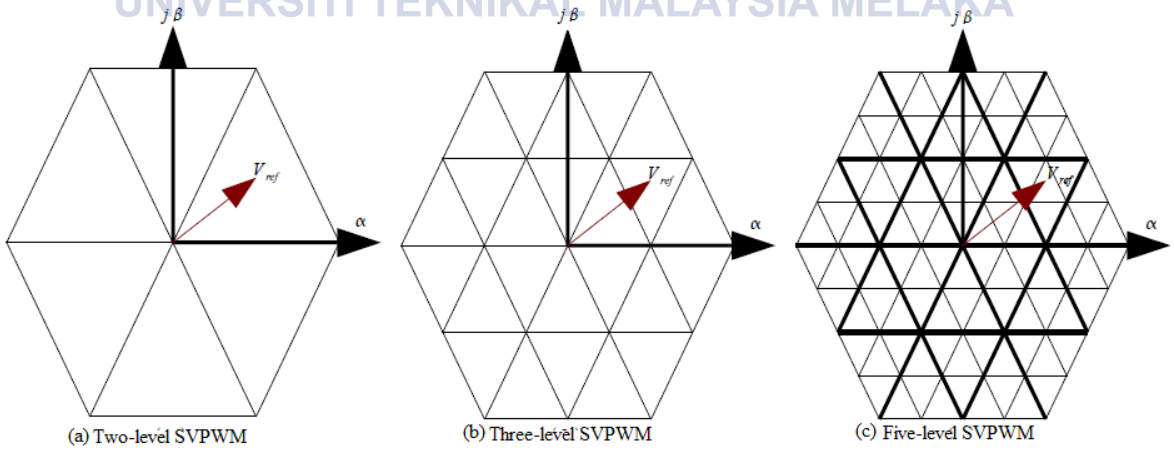


Figure 2.18: The hexagon and small triangle of different level

The hexagon of two-level SVPWM is shown in Figure 2.18 (a), which is the simplest configuration compared to other higher-level SVPWM, because it does not involved any small triangle in sector. The complexity of higher-level SVPWM increase is due to intricacy in determine the V_{ref} located on which small triangular in a sector. Two-level SVPWM only composes of eight possible states; inactive zero vectors and six active vectors. The hexagon is divided into six equal sectors, each sector of the two-level SVPWM control only by four vectors; two active vectors and two inactive vectors as shown in Figure 2.19. Interval angle of each sector is 60^0.

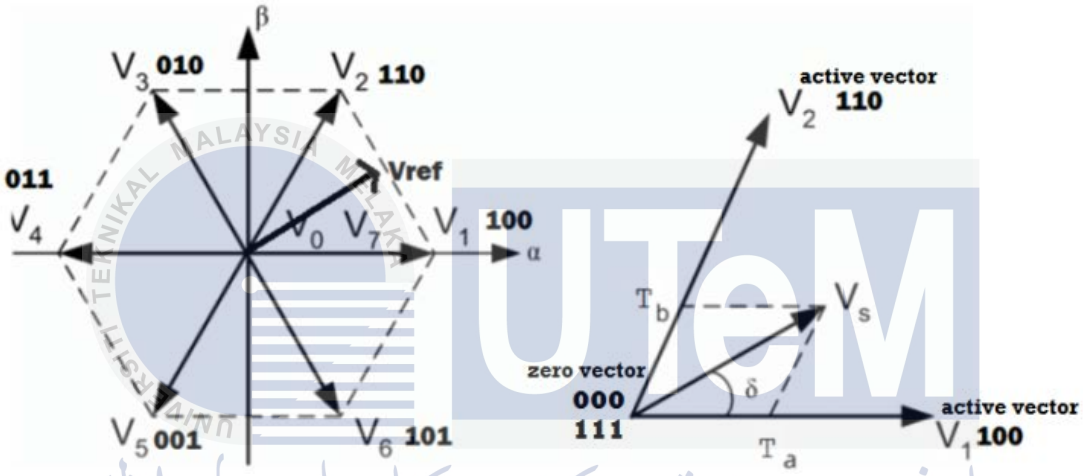


Figure 2.19: Eight vectors hexagon of two-level SVPWM

In two-level SVPWM, the summations of three reference signals are transformed into reference vector, V_{ref} and phase angle, θ. These two values can be calculated as Equation (2.9) and Equation (2.10), respectively. The sector on which V_{ref} laying is used to determine the switching states of the inverter. The V_{ref} rotate in angular velocity that equal to inverter output AC voltage frequency [34], and three phase inverter output rotating with angular speed by Equation (2.11). The magnitude of the active vector inverter output is $\frac{2}{3}V_{dc}$, and the phase voltage output is $\frac{2}{3}\pi$ from each other [35].

$$\theta = tan^{-1}\left[\frac{V_\alpha}{V_\beta}\right] = \frac{2\pi}{3} \tag{2.9}$$

$$V_{ref} = \sqrt{{V_\alpha}^2 + {V_\beta}^2} = \frac{2}{3}V_{dc} \tag{2.10}$$

$$\omega = 2\pi\, f_{ref} \tag{2.11}$$

According to which sector that contains of the V_{ref}, the ON/OFF switching time of inverter can be calculated by using Equation (2.12).

$$t_a = T_S \frac{3V_{ref}\sin(\frac{\pi}{3} - \theta)}{2V_{dc}\sin(\frac{\pi}{3})}$$

$$t_b = T_S \frac{3V_{ref}\sin(\frac{\pi}{3})}{2V_{dc}\sin(\frac{\pi}{3})}$$

$$t_c = \frac{T_S - t_a - t_b}{2} \tag{2.12}$$

The switches in Table 2.3 are working in complementary method for upper switches and lower switched, in order to get the output and avoid short circuiting. The inverter legs are switched in different vectors such the output voltage is shifted from one to another and hence producing the changes in waveform polarity as shown in Figure 2.20.

Table 2.3: Switching states for two-level inverter

S_a	S_b	S_c	V_a	V_b	V_c
1	0	0	$\frac{2}{3}\pi$	$-\frac{1}{3}\pi$	$-\frac{1}{3}\pi$
1	1	0	$\frac{1}{3}\pi$	$\frac{1}{3}\pi$	$-\frac{2}{3}\pi$
0	1	0	$-\frac{1}{3}\pi$	$-\frac{1}{3}\pi$	$\frac{2}{3}\pi$
0	1	1	$-\frac{2}{3}\pi$	$\frac{1}{3}\pi$	$\frac{1}{3}\pi$
0	0	1	$-\frac{1}{3}\pi$	$-\frac{1}{3}\pi$	$\frac{2}{3}\pi$
1	0	1	$\frac{1}{3}\pi$	$-\frac{2}{3}\pi$	$\frac{1}{3}\pi$

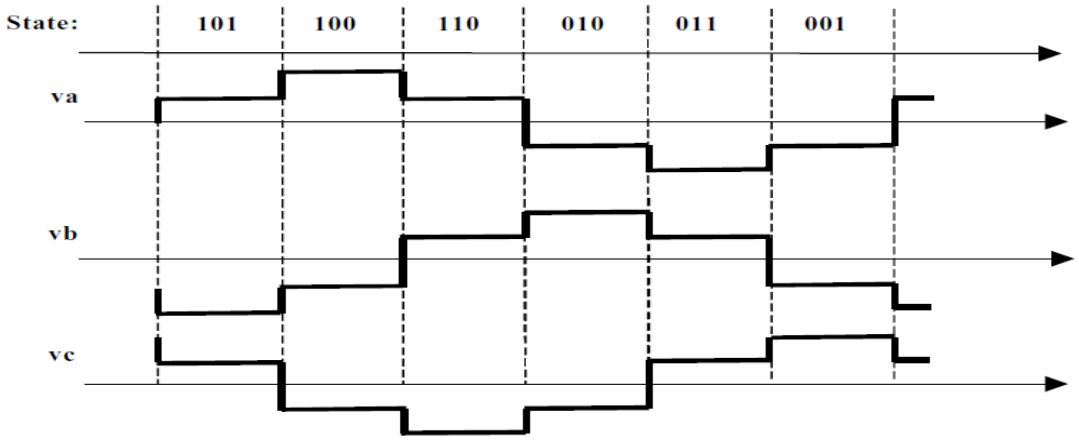


Figure 2.20: Output voltage waveform of two-level inverter

For *n*-level multilevel inverter, small triangle existed in a sector is $(n\text{-}1)^2$. The idea of operation for three-level SVPWM and two-level SVPWM are similar, but three level SVPWM is more complex due to the selection of small triangle and calculation of dwell times. The hexagon of three-level SVPWM is shown in Figure 2.18 (b) clearly shows that there are four small triangles inside a sector. As the number of triangles and vector states are increased, hence the calculations of dwell times become more complicated.

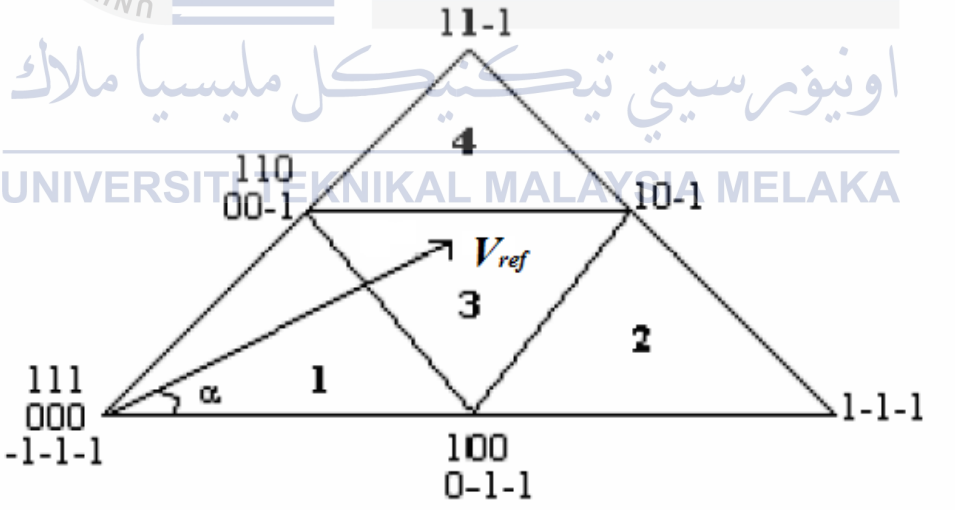


Figure 2.21: Vector in sector 1

As shown in Figure 2.21, different triangle that V_{ref} falls, the switching vectors can be differenced. Many approaches have been proposed by researches, in order to design a three-level SVPWM in most simplified method [35-41].

2.3.3 Selective Harmonic Distortion

The idea of the selective harmonic elimination (SHE-PWM) is based on the Fourier series expansion of output voltage to remove the lower order harmonics in a switching state. The Fourier series expansion for a multilevel inverter is based on the Equation (2.13).

$$V(\omega t) = \sum_{n=1,3,5,\ldots}^{k} \frac{4V_{dc}}{n\pi}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots][\sin(n\omega t)] \quad (2.13)$$

Where *n* is the harmonic order of the output voltage, *k* is the number of switching angles, and α is switching angles that must follows the condition of $\alpha_1 < \alpha_2 < \ldots < \frac{\pi}{2}$. The main function of switching angle is to minimize voltage THD ratio. The equation system of SHE-PWM method in order to eliminate the harmonic order of multilevel inverter is shown in Equation (2.14), and where *m* is modulation index.

$$\begin{aligned} &cos(\alpha_1) - cos(\alpha_2) \ldots + cos(\alpha_N) = m\frac{\pi}{4} \\ &cos(3\alpha_1) - cos(3\alpha_2) \ldots + cos(3\alpha_N) = 0 \\ &\vdots \\ &cos(N\alpha_1) - cos(N\alpha_2) \ldots + cos(N\alpha_N) = 0 \end{aligned} \quad (2.14)$$

The $\alpha_1, \alpha_2, \ldots, \alpha_N$ can be determined by using Newton-Raphson Iterations. The switching angles of SHE-PWM in three-level is shown in Figure 2.22 [49-53].

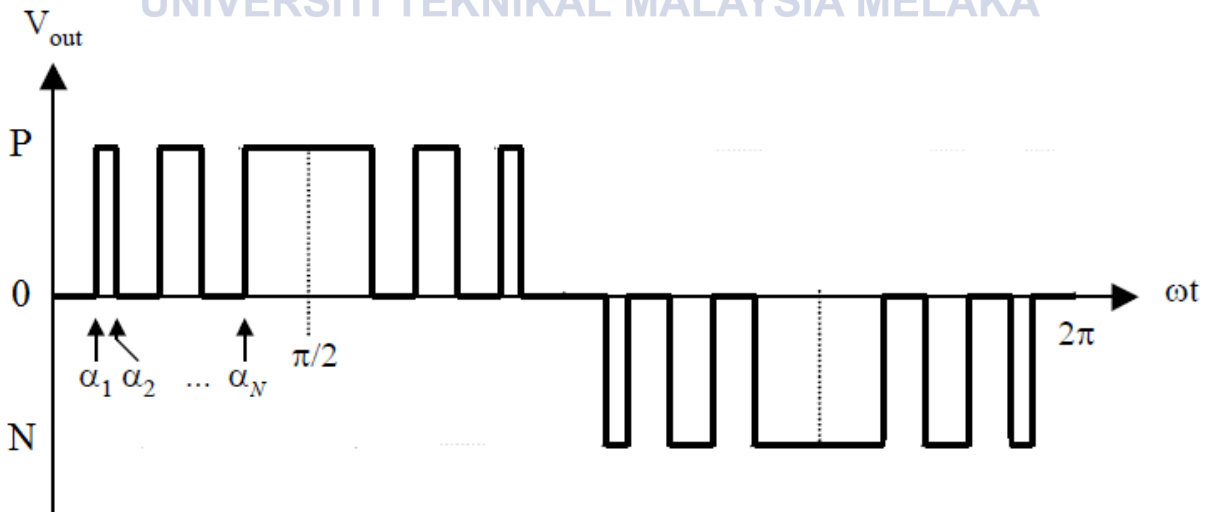


Figure 2.22: Switching angles of SHE-PWM in three-level

The challenge of dealing with SHE-PWM is the method for derived the trigonometric transcendental equations for different types of multilevel inverter topologies. If the amplitude of a harmonic is zero, then the particular harmonic will be eliminated. The switching states of the switching angles would control the switching components on the states turned on or turned off by eliminated lower order harmonics [55]. For single-phase applications system, the lowest harmonics are needed to be eliminated. But for three-phase application system, only the triplen harmonic are needed to eliminate because all the non-triplen harmonics are already been eliminated by 120-degrees phase shift characteristics.

Some of the multilevel inverter applications are operated in low switching frequency conditions. Hence, SHE-PWM does provide a few advantages over the other switching modulations. SHE-PWM provides low switching frequency with a wider multilevel inverter bandwidth and better DC source utilization [52].

2.4 Applications of Multilevel Inverter

Nowadays, the merged of multilevel inverter application in daily life have become common, such as the application of inverter as adjustable speed drive in air-conditioner and refrigerator can promoted the benefits of efficiency and energy saving. The application of inverter not only restrict on household application but also widely used in industrial field, such as power conversion for higher voltage in grid, flexible AC transmission system (FACTS) devices, STATCOMs, and etc. It is undeniable that inverter is one of the equipment boost up the interface of renewable energy in daily life because inverter can supplied the electrical energy into the grid.

2.4.1 Renewable Energy Multilevel Inverter

Nowadays, due to the rapid growth in the green technology, many natural alternative energy, such as wave energy, wind energy and solar energy have been used to replace fossil fuel combustion energy. Multilevel inverters have become very essential equipment in these

renewable energy fields to convert the renewable energy in constant DC form into AC form in order to supply it into national grid and meets grid. In these renewable energy fields, multilevel inverters does provided a lot of advantages over than two-level conventional inverter, in term of THD, switching losses and efficiency. For instance, neutral point clamped is suitable for conversion of wind energy and wave energy due to its properties required single DC source. Meanwhile, the conversion of solar energy is more suitable by using cascaded H-bridge multilevel inverter. As shown in Figure 2.23 and Figure 2.24, wind energy and wave energy are using the generators to convert the mechanical energy created by the movement of the natural resources into electrical AC energy form. Since, this AC energy form is in inconstant state because the variation of the movement depends on the weather changes and cannot be controlled; hence, rectifier is required to convert inconstant AC energy into constant DC energy form. An inverter is employed after the rectifier in order to convert the constant DC energy form into constant AC energy form with same frequency, amplitude and phase shift, and then supplied to national grid [65-67].

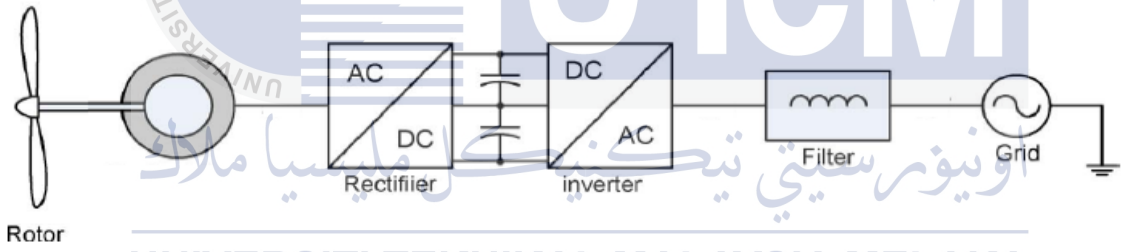


Figure 2.23: Operation of wind farm to national grid

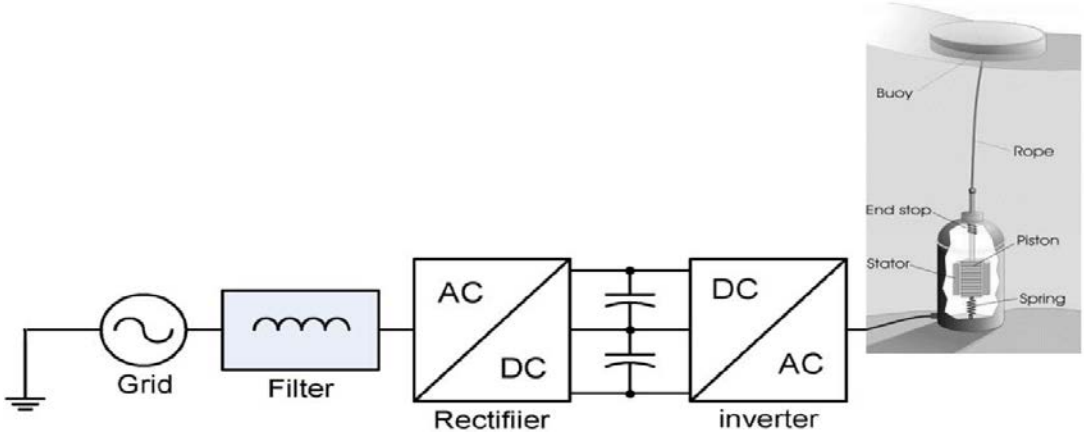


Figure 2.24: Operation of wave energy station to national grid

The operation of solar PV renewable energy as shown in Figure 2.25 is a little bit different from operation of conversion of wave energy and wind energy. The energy gain from solar PV is in DC energy form and depends on the intensity of light. Hence, instead of using rectifier, it is using the DC-DC converter to convert inconstant DC energy into constant DC energy [61-64].

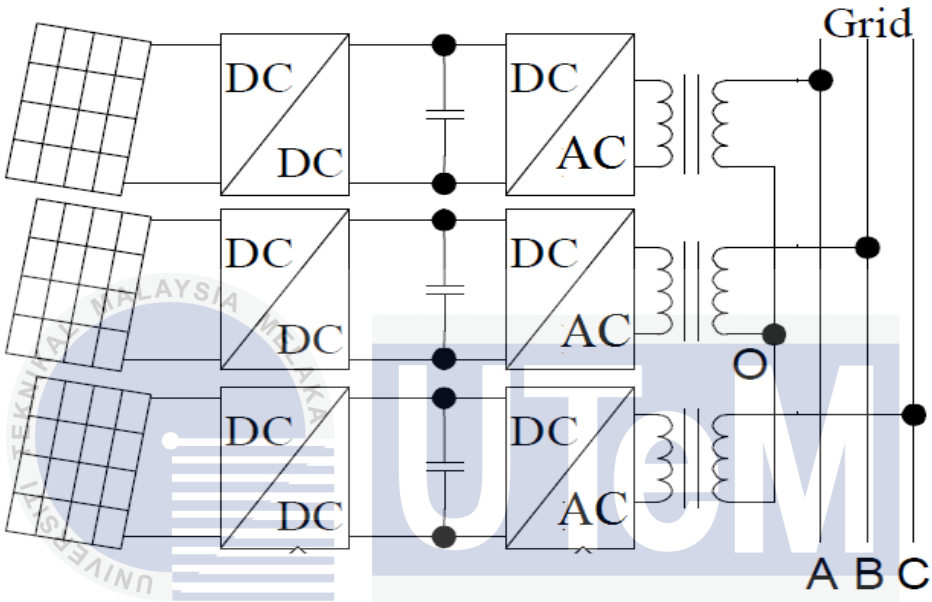


Figure 2.25: Operation of standalone PV station to national grid

The combination of this rectifier-inverter is known as back-to-back converter as shown in Figure 2.26. As can be seen in this topology, the major drawback of back-to-back converter is the number of switch required for this topology is quite a plenty number, and thus contributes the complexity of the switching modulation. The advantage of back-to-back converter is the controllable of the voltage and frequency and directly improves the power quality into the grid system [68-69].

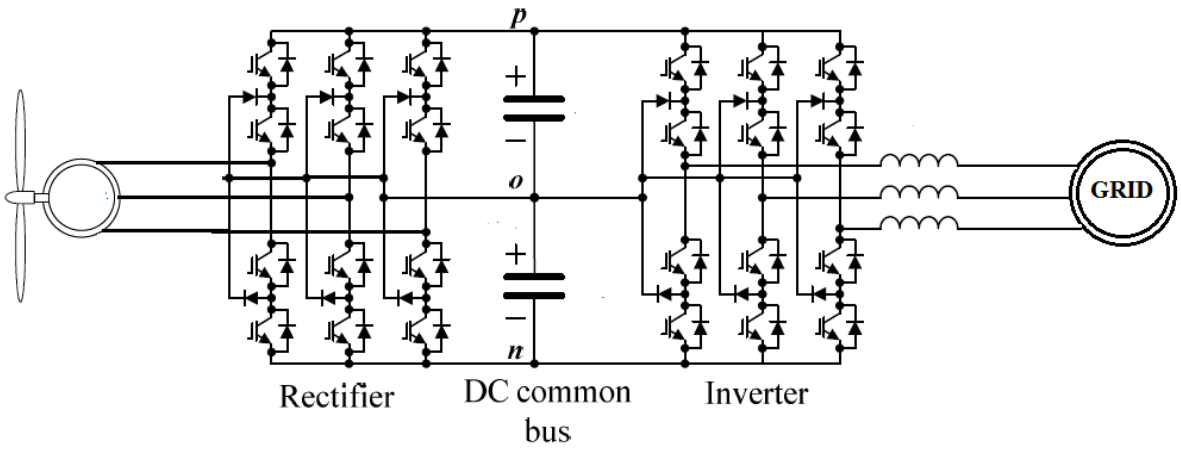


Figure 2.26: Back-to-back converter

2.4.2 Adjustable Speed Drive

Adjustable speed drives also known as variable speed drives become a very important application in this industrial field. The way of controlling and varying the speed of the drive depend on the situation requirement, and result in significant energy saving compared to traditional control method [75]. By controlling the speed of the drive can also control the speed of starting operation, smoother the operation and control the speed of the torque. Even there are many benefits by using the adjustable speed drive; but there are still disadvantages existed; such as motor easy heat up when operated in low speed, cost of the device and maintenance problem [79]. The switching modulation used to control adjustable speed drive is the sinusoidal pulse width modulation, which provides the better efficiency in controlling the application's speed by control the width of the pulse. The longer the pulse, the higher the power would supplied to the load. The topology of adjustable speed drive is shown in Figure 2.27 [77].

Another important function performed by the multilevel inverter is the direct torque control (DTC), which is used as a control strategy used in control torque for AC drives applications based on the current and voltage of the motor. The major problem faced by multilevel inverter in this application is higher torque ripple. Even many solutions have been proposed by researchers in order to address this problem, but the problem still become severe when the number of output voltage level increased. By selecting suitable inverter topology and

control switching modulation, the major drawback effect of this application can be reduced [56-60].

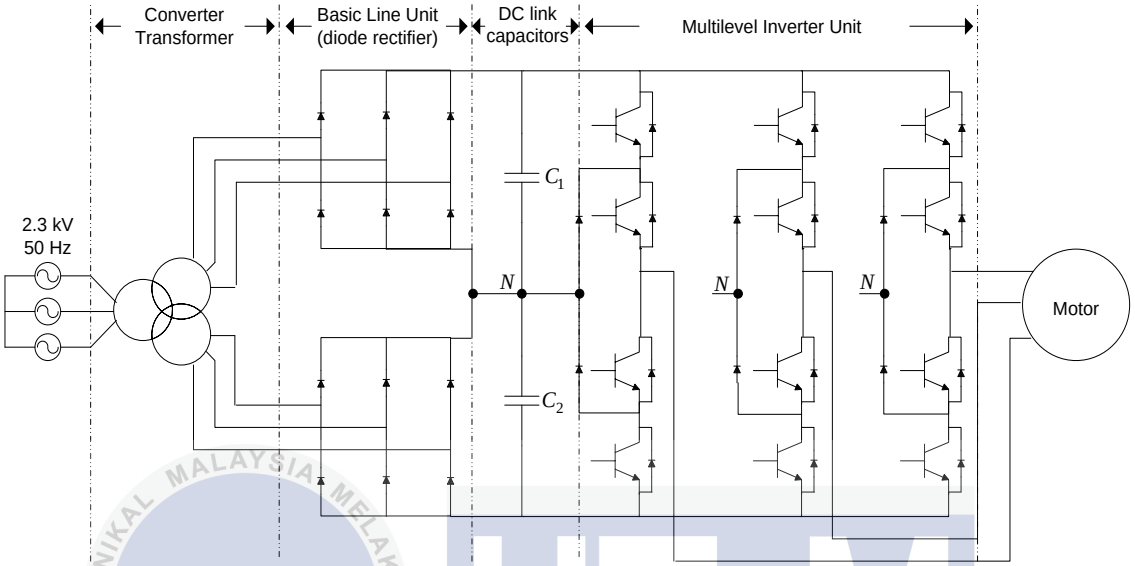


Figure 2.27: Adjustable speed drive

2.5 Summary

Many topologies have been discussed in this chapter. Different applications would adopt difference types of topologies. Applications with certain requirement properties can be designed by using asymmetric hybrid inverter. Different control switching modulations have its own pros and cons, sinusoidal pulse width modulation is more simplest compared with space vector pulse width modulation. The complexity would not increase even the number of level output voltage is increase, but the efficiency of space vector pulse-width modulation is much better than sinusoidal pulse width modulation. Selective harmonic elimination is a method of efficiency by eliminated the harmonic order, but the derivation of trigonometric transcendental equations would become complicated as the number of level output voltage increased. It is undeniable the implemented of inverter in application of industrial field and household application become inevitable, as the inverter would provide the advantages of energy efficiency and money saving.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Introduction

The important parameters of an inverter, such as switching losses, DC-link voltage balancing, and harmonic content are deeply associated with the control switching modulation. The most usual switching modulations that adopted are sinusoidal pulse-width modulation (SPWM), space vector pulse-width modulation (SVPWM), and selective harmonic elimination (SHE-PWM). This chapter would discuss about the process that used to generate the switching signal that used to control the switching state of inverter. The control switching modulations that would discuss in this chapter are SPWM and SVPWM. This chapter is divided into two parts. The first part in this chapter is control switching modulation based on two-level conventional inverter; and the second part is focused on the control switching modulation on three-level and five-level NPC-MLI.

3.2 Control Switching Modulation of Two-Level Conventional Inverter

Simulation models of three-phase two-level conventional inverter have been developed in MATLAB Simulink R2010a as shown in Figure 3.1. Three-phase two-level conventional inverter is composed of six IGBTs. Each phase of the inverter consists of complimentary switch pair (upper switch and lower switch). The parameters used for simulation SPWM and SVPWM are given in Table 3.1.

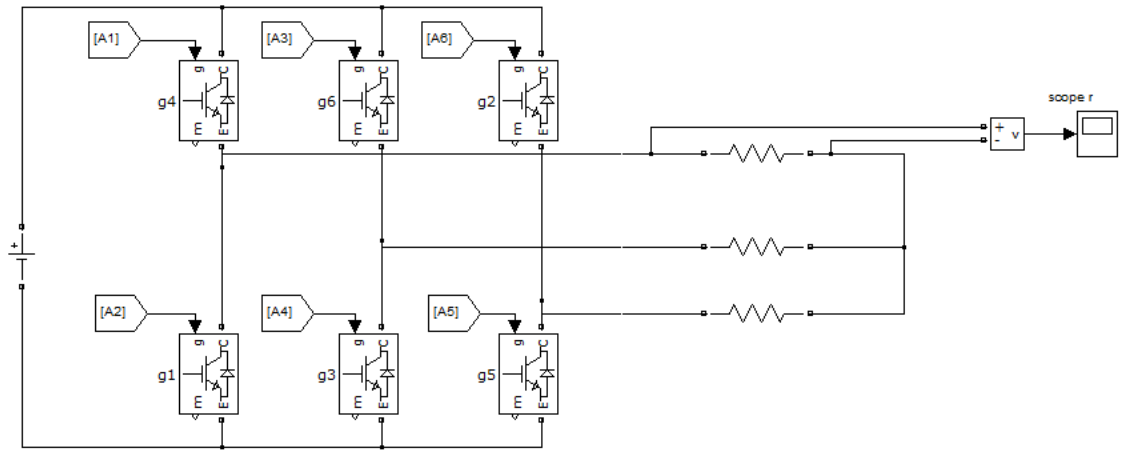


Figure 3.1: Simulink models for three-phase two-level conventional inverter

Table 3.1: Simulation parameters for two-level conventional inverter

Parameters	Values
DC Input source	$400V_{DC}$
Fundamental frequency	50Hz
Switching frequency	2k Hz
Load	5Ω & 25mH

3.2.1 Two-level Sinusoidal Pulse-Width Modulation (SPWM)

SPWM is a method that a low frequency reference waves compared with the high switching triangle carrier frequency though comparator. The idea of comparator is illustrated in Figure 3.2.

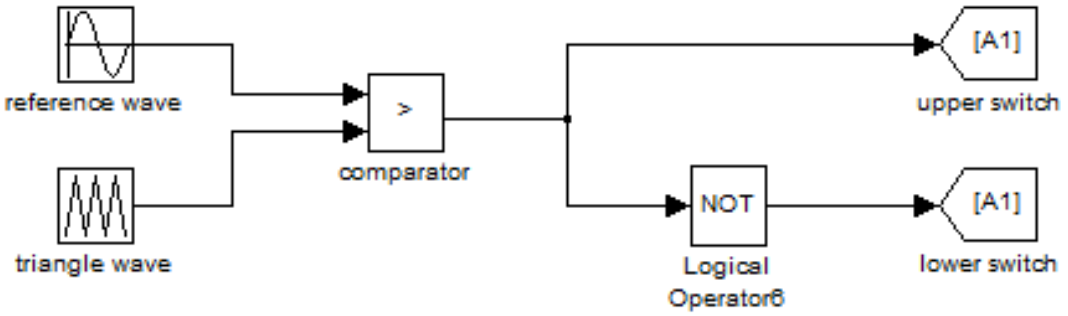


Figure 3.2: Comparison between reference and carrier waveform

As in Figure 3.2, the output of comparator is used to control the upper switch and lower switch of inverter. The upper switch and lower switch are work in complementary manner. The desired voltage output frequency can be controlled by low frequency reference waveform. The desired output voltage frequency will be same as reference sinusoidal frequency. Based on the Figure 3.3, if the reference sinusoidal waveform is higher than carrier triangle waveform, the upper switch turns on and the lower switch turns off. If the reference waveform is lower than carrier waveform, the upper switch turns off and lower switch turns on.

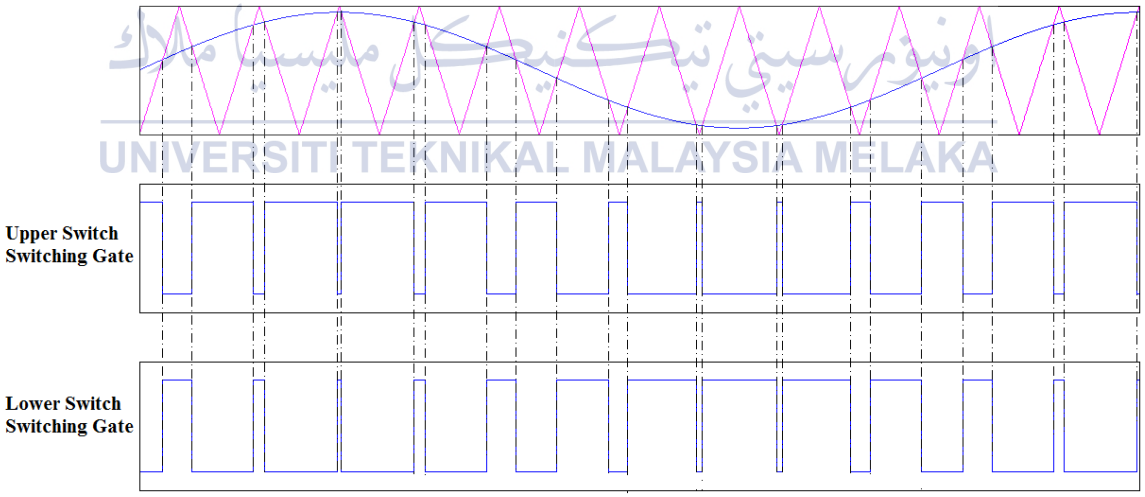


Figure 3.3: Gate signal generation for SPWM

Due to the operation of conventional inverter is in three phases, hence the inverter would consist of the three reference sinusoidal waveforms with the phase shift difference by 120^0, as shown in Figure 3.4. The idea of SPWM with three-phase reference signal and high frequency carrier signal in Matlab/SIMULINK is shown in Figure 3.5.

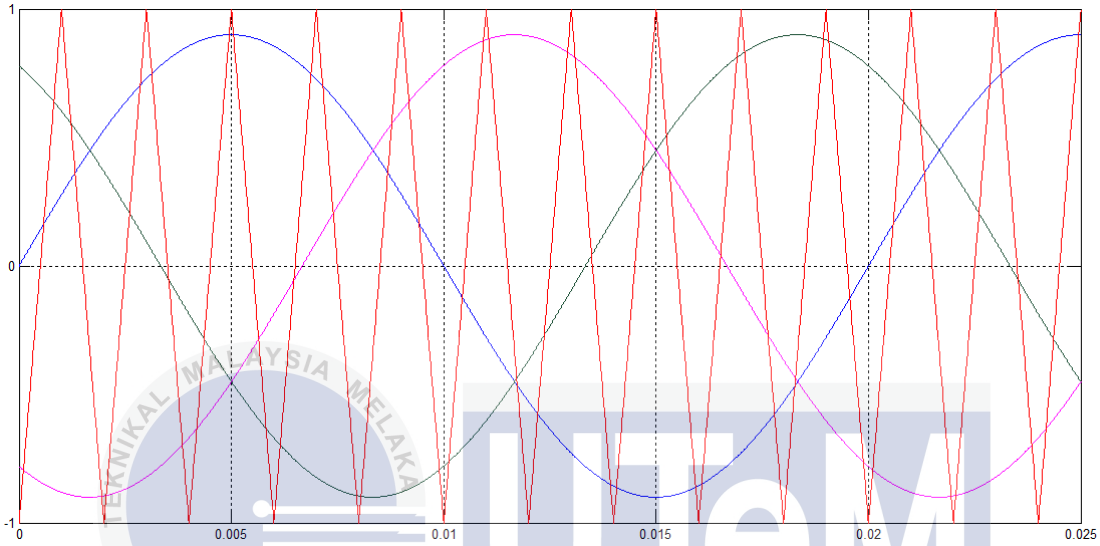


Figure 3.4: Three phase sinusoidal waveform with carrier waveform

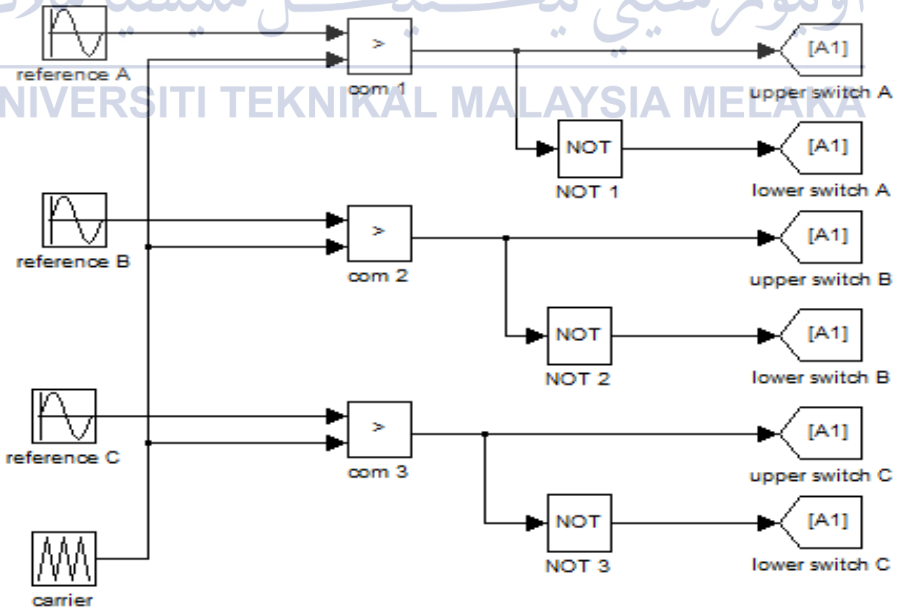


Figure 3.5: Three-phase switching scheme

3.2.2 Two-level Space Vector Pulse-Width Modulation (SVPWM)

SVPWM is a method that selection of switching state is based on the vectors of the 60-degree coordinates. The phase switching state remains the same for a constant 60-degree and the vector state will changes after 60-degree interval. The first steps in two-level SVPWM are the calculation of reference voltage vector,V_{ref} and the phase angle, θ. These two values are generated from summation of three reference waveforms as shown in Figure 3.6.

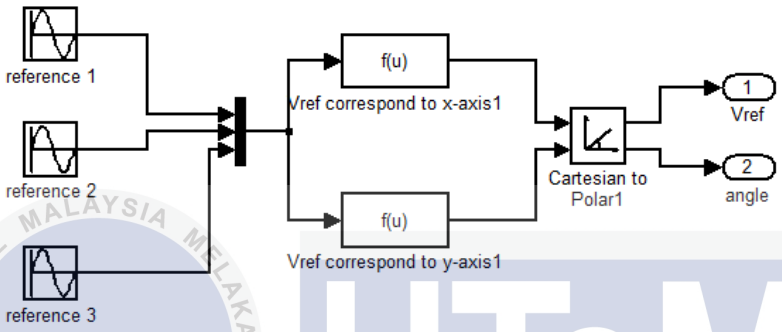


Figure 3.6: Reference voltage vector,V_{ref} and the phase angle, θ

Figure 3.7 shows the second step for two-level SVPWM, is to divide equally the sector with every 60-degree and select the sector based on the phase angle, θ obtained from step 1.

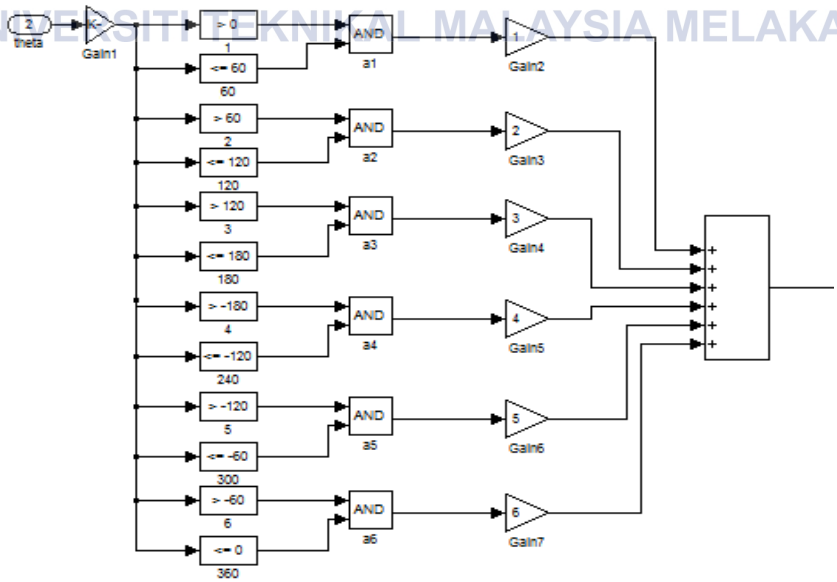


Figure 3.7: Division of six sectors

Theoretically, V_{ref} will rotate around all sectors as shown in Figure 3.8; hence, the vector switching state is determined according to which sector that V_{ref} laying. In Matlab/SIMULINK, the vector determinations for every sector can be clarified in Figure 3.9.

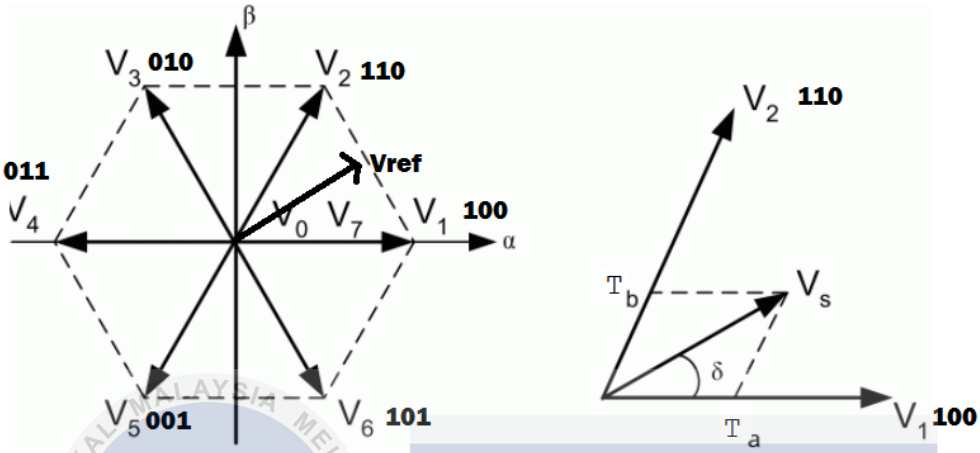


Figure 3.8: Hexagon with six active vectors

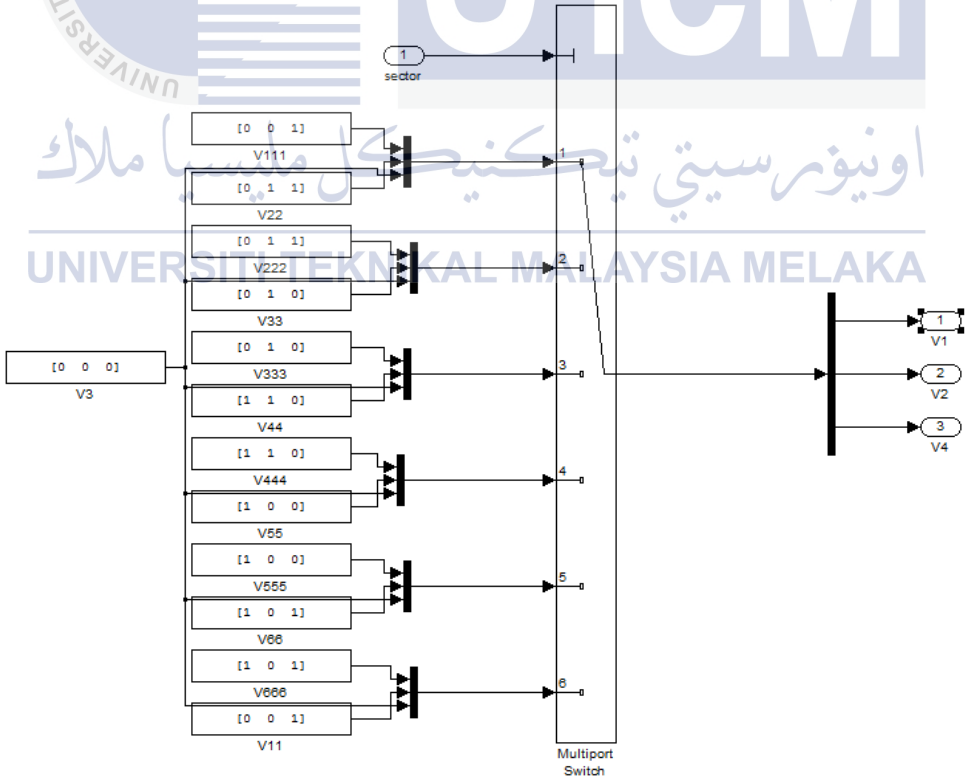


Figure 3.9: Vector switching states

As can be seen in Figure 3.8, each leg switching state is determined by active vector in where V_{ref} is allocated. Besides that, each sector is within the two active vectors, V_1 and V_2. V_1 happened during switching period T_a,and V_2 happened during switching period T_b. Figure 3.10 illustrates the determining the switching period.

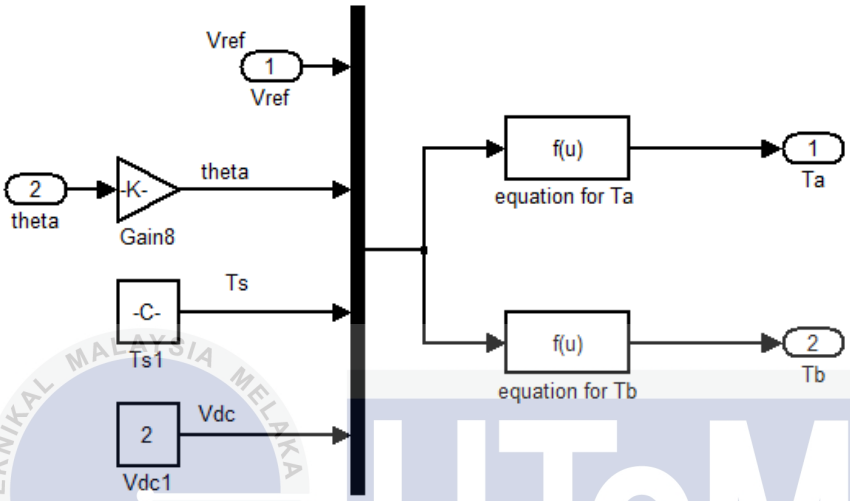


Figure 3.10: Determining the switching period

Finally, according to which sector and switching period of reference voltage vector was laying, the switching state can be determined, as it depicted in Figure 3.11.

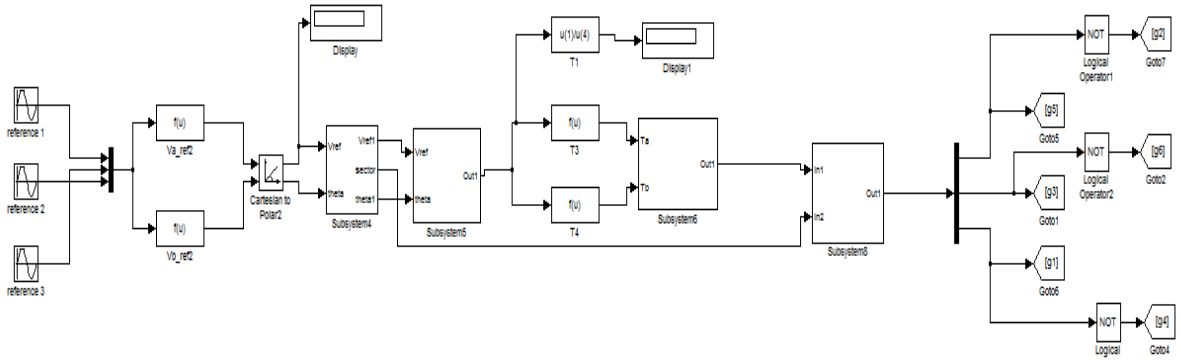


Figure 3.11: Switching schemes of SVPWM

3.3 Control Switching Modulation of Three-level and Five-level NPC-MLI

Simulation models of three-phase three-level NPC-MLI have been developed in MATLAB/Simulink R2010a as shown in Figure 3.12. Three-level NPC-MLI is composed of four IGBTs in a leg. The overall IGBTs required in three-phase three-level NPC-MLI are twelve. In each leg of the inverter consists of two complimentary switch pairs; pair a1-a3 and pair a2-a4. The parameters used for simulation three-level MSPWM and SVPWM are given in Table 3.2.

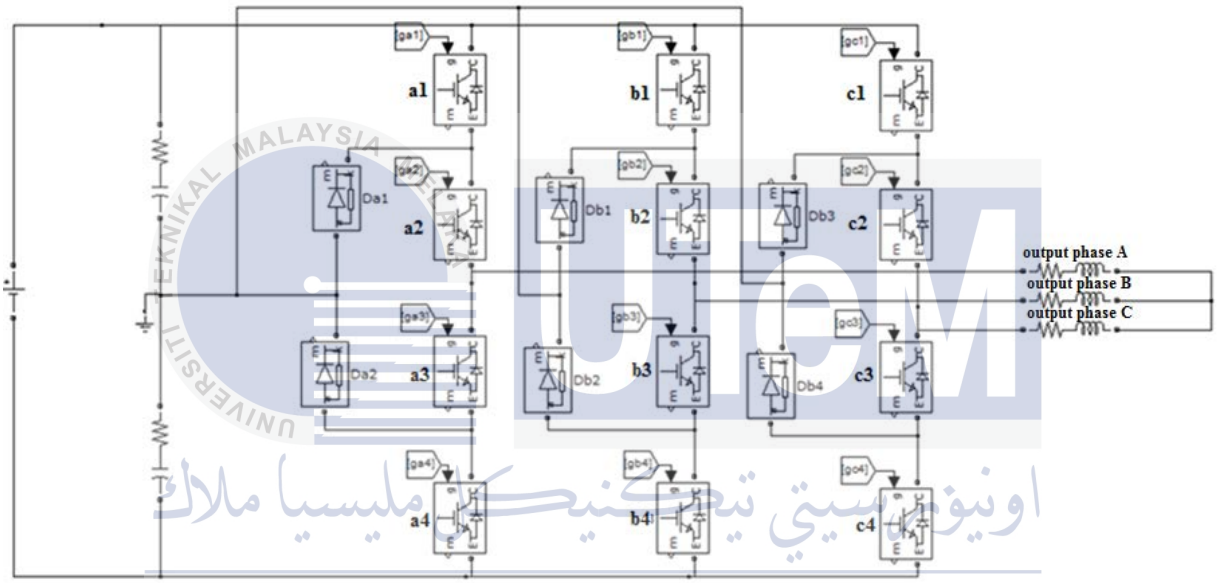


Figure 3.12: Simulink models for three-phase three-level NPC-MLI

Table 3.2: Simulation parameters for three-level NPC-MLI

Parameters	Values
Input source	$800V_{DC}$
Fundamental frequency	50Hz
Switching frequency	2k Hz
Resistive load	5Ω
Inductive load	25mH

Simulation models of three-phase five-level NPC-MLI have been developed in MATLAB Simulink R2010a as shown in Figure 3.13. Five-level NPC-MLI is composed of eight IGBTs in a leg. The overall IGBTs required in three-phase five-level NPC-MLI are 24. Each phase of the inverter consists of four complimentary switch pairs; pair a1-a5, pair a2-a5, pair a3-a6 and pair a4-a8; The parameters used for simulation five-level MSPWM and SVPWM are given in Table 3.3.

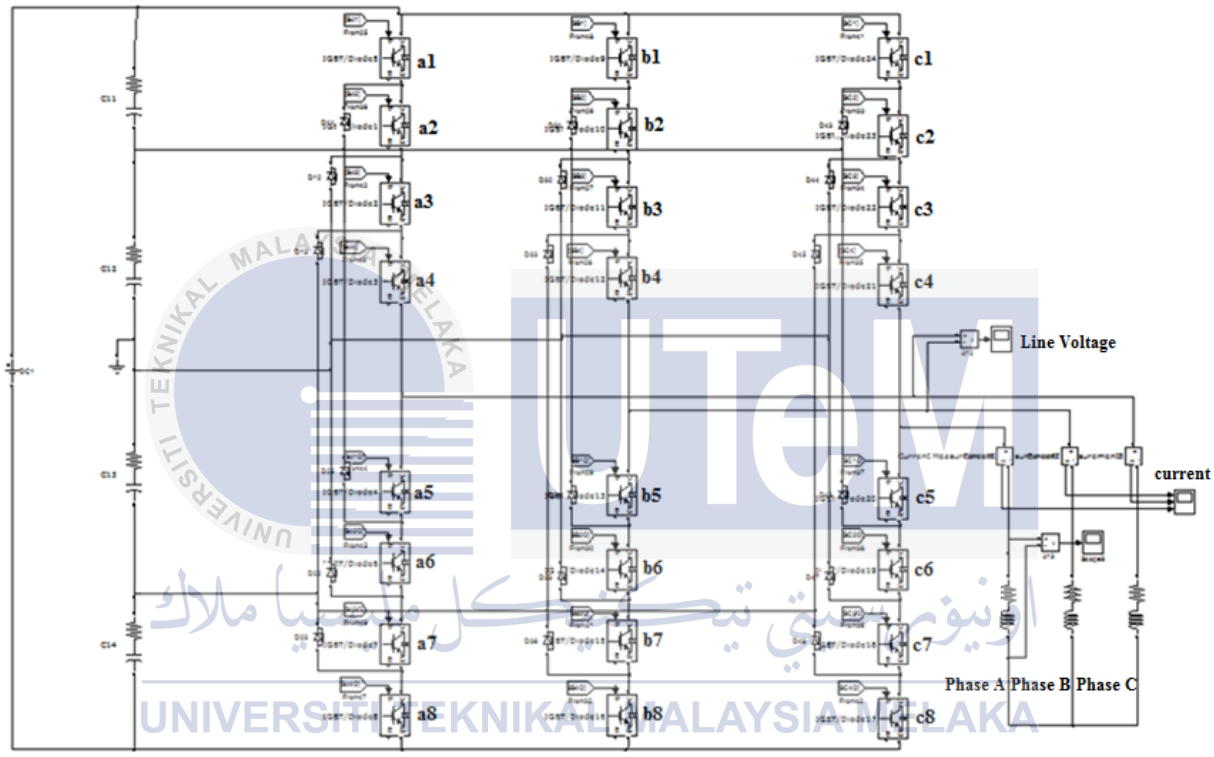


Figure 3.13: Simulink models for three-phase three-level NPC-MLI

Table 3.3: Simulation parameters for five-level NPC-MLI

Parameters	Values
DC Input source	$800V_{DC}$
Fundamental frequency	50Hz
Switching frequency	2k Hz
Resistive load	5Ω
Inductive load	25mH

3.3.1 Multicarrier Sinusoidal Pulse-Width Modulation (MSPWM)

Multicarrier sinusoidal pulse-width modulation (MSPWM) is a switching method that used in control multilevel inverter, where the number level of the output is greater than two. This method is derived from two-level SPWM. The operation of MSPWM is similar with SPWM, where low frequency reference waves compared with the high switching triangle carrier frequency using comparator. The difference between SPWM and MSPWM is the numbers of triangular carrier level required by five-level is four, while for three-level involved is only two. The number of triangular carrier, *N* required is *N*= (*m*-1), where *m* is the number of output levels. The idea of comparator for three-level MSPWM in Matlab/SIMULINK is shown in Figure 3.14.

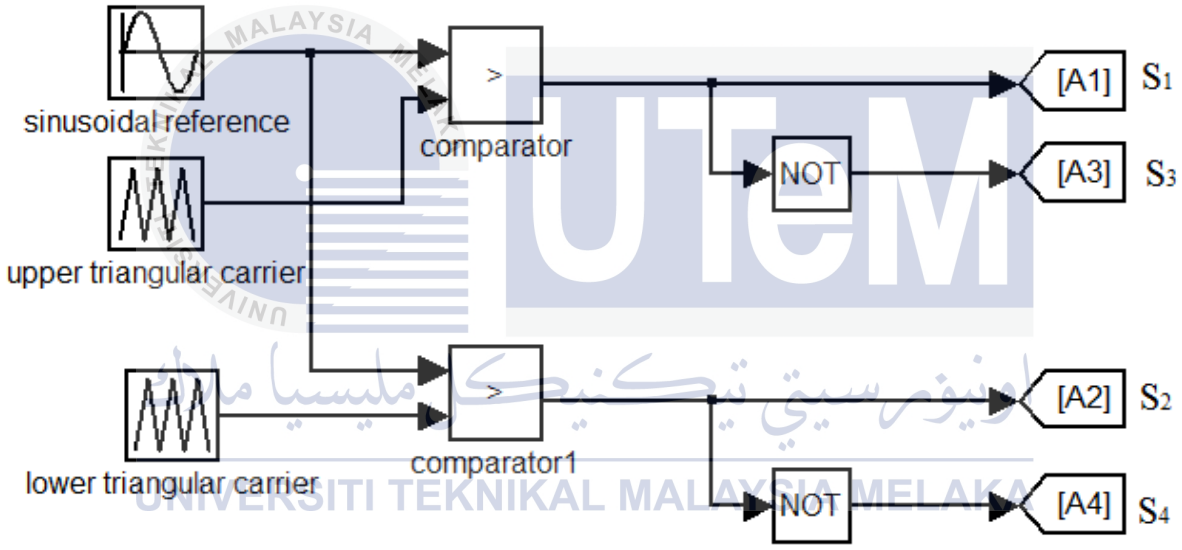


Figure 3.14: Comparator for three-level MSPWM

The comparator results of Figure 3.14 are used to control the switches of three-level NPC-MLI. The S_1 and S_3 are controlled by the upper triangular carrier signal and the S_2 and S_4 are controlled by lower triangular carrier signal. The desired output voltage frequency will be same as reference sinusoidal frequency. Based on the Figure 3.15, if the reference sinusoidal waveform is higher than upper triangle carrier waveform, the S1 turns on and the S3 turns off. If the reference waveform is higher than lower carrier waveform, the S2 turns on and S4 turns off.

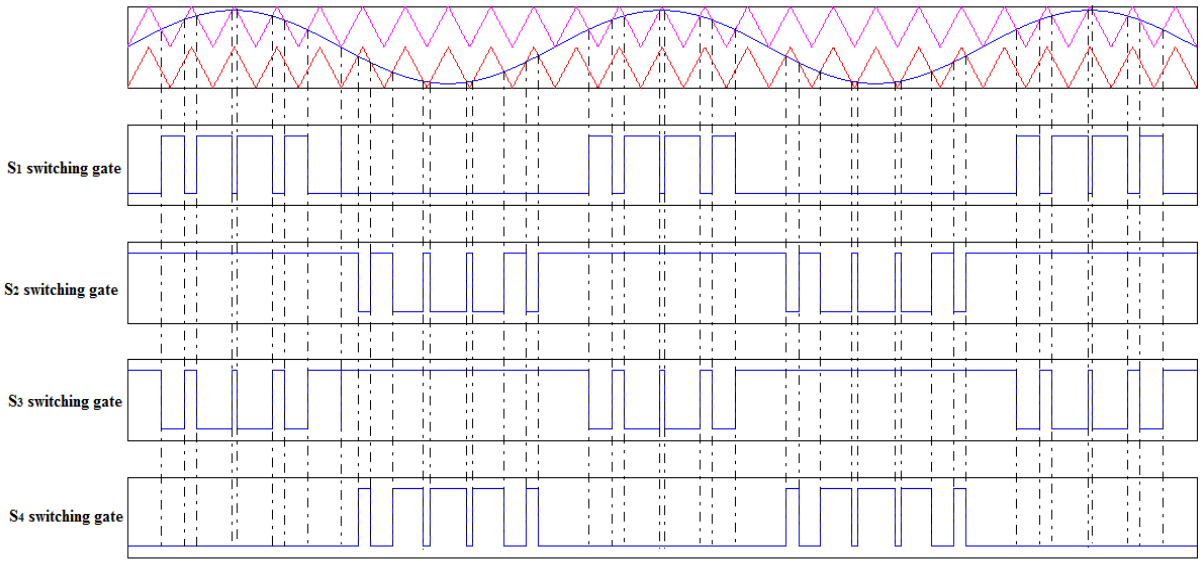


Figure 3.15: Gate signal generation for three-level MSPWM

Due to the increased number of switches in five-level NPC-MLI; hence the number of levels of triangular carrier waveform also needs to be increased, as it is used to generate signal and control switches. The idea of comparator for five-level MSPWM in Matlab/SIMULINK is shown in Figure 3.16. The schematic diagram of switching gates of five-level MSPWM is shown in Figure 3.17.

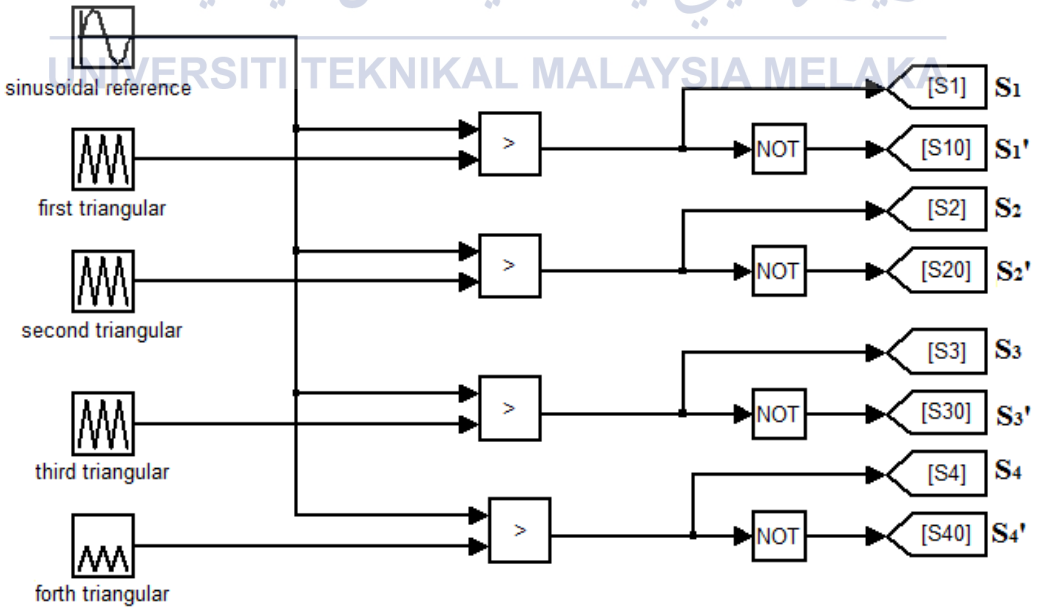


Figure 3.16: Comparator for five-level MSPWM

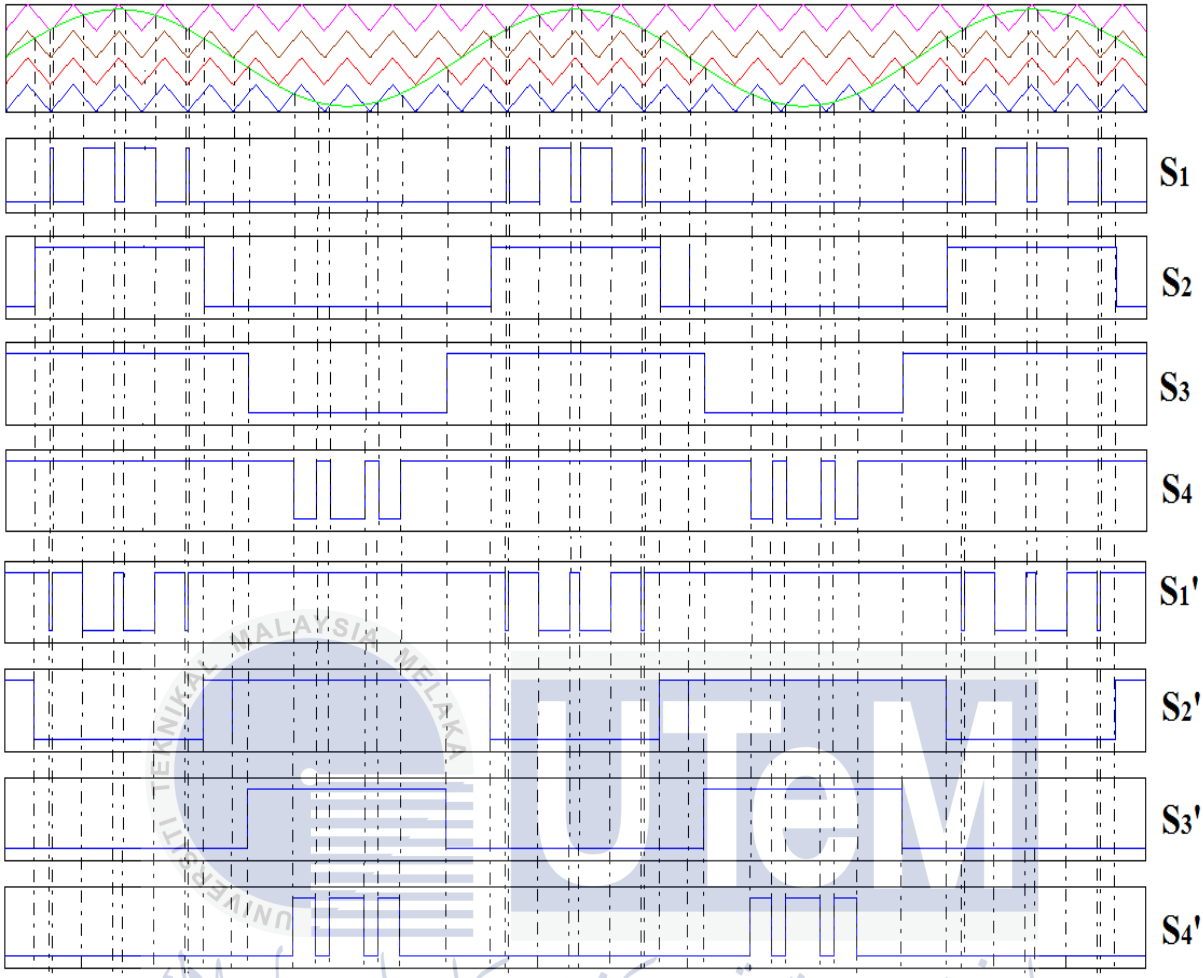


Figure 3.17: Gate signal generation for five-level MSPWM

In this study, the operation of NPC-MLI is in three-phase system; hence the operation of NPC-MLI would consist of the three references sinusoidal waveforms with the phase shift difference by 120^0 compared with triangular carrier waveforms as shown in Figure 3.18. The idea of three-level MSPWM with three-phase reference signal and two high frequency carrier signal in Matlab/SIMULINK is shown in Figure 3.19.

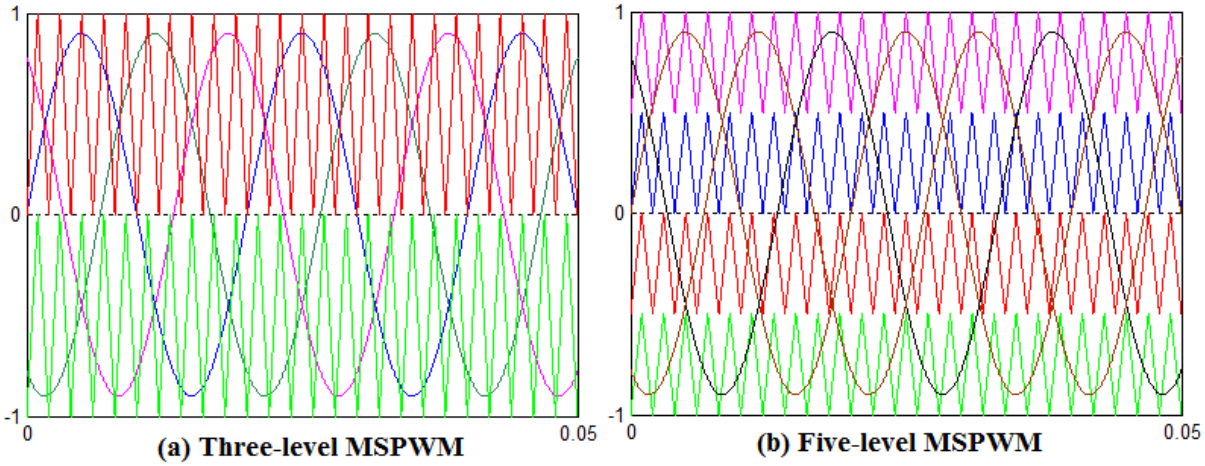


Figure 3.18: Three reference signals with multiple carrier signals

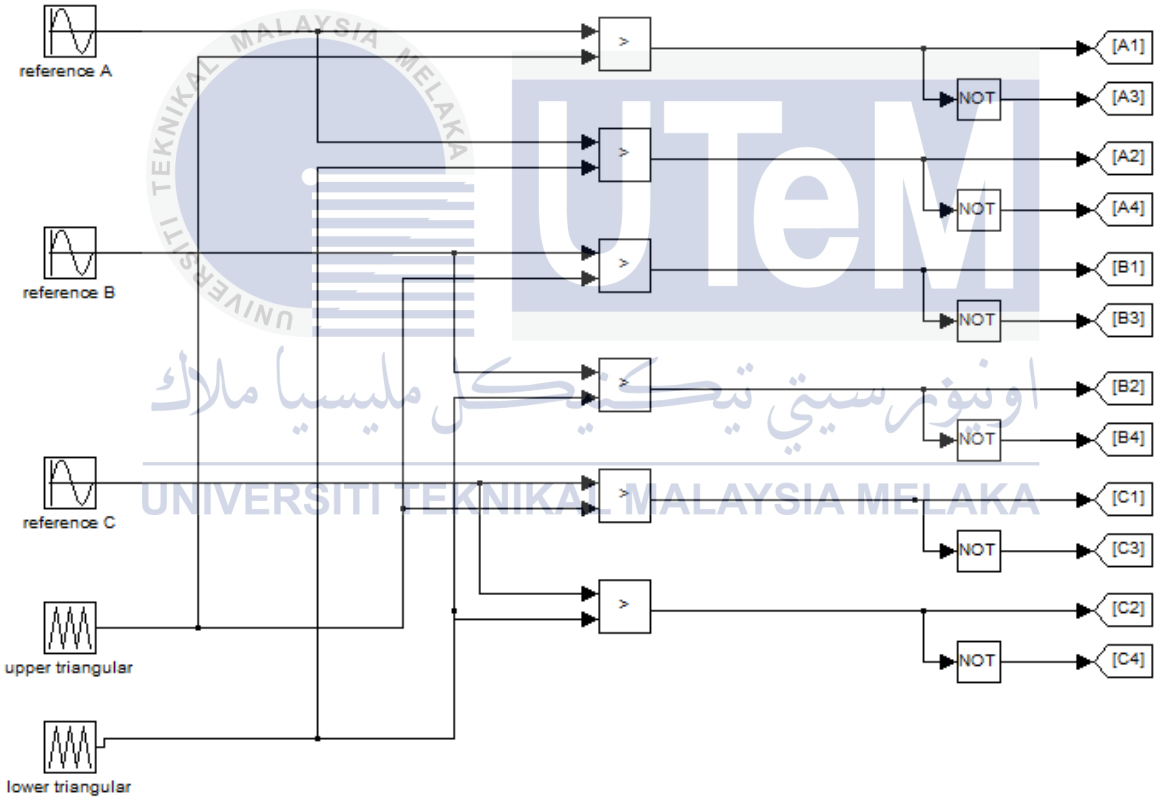


Figure 3.19: Three-level MSPWM in Matlab/SIMULINK

3.3.2 Three-Level Space Vector Pulse-Width Modulation (SVPWM)

SVPWM is a control switching modulation technique that generated reference voltage, V_{ref} moves along circular around hexagon. The vector switching sequence is based on nearest active vectors on which the V_{ref} is laying. For *n*-level multilevel inverter, small triangle existed in a sector is $(n\text{-}1)^2$. Three-level SVPWM is more complex compared to two-level SVPWM due to difficult in selecting the suitable small triangle on which V_{ref} located. The three-level SVPWM proposes in this study is based on two-level simplification. The schematic diagram of three-level SVPWM hexagon is shown in Figure 3.20.

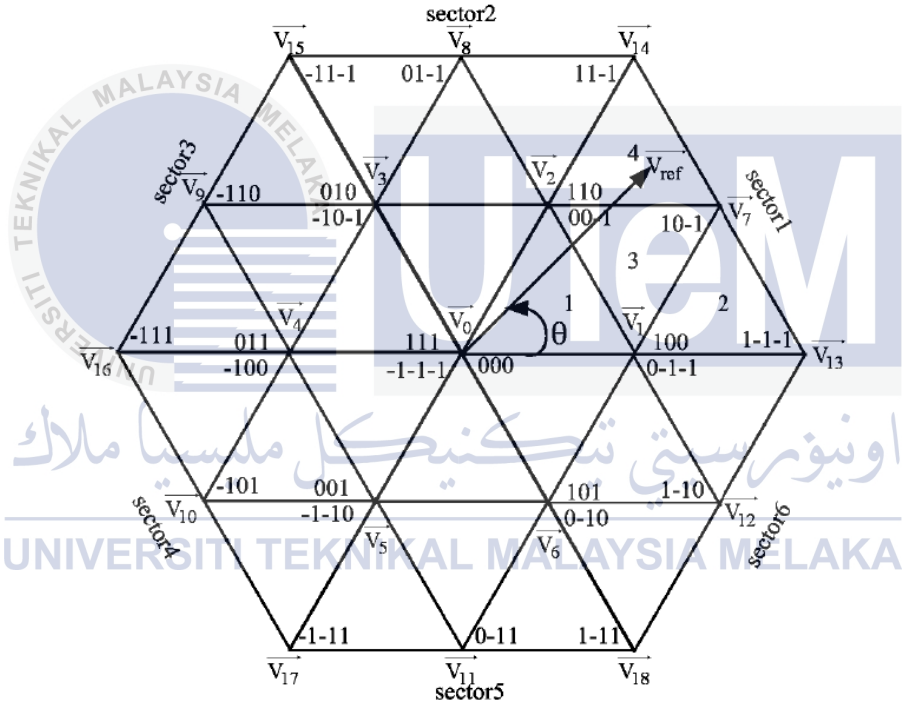


Figure 3.20: Hexagon for three-level SVPWM

The first step in designing a SVPWM regardless the number of output level is determination of reference voltage, V_{ref} and its phase angle, θ. The θ must be within the range of $0° < \theta < 360°$. These two values are generated from summation of three reference waveforms as shown in Figure 3.21.

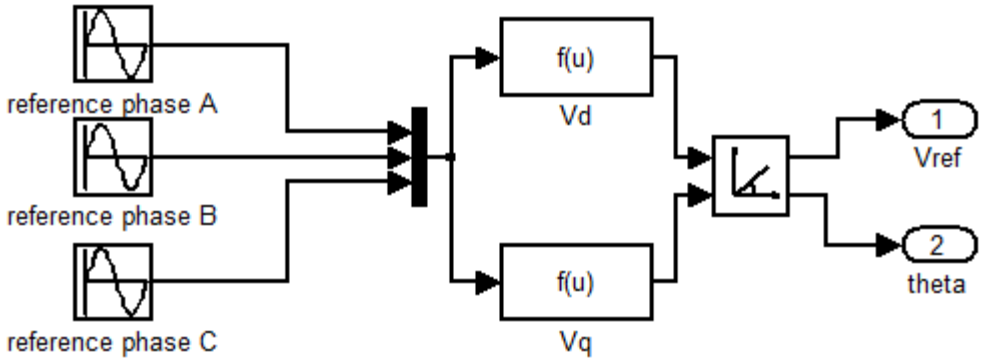


Figure 3.21: Determination of V*ref* and θ

The second step is determination of sector, *S* and its angle within the sector, γ that based on the θ in the first step; these two values can be determined by Equation (3.1) and Equation (3.2). The operation of determination of these two values in Matlab/SIMULINK is shown in Figure 3.22.

$$S = int\left(\frac{\theta}{60}\right) + 1 \tag{3.1}$$

$$\gamma = rem\left(\frac{\theta}{60}\right) \tag{3.2}$$

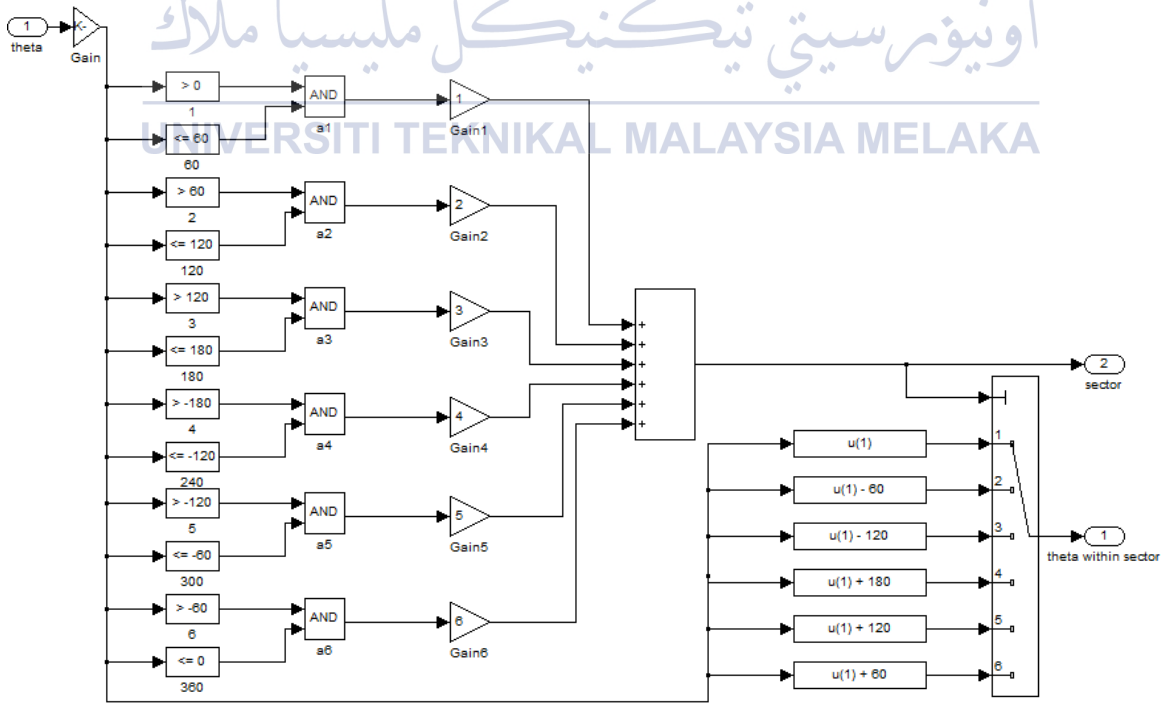


Figure 3.22: Determination of sector, *S* and its angle within the sector, γ

The angle within the sector, γ that obtained in step above is used to calculate the coordinates (V_α, V_β) as presented in Equations (3.3) and (3.4), respectively. The calculation of coordinates (V_α, V_β) is shown in Figure 3.23.

$$v_\alpha = v_{ref} \times cos\gamma \tag{3.3}$$

$$v_\beta = v_{ref} \times sin\gamma \tag{3.4}$$

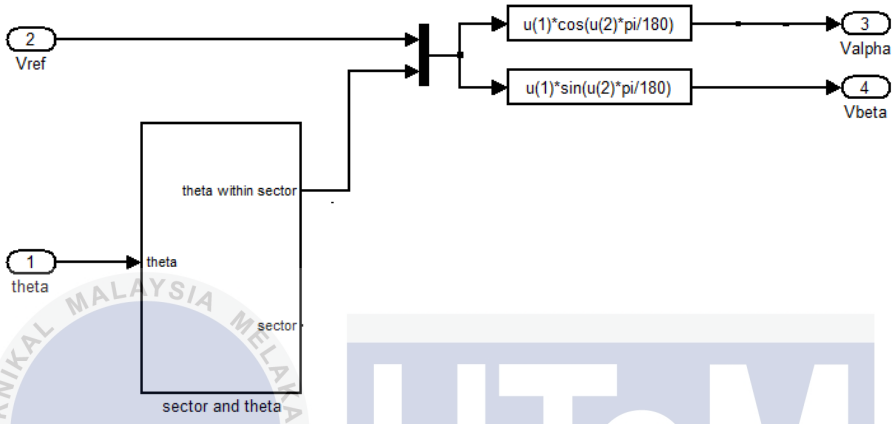


Figure 3.23: Calculation of coordinates (V_α, V_β)

The third step of designing a three-level SVPWM is identification of small triangle within sector. There are four small triangles in a sector; area 1, area 2, area 3 and area 4 as shown in Figure 3.24. By referring to Figure 3.20, the overall small triangles inside hexagon are twenty-four triangles.

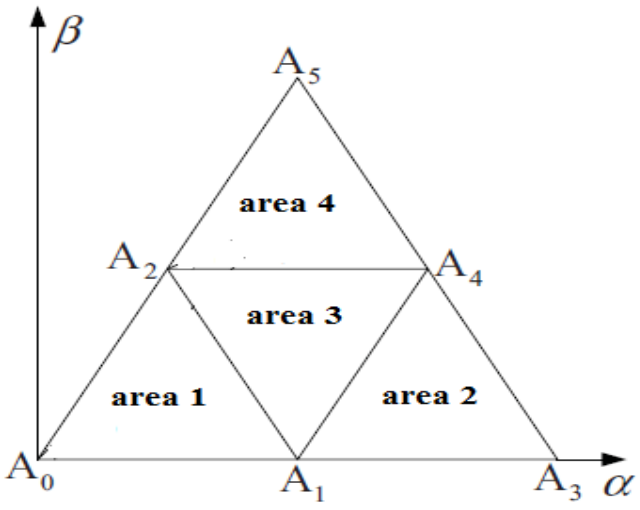


Figure 3.24: Small triangles in sector 1: area 1, area 2, area 3, and area 4

The selection of small triangle is based on two integers, B_1 and B_2 that depend on the coordinates (V_α, V_β) as given in Equation (3.5) and Equation (3.6), where h is $\frac{\sqrt{3}}{2}$. The judgement of small triangle is shown in Table 3.4.

$$B_1 = int\left(v_\alpha + \frac{v_\beta}{\sqrt{3}}\right) \tag{3.5}$$

$$B_2 = int\left(\frac{v_\beta}{h}\right) \tag{3.6}$$

Table 3.4: Rule for selection small triangle

Triangle	B_1	B_2
1	0	0
2,3	1	0
4	1	1

If the triangle is in area 1 and 4, then coordinates (V_α, V_β) using will be same as Equation (3.3) and Equation (3.4). But if the triangle is in area 2 and 3, then the new coordinates ($V_{\alpha i}$, $V_{\beta i}$) is needed to be recalculated by using Equation (3.7) and Equation (3.8). The coordinates of area 3 and area 4 is shown in Figure 3.25.

$$v_{\alpha i} = B_2(v_\alpha - B_1 + 0.5) \tag{3.7}$$

$$v_{\beta i} = h(v_\beta - B_2) \tag{3.8}$$

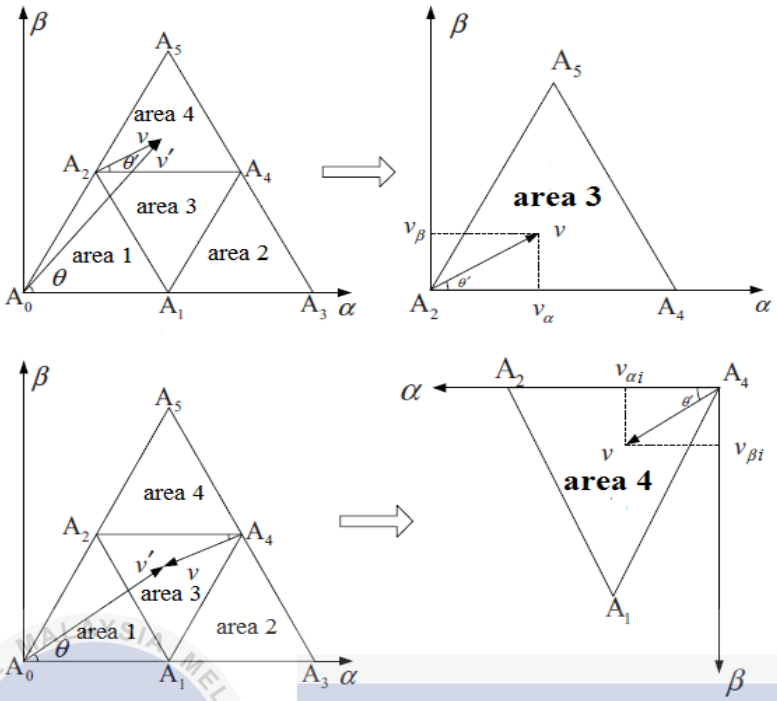


Figure 3.25: Coordinate in area 3 and new coordinate in area 4

In order to differentiate between area 2 and area 3, new coordinates ($V_{\alpha i}$, $V_{\beta i}$) getting in upper step will be compared by using new rule, if $V_{\alpha i} <= V_{\beta i}$, then triangle is in area 2, otherwise triangle is in area 3. The selection of small triangle in Matlab/SIMULINK is shown in Figure 3.26.

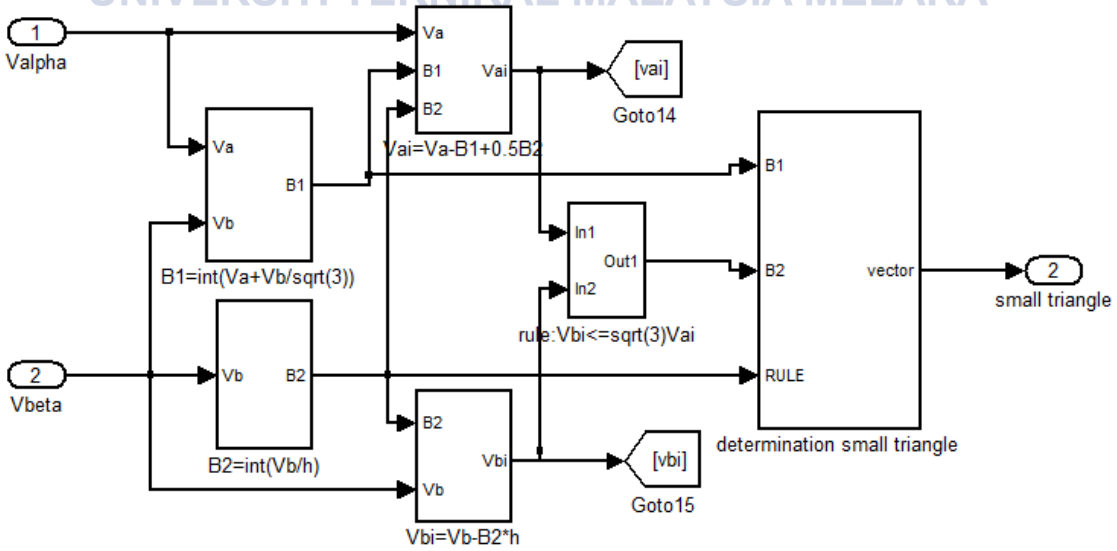


Figure 3.26: Selection of small triangle

The next step is the calculation of the switching time. The switching time of proposed method can be calculated based on switching time of two-level SVPWM. The T_a, T_b and T_c can be obtained as Equation (3.9), Equation (3.10) and Equation (3.11) respectively. The calculation of switching time of three-level SVPWM in Matlab/SIMULINK is shown in Figure 3.27.

$$T_a = t_s \times \left(v_\alpha - \frac{v_\beta}{2h}\right) \tag{3.9}$$

$$T_b = v_\beta \times \frac{t_s}{h^2} \tag{3.10}$$

$$T_c = t_s - T_a - T_b \tag{3.11}$$

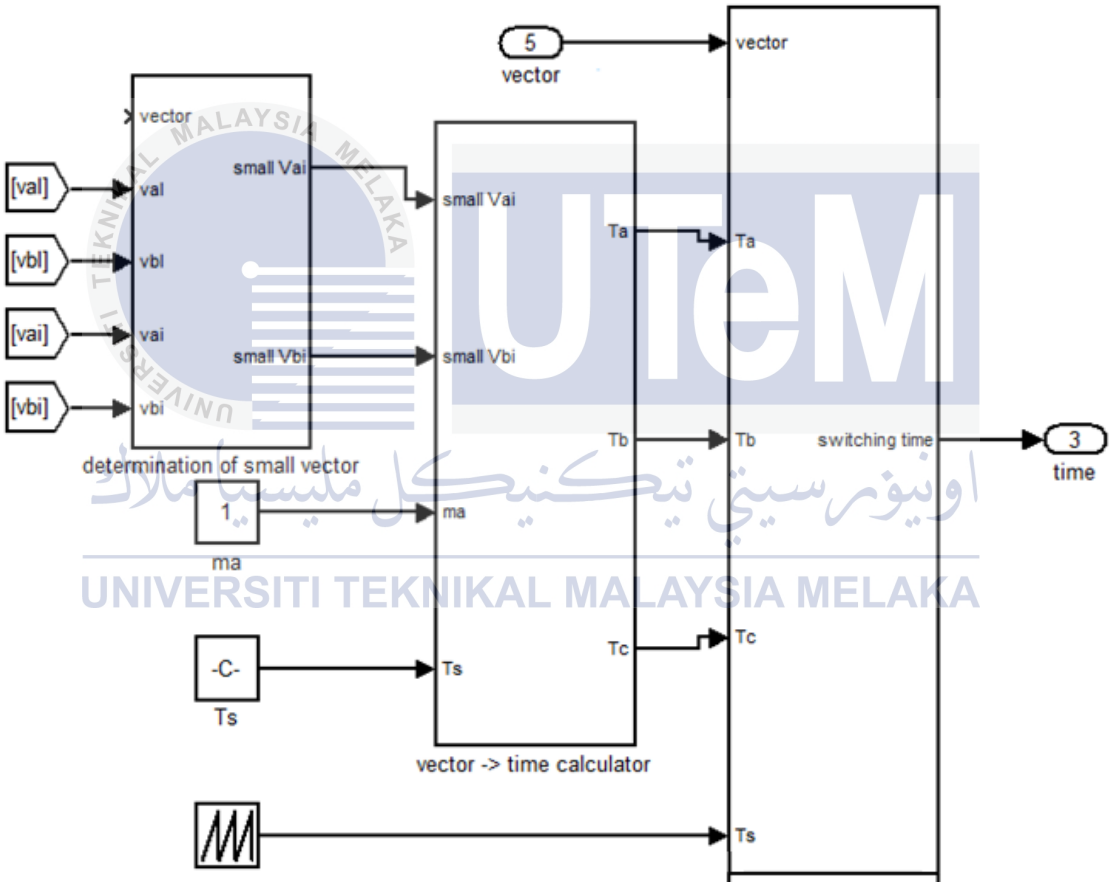


Figure 3.27: Calculation of switching time

The switching pattern of T_a, T_b and T_c are totally depend on the which small triangle that V_{ref} is lying. Figure 3.28 will illustrated the switching pattern for four different small triangles in sector 1. The switching pattern of area 2 is shown in Figure 3.29.

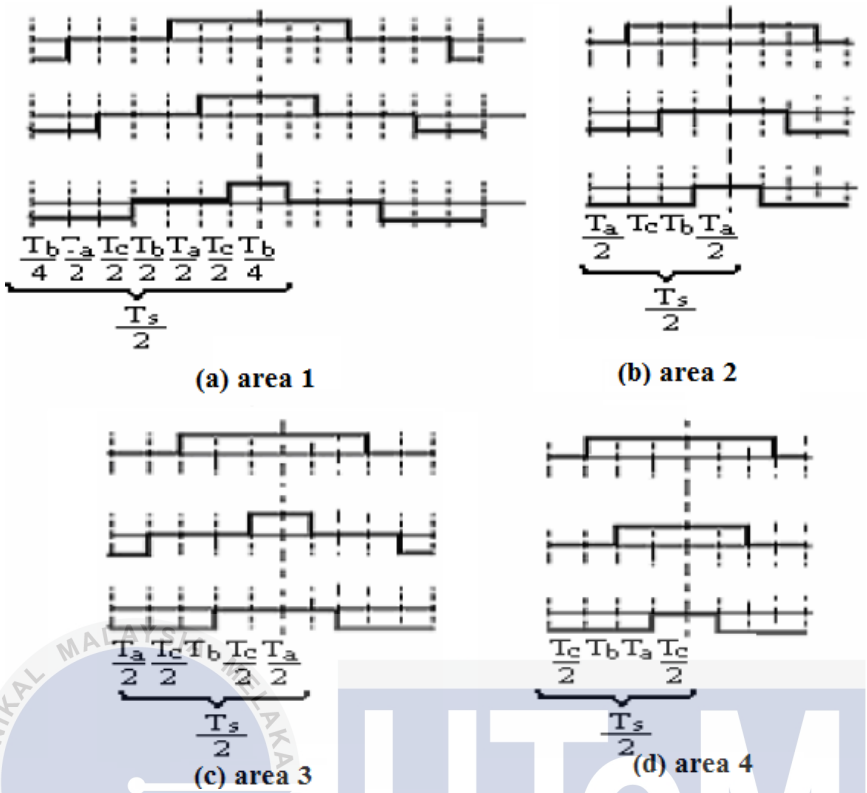


Figure 3.28: Switching pattern of small triangle in sector 1

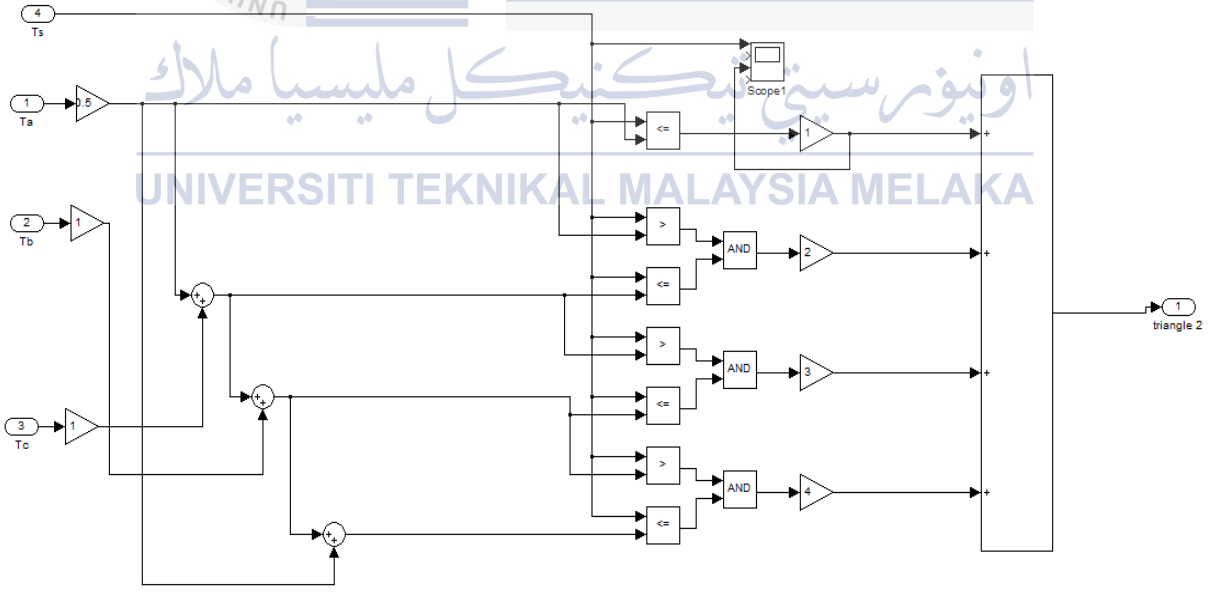


Figure 3.29: Switching pattern for area 2 in Matlab/SIMULINK

The overall schematic diagram of three-level SVPWM that has been developed in Matlab/SIMULINK is shown in Figure 3.30.

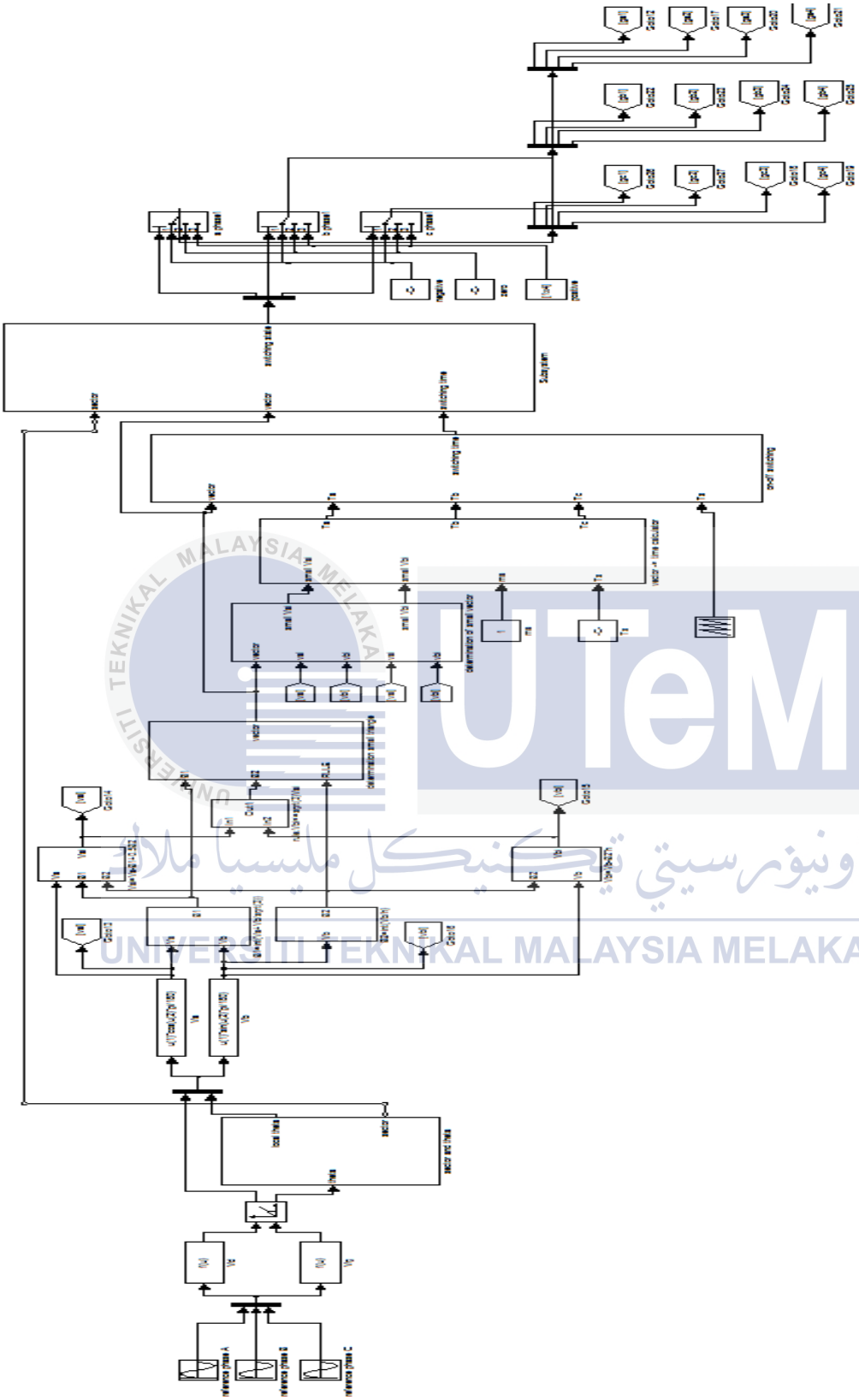


Figure 3.30: The overall schematic diagram of SVPWM

3.4 Summary

In this chapter, process constructions in Matlab/SIMULINK for two-level SVPWM, three-level SVPWM, SPWM and MSPWM algorithms have been analysed. MSPWM is a control switching modulation that extended from SPWM, the switching control method of MSPWM is same as SPWM. Besides that, It is clearly demonstrated that operation of SVPWM is more complicated compared to SPWM or MSPWM. Operation of SVPWM become more complex when the number of output voltage levels involved is increased. Meanwhile, the complexity level of SPWM does not increases even the number of output voltage levels is increased.

CHAPTER 4

ANALYSIS AND DISCUSSION

4.1 Introduction

Output voltage and current are the most important feature that used to define the performance of topologies and switching modulation. Types of topologies that would be discussed on this chapter are two-level conventional inverter, three-level neutral point clamped and five-level neutral point clamped multilevel inverters. This chapter is divided into four parts; the first part is discussed the two-level inverter, second part discussed about three-level neutral point clamped multilevel inverter, the third part is about five-level neutral point clamped multilevel inverter, and the final part is discussed about the comparison the performance of these topologies. The part two and part three are divided into two sections; the first section is an analysis THD level of the output and the second part is discussed about the balancing of DC-link capacitor voltage.

4.2 Two-level Conventional Inverter

The modeling of the two-level conventional inverter has been implemented in Matlab/SIMULINK and the schematic diagram is illustrated in Figure 4.1. In the analysis of two-level conventional inverter, sinusoidal pulse-width modulation (SPWM) and two-level space vector pulse-width modulation (SVPWM) have been employed to control switches of the two-level inverter. THD analysis of output line voltage and current have been performed in this section. The significant design parameters were as follows Table 4.1.

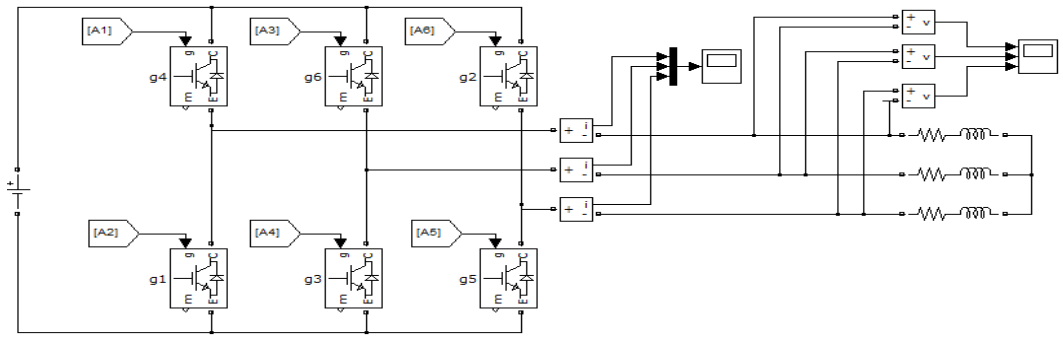


Figure 4.1: Modelling of the two-level conventional inverter

Table 4.1: Important simulation parameter of two-level inverter

Parameters	Values
DC input	400 V
Resistive load	5Ω
Inductive load	25mH

This conventional inverter is known as two-level inverter is because the phase output that generated are only – ½ V_{dc} and ½ V_{dc}. The simulation output of two-level inverter that follows the parameters in Table 4.1 is presented in figure 4.2, simulation phase output value results are -200V and 200V.

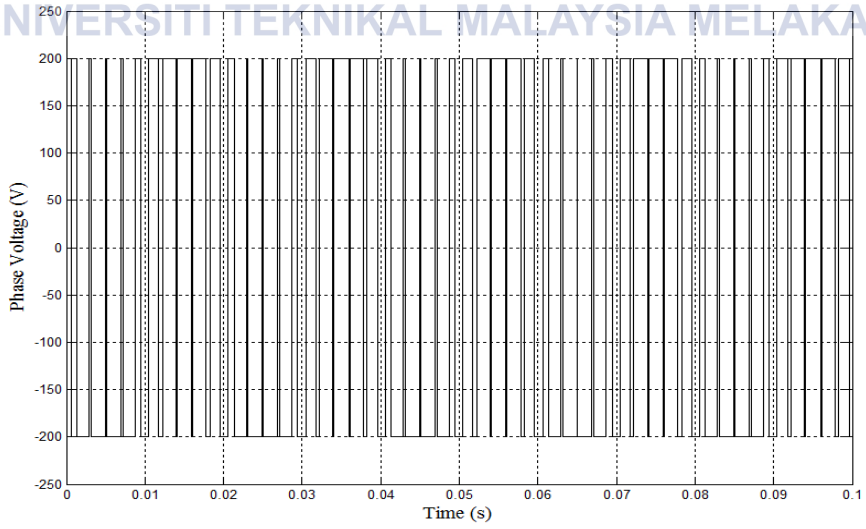
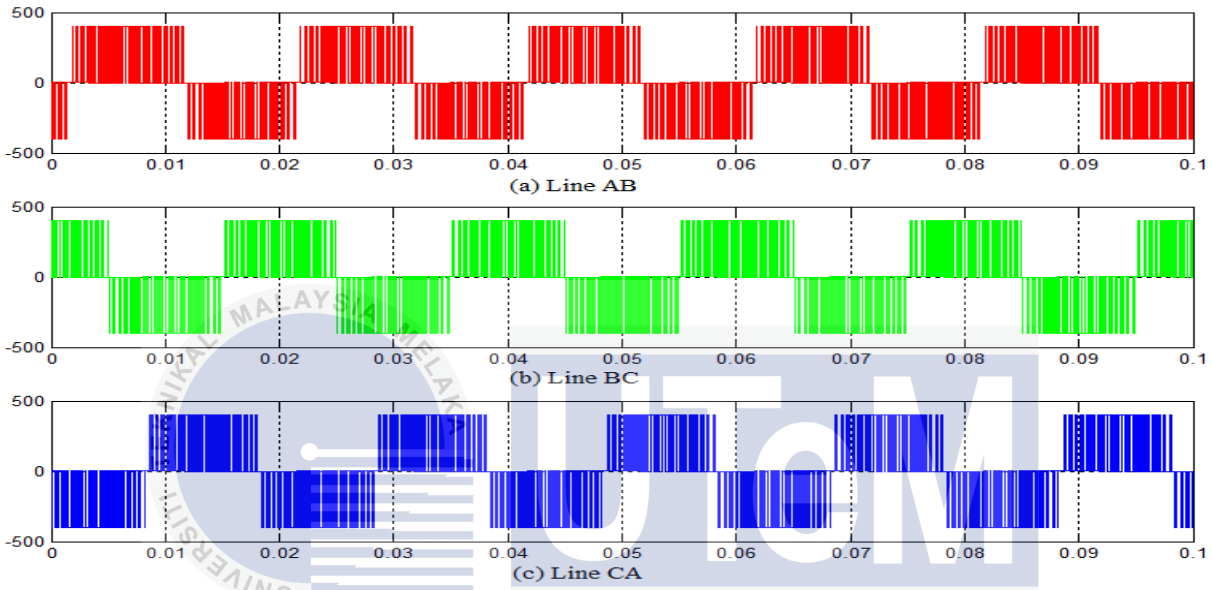
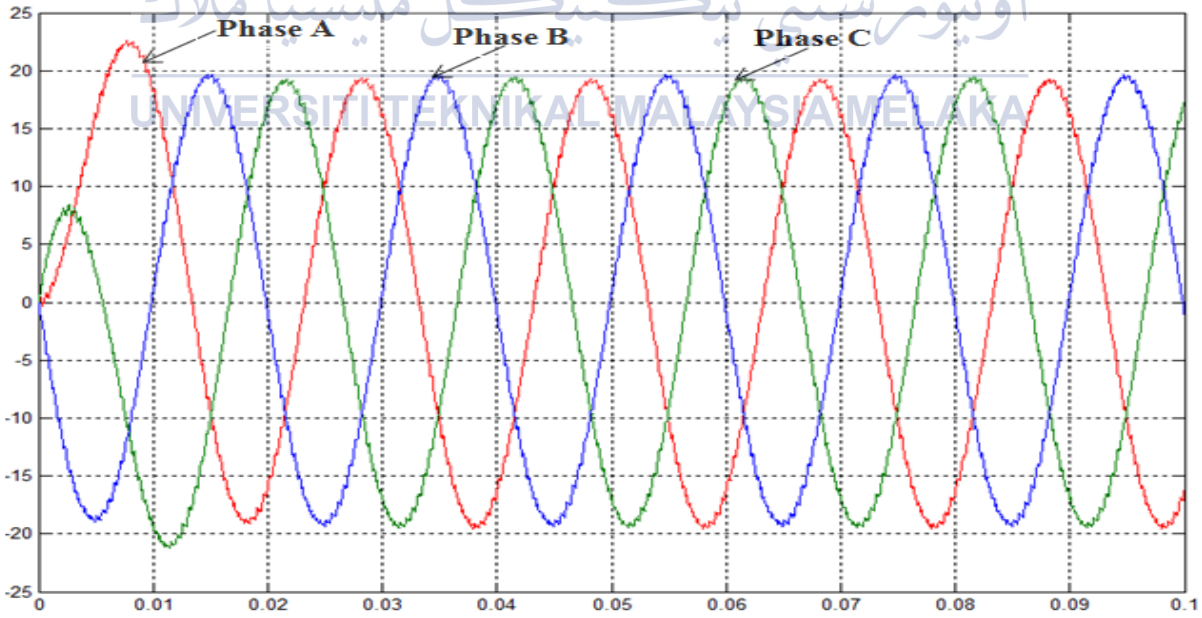


Figure 4.2: Phase voltage of two-level conventional inverter

Simulated output line voltage and current waveform of two-level SPWM on the two-level conventional inverter with parameters of 2 kHz switching frequency and modulation index of 0.9 have been depicted in Figure 4.3. The THD voltage of the simulation is 80.03%; while the THD current of the simulation is 1.53%. Fast Fourier Transform (FFT) of the simulation is illustrated in Appendix A.



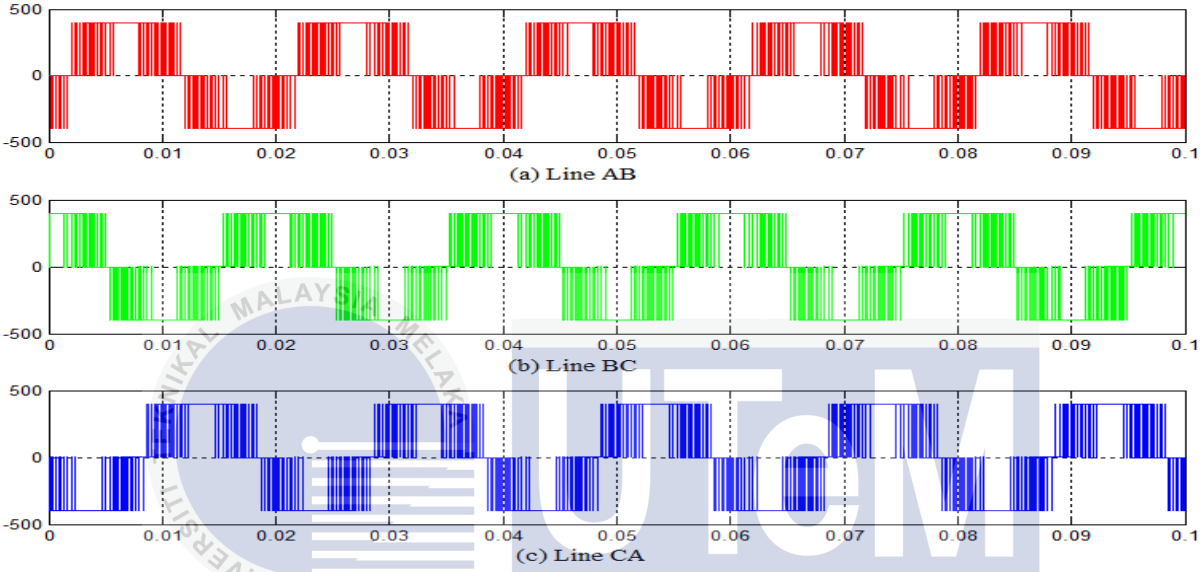
(a) Simulated line voltage waveform of SPWM



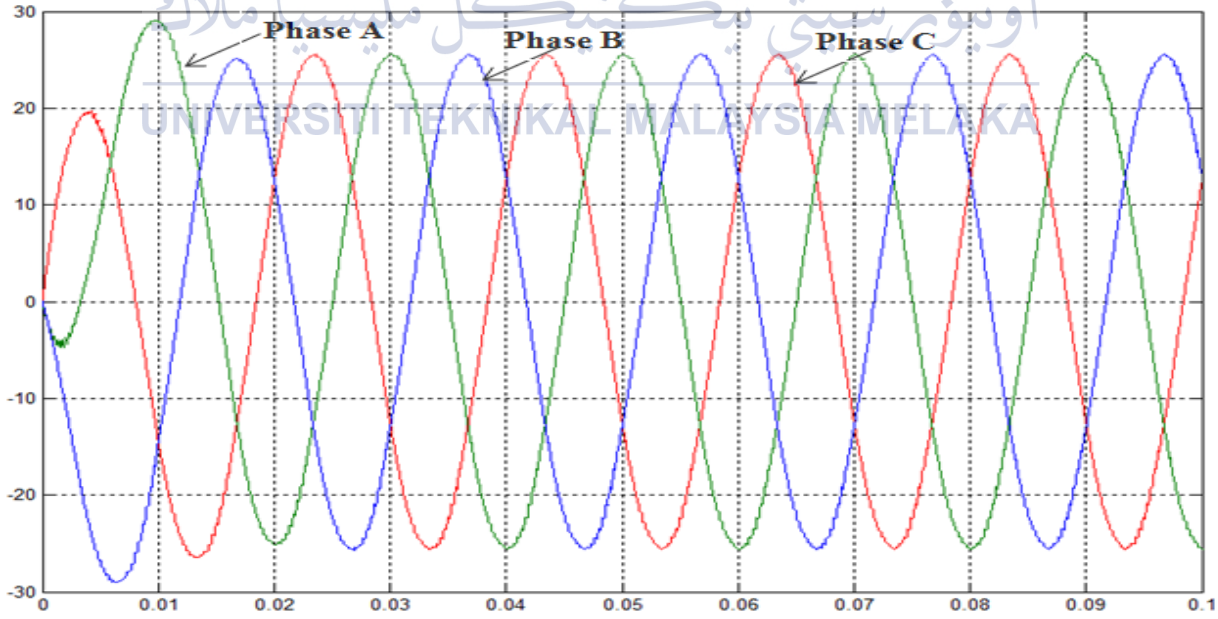
(a) Simulated output current waveform of SPWM

Figure 4.3: Simulation output waveforms of SPWM

The simulation of output voltage and current waveform of two-level SVPWM on the two-level conventional inverter with parameters of 2 kHz switching frequency and modulation index of 0.9 have been depicted in Figure 4.4. The THD voltage of the simulation is 47.32%, while the THD current of the simulation is 1.09%. FFT of the simulation is shown in Appendix B.



(a) Simulated line voltage of two-level SVPWM



(b) Simulated output current of two-level SVPWM

Figure 4.4: Simulation output waveforms of two-level SVPWM

4.2.1 THD Analysis of Two-Level Conventional Inverter

Performances of two-level SPWM and SVPWM switching modulations in terms of total harmonic distortion (THD) for output line voltage and output current with different switching frequencies ranging from 1 kHz to 5 kHz have been analysed. Meanwhile, modulation index is set at 0.90 for all switching frequencies and this inverter is connected to a balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.5 and Figure 4.6 show the comparison of the THD level for line voltage and output voltage with different switching frequency.

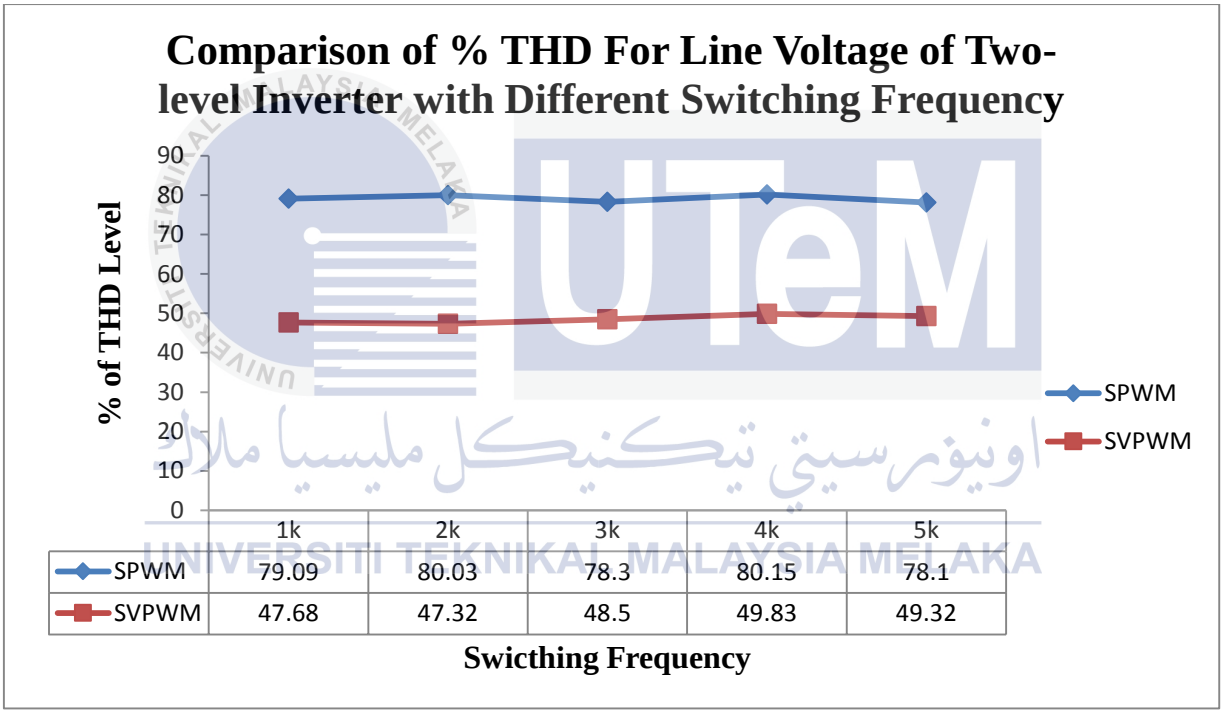


Figure 4.5: Simulation with varying switching frequency from 1 kHz to 5 kHz for line voltage

According to Figure 4.5, the line voltage performs almost a linear relationship with increases in switching frequency. The average THD voltage of SPWM is around 79% and average THD voltage of SVPWM is around 48.5%. Besides that, from Figure 4.5, it can be concluded that SVPWM switching modulation is the best control method for two-level conventional inverter since it would bring out the lower THD voltage of production quality compared to the SPWM switching modulation.

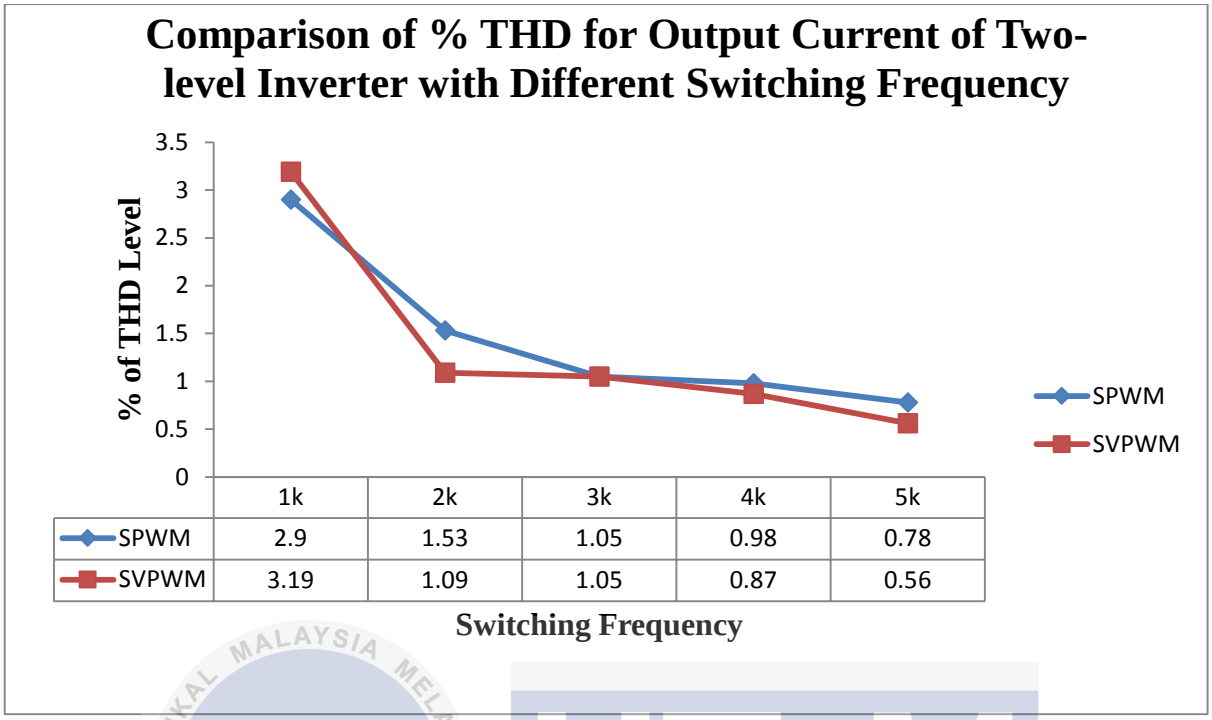
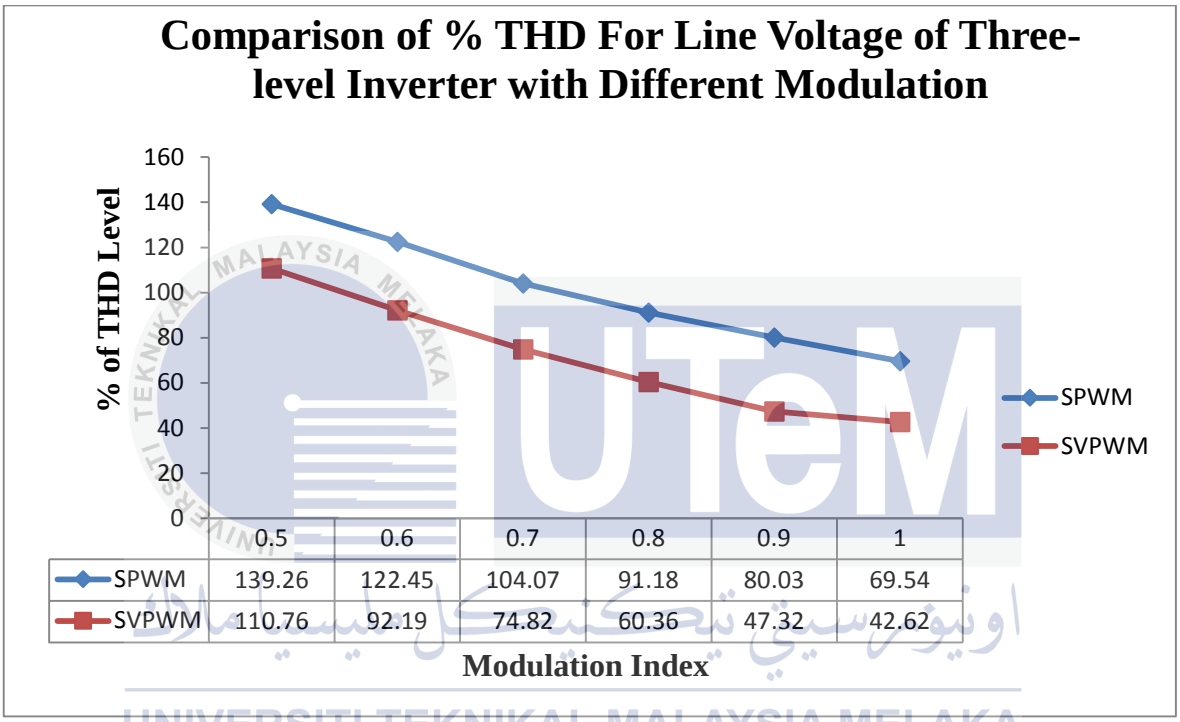


Figure 4.6: Simulation with varying switching frequency from 1 kHz to 5 kHz for output current

From Figure 4.6, the THD current of two-level inverter is decreased by increasing the switching frequency. Analysis indicates that the higher the switching frequency would produce the lower percentages of THD current quality, and the lower switching frequency would produce higher THD current quality. For two-level SVPWM, the THD current during 1 kHz is 3.19%; while the THD current during 5 kHz is 0.56%. Another obvious significance can be easily observed from Figure 4.6 is the THD levels of both switching modulations were reduced sharply with switching frequency increases from 1 kHz to 2 kHz. For two-level SVPWM, the THD current is reduced from 3.19% to 1.09% when the switching frequency increases from 1 kHz to 2 kHz.

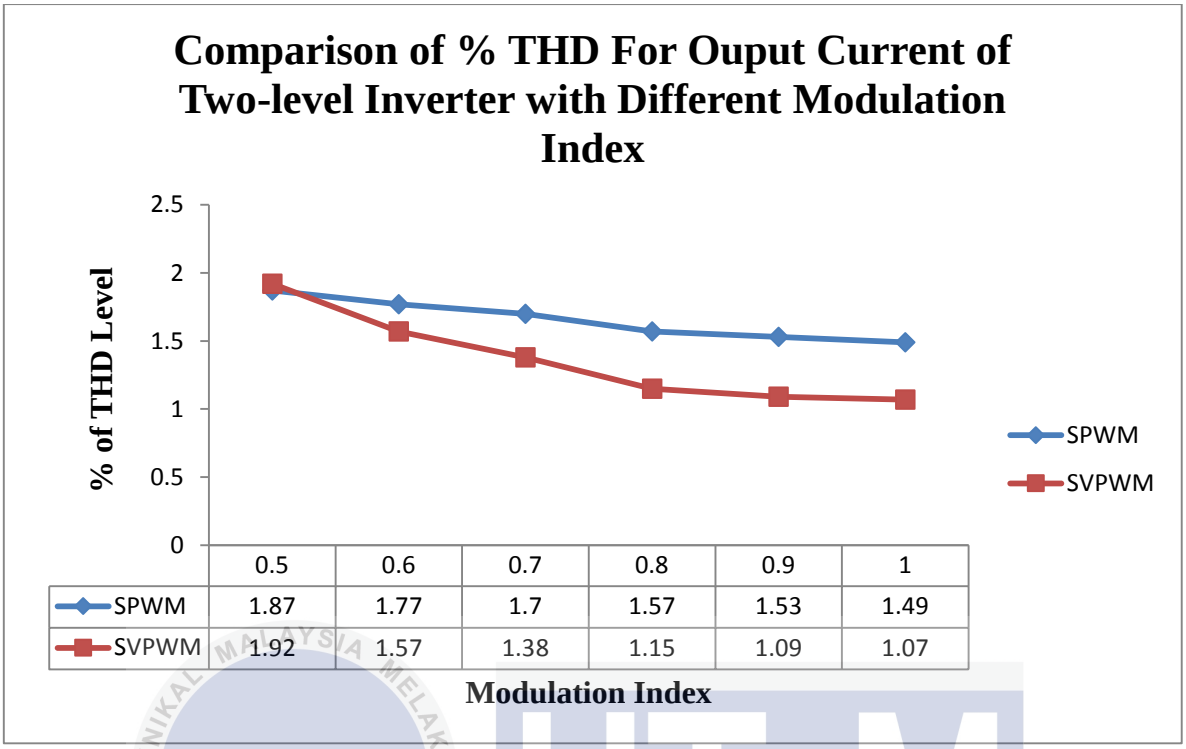
Next, THD analysis with fixed switching frequency 2 kHz against modulation index that varied from 0.5 to 1.0 for both two-level SVPWM and SPWM switching modulation have been observed. Meanwhile, two-level inverter system is connected to a balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.7 and Figure 4.8 shows the comparison of percentages of THD for line voltage and output current with different modulation index.



	0.5	0.6	0.7	0.8	0.9	1
SPWM	139.26	122.45	104.07	91.18	80.03	69.54
SVPWM	110.76	92.19	74.82	60.36	47.32	42.62

Figure 4.7: Simulation with varying modulation index from 0.5 to 1 for line voltage

As can be seen in Figure 4.7, two obvious significances can be discovered. Firstly, the THD of the line voltage is directly influenced by the modulation index; by increasing the modulation index of the switching modulation will causes the percentages THD of the line voltage will decrease. For SPWM, the THD voltage is decreased from 139.26% to 69.54% for modulation index increased from 0.5 to 1.0. Secondly, the graph clearly indicated that the percentages of THD for two-level SVPWM are lesser than two-level SPWM with the same modulation index. For a modulation index of 0.9, it was shown that the THD voltage is significantly reduced 37.41% from two-level SPWM to two-level SVPWM, which mean the voltage quality for two-level SVPWM is better than two-level SPWM.



	0.5	0.6	0.7	0.8	0.9	1
SPWM	1.87	1.77	1.7	1.57	1.53	1.49
SVPWM	1.92	1.57	1.38	1.15	1.09	1.07

Figure 4.8: Simulation with varying modulation index from 0.5 to 1 for output current

Different modulation index on different switching modulation would results a different output current quality. As can be observed from Figure 4.8, the higher the modulation index, the lower the THD current; all the two-level switching modulation shows the characteristics of reduction in percentages of THD current with increasing in modulation index. For SPWM, the THD current is decreased from 1.87% to 1.49% when the modulation index is increases from 0.5 to 1.0. Secondly, the graph clearly demonstrates that the percentage of THD current for two-level SVPWM is lower than two-level SPWM with the same modulation index. For modulation index 0.9, the THD current of SPWM is 1.53%; while for two-level SVPWM, the THD current is only 1.09%.

4.3 Three-level Neutral Point Clamped Multilevel Inverter

A detailed analysis is done on the three-level neutral point clamped multilevel inverter (NPC-MLI) by simulating through Matlab/SIMULINK and the schematic diagram is illustrated in Figure 4.9. In the simulation of three-level NPC-MLI, multicarrier sinusoidal pulse-width modulation (MSPWM) with the control method of PD and POD switching modulation, and three-level space vector pulse-width modulation (SVPWM) have been employed to control switches of the three-level NPC-MLI. Percentages THD of output line voltage and current have been analysed, and analysis of DC-link balancing have been executed. The important design parameters were as follows Table 4.2. Switching losses will not discussed in this chapter.

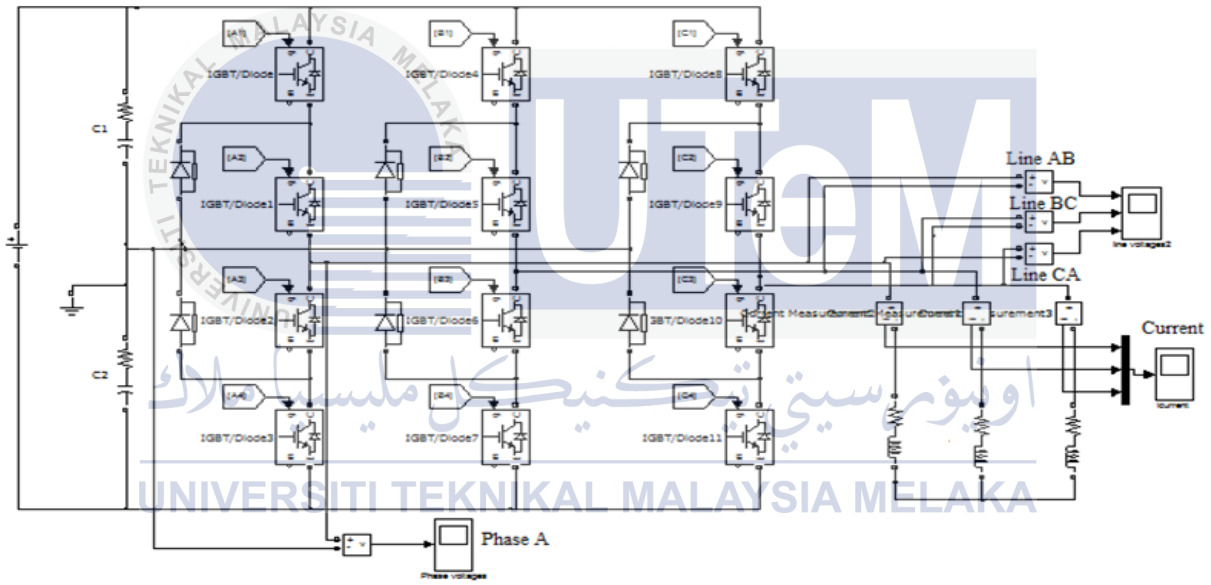


Figure 4.9: Modelling of three-level neutral point clamped

Table 4.2: Important simulation parameter of three-level NPC-MLI

Parameters	Values
DC input	800 V
DC – link capacitance	$2200\mu F$
Resistive load	5Ω
Inductive load	25mH

NPC-MLI with four switching IGBTs in one phase is known as three-level NPC-MLI, because the phase output produced is involved in 3 stages; - ½ V_{dc}, 0 and ½ V_{dc}. The phase output generated by three-level NPC-MLI with the parameter in Table 4.2 is shown in Figure 4.10, phase output result of three-level NPC-MLI are -400V, 0 and 400V.

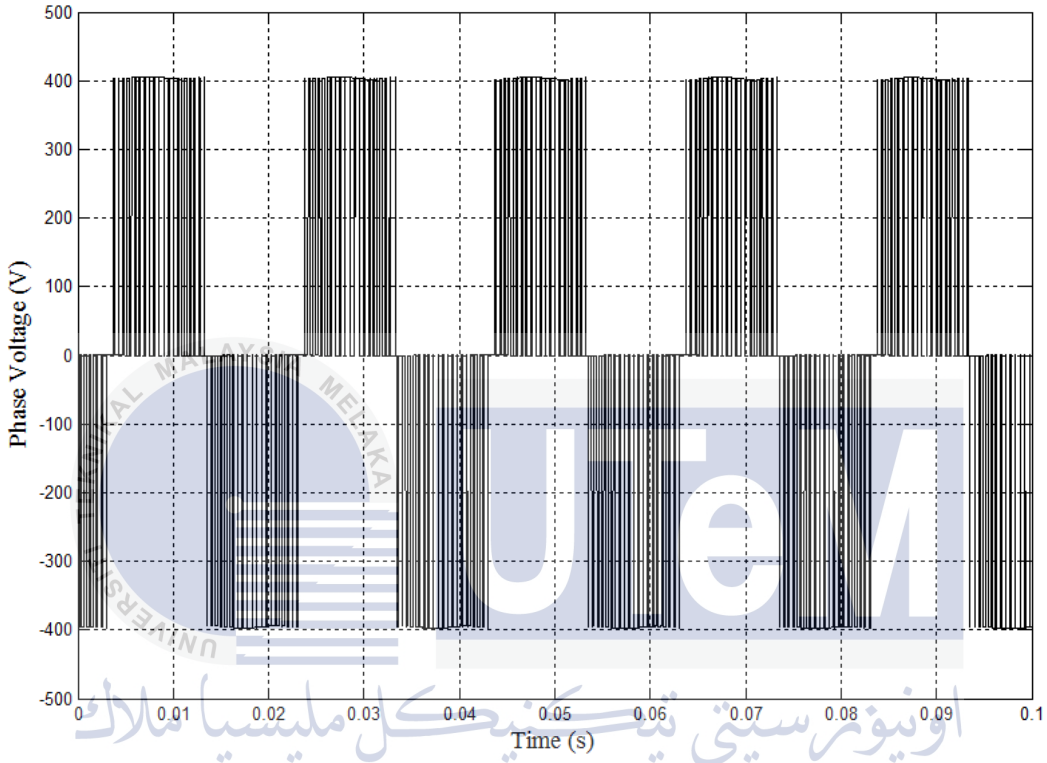
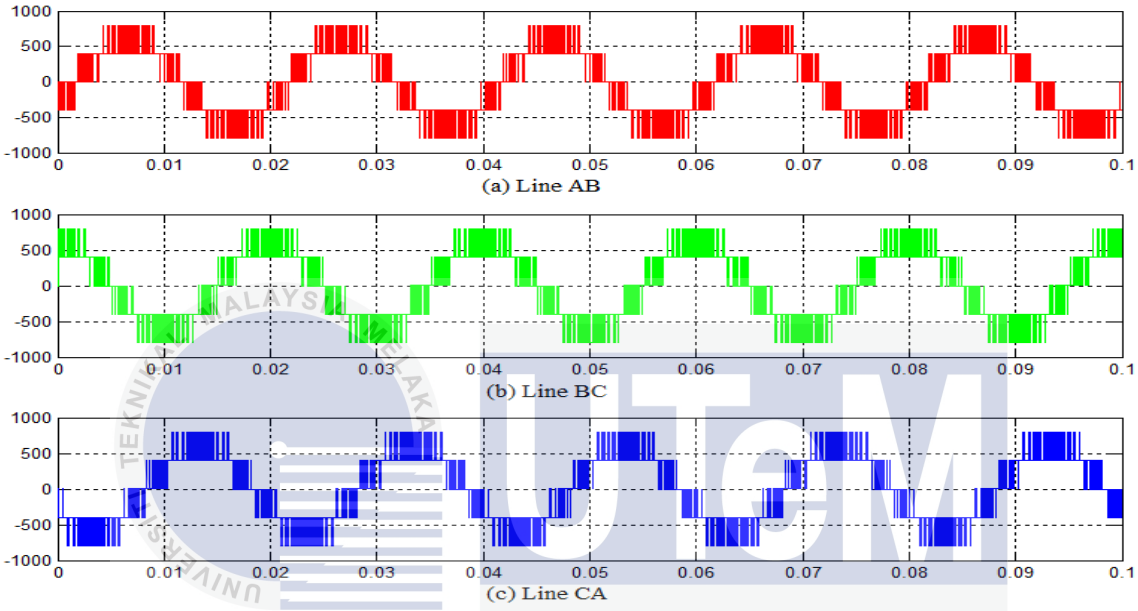
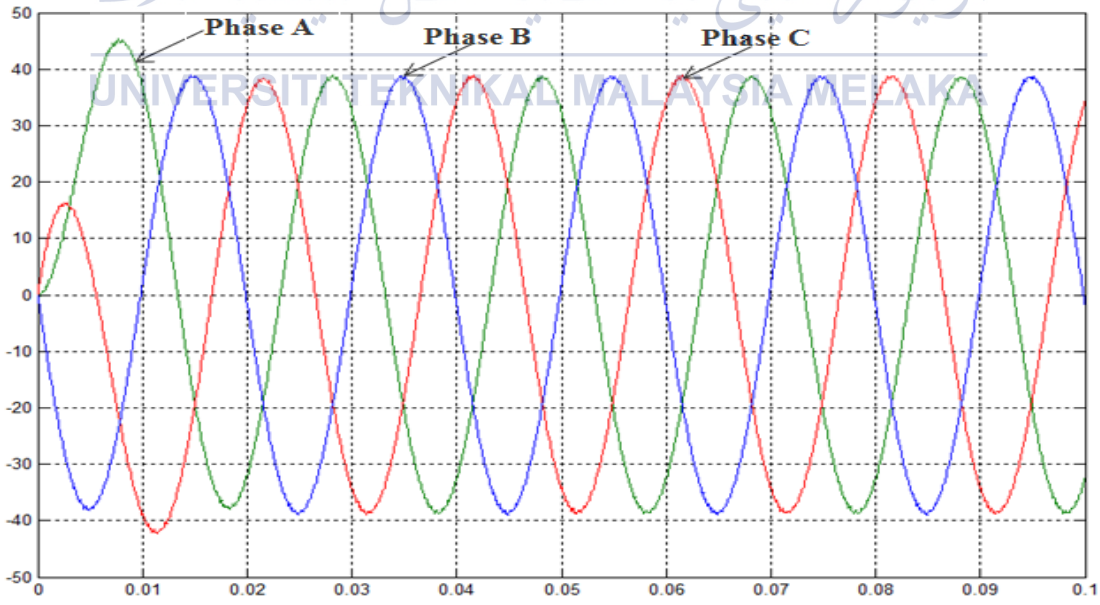


Figure 4.10: Phase voltage of three-level NPC-MLI

The simulation of output line voltage and current waveform of three-level MSPWM with control method PD switching modulation on three-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been presented in Figure 4.11. The THD voltage of the simulation is 39.35%; while the THD current of the simulation is 0.67%. FFT of the simulation is illustrated in Appendix C



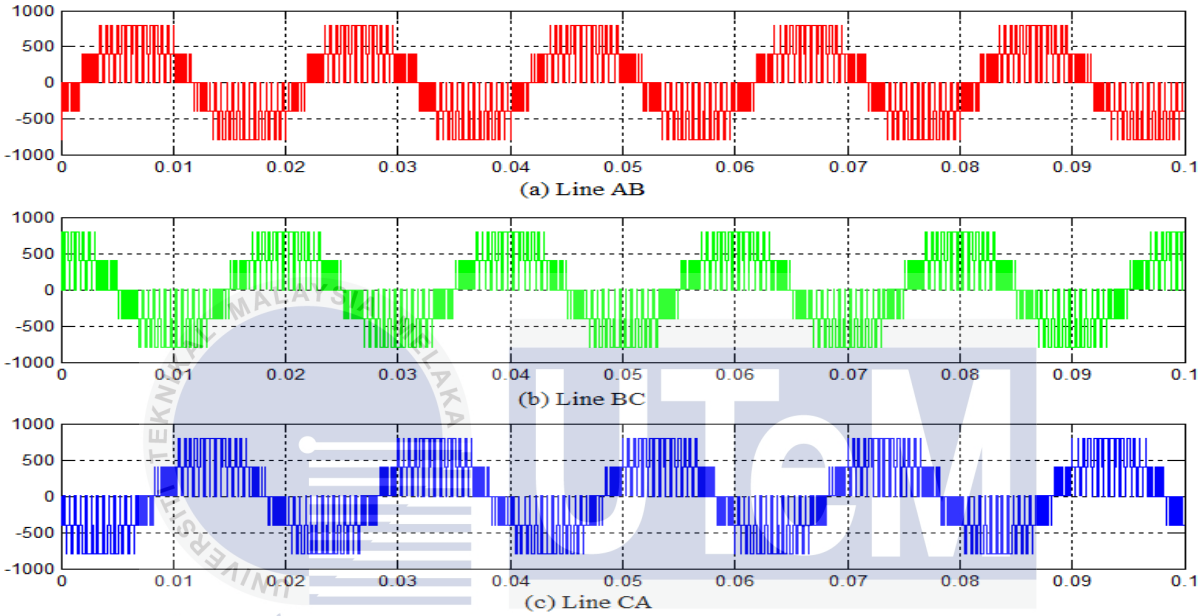
(a) Simulated line voltage waveform of PD switching modulation



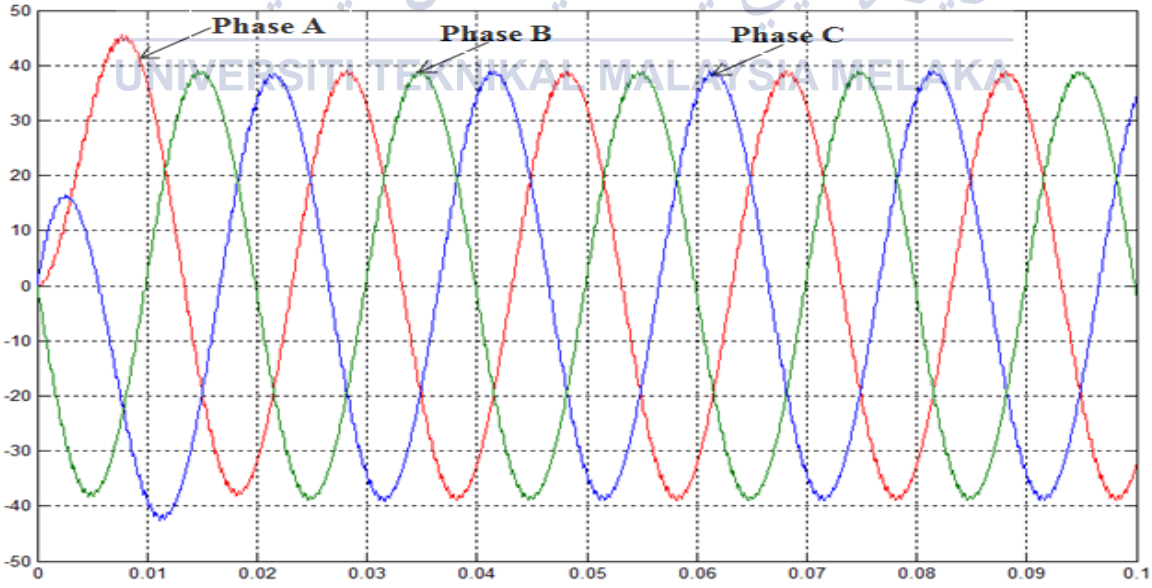
(b) Simulated output current waveform of PD switching modulation

Figure 4.11: Simulation output waveforms of PD switching modulation

Simulated output line voltage and current waveform of three-level MSPWM with control method POD switching modulation on three-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been presented in Figure 4.12. The THD voltage of the simulation is 54.15%; while the THD current of the simulation is 1.28%. FFT of the simulation is illustrated in Appendix D.



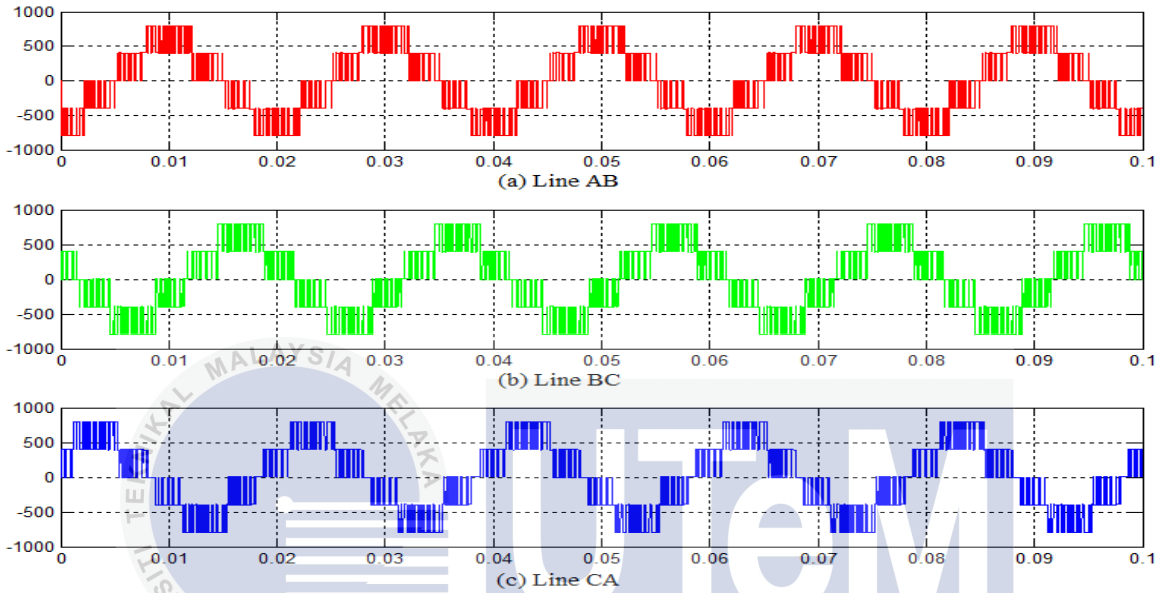
(a) Simulated line voltage waveform of POD switching modulation



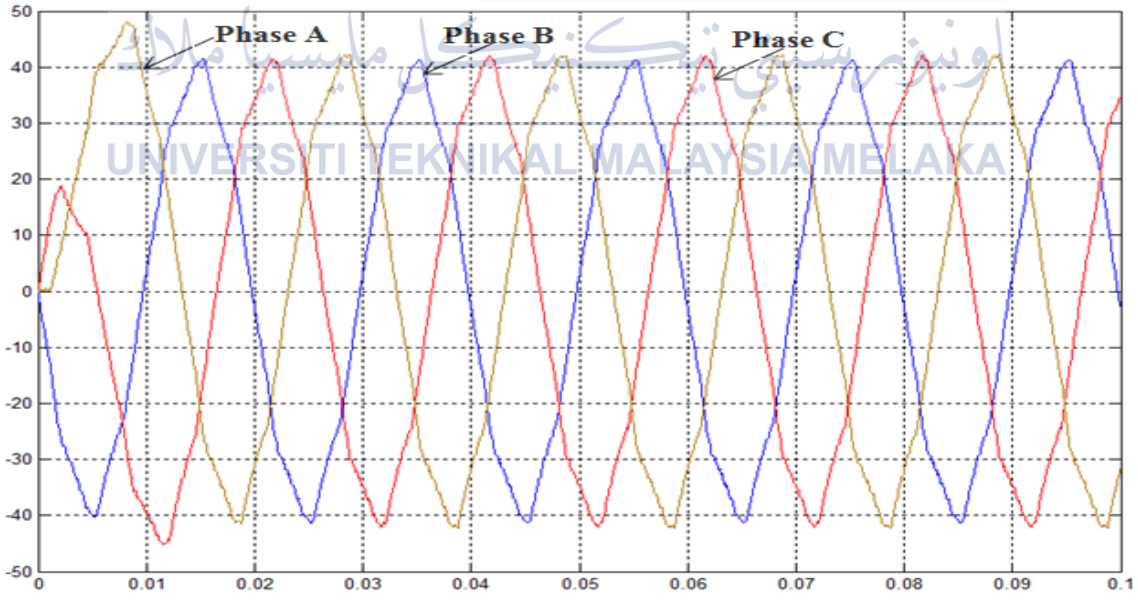
(b) Simulated output current of POD switching modulation

Figure 4.12: Simulation output waveform of POD switching modulation

Simulated output line voltage and current waveform of three-level SVPWM on three-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been illustrated in Figure 4.13. The THD voltage of the simulation is 45.60%; while the THD current of the simulation is 4.23%. FFT of the simulation is illustrated in Appendix E



(a) Simulated line voltage waveform of three-level SVPWM

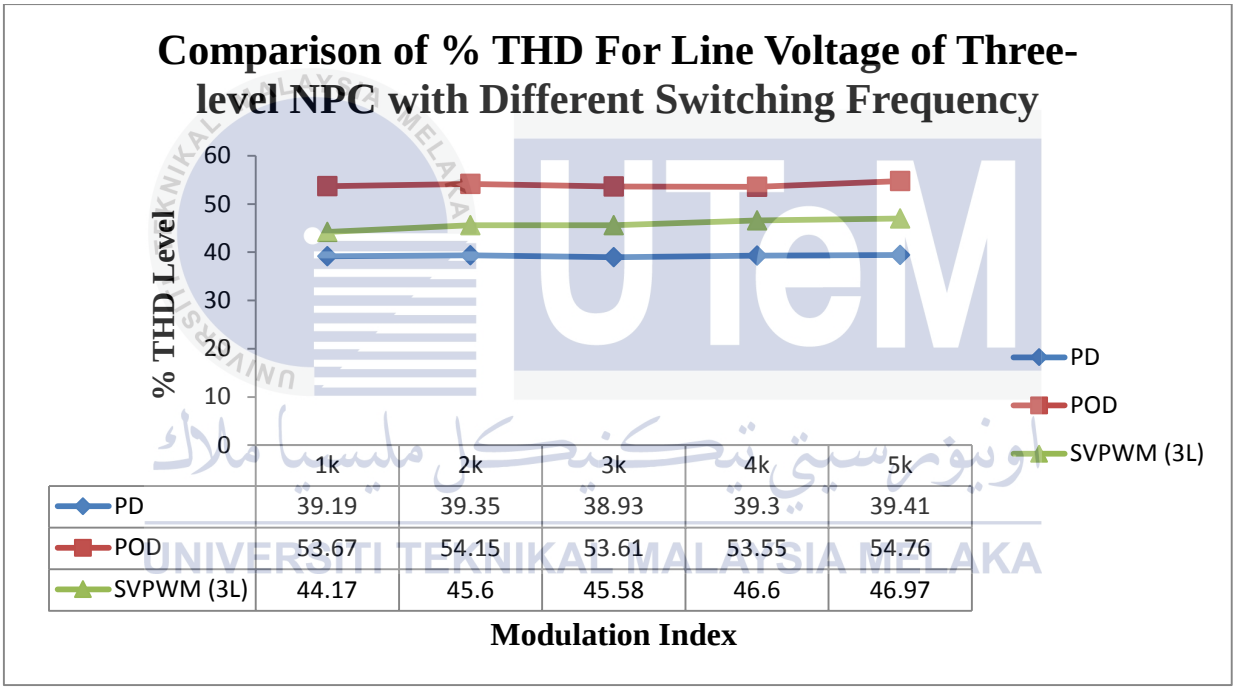


(b) Simulated output current of three-level SVPWM

Figure 4.13: Simulation output waveforms of three-level SVPWM

4.3.1 THD Analysis of Three-Level Neutral Point Clamped Multilevel Inverter

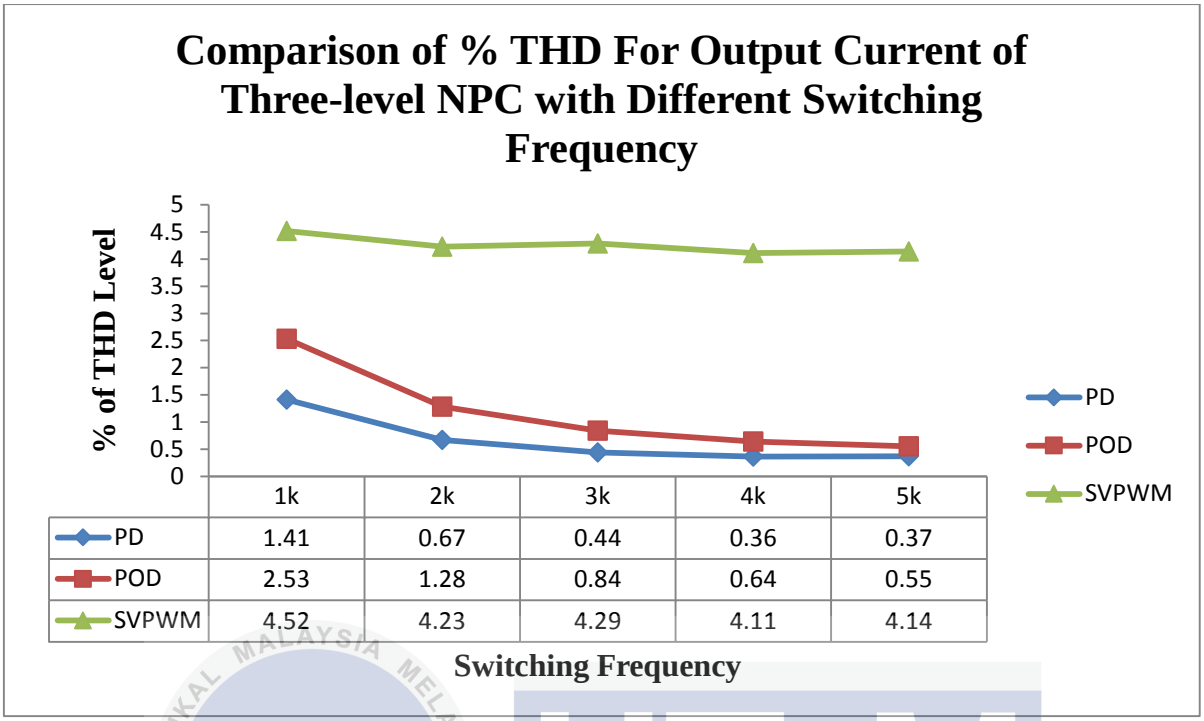
Performances of three-level switching modulation PD, POD and three-level SVPWM in terms of total harmonics distortion (THD) for output current and line voltage with fixed modulation index 0.9 and switching frequency varied from 1 kHz to 5 kHz have been analysed. Meanwhile, the three-level NPC-MLI system is connected to a balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.14 and Figure 4.15 show the comparison of percentages of THD for line voltage and output voltage with different switching frequency.



	1k	2k	3k	4k	5k
PD	39.19	39.35	38.93	39.3	39.41
POD	53.67	54.15	53.61	53.55	54.76
SVPWM (3L)	44.17	45.6	45.58	46.6	46.97

Figure 4.14: Simulation with varying switching frequency from 1kHz to 5kHz for line voltage

According to Figure 4.14, the THD voltage of all switching modulation is independent with the change in switching frequency increases from 1 kHz to 5 kHz. The line voltage performs almost a linear relationship with the change of switching frequency. The average THD voltage of PD, POD and three-level SVPWM are 39.38%, 53.98% and 45.78%, respectively. Besides that, Figure 4.14 also reveal the fact that PD switching modulation would produce the lower THD voltage around 39.38%; while, the POD switching modulation generated the higher THD voltage around 53.98%.

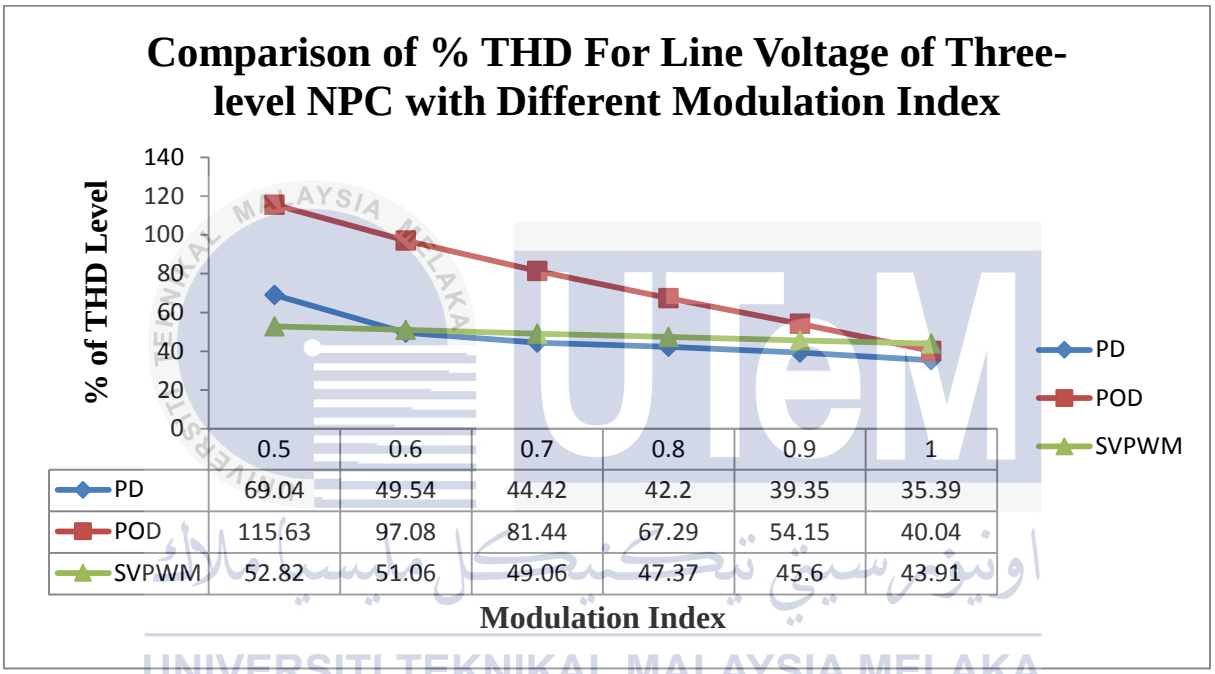


	1k	2k	3k	4k	5k
PD	1.41	0.67	0.44	0.36	0.37
POD	2.53	1.28	0.84	0.64	0.55
SVPWM	4.52	4.23	4.29	4.11	4.14

Figure 4.15: simulation with varying switching frequency from 1kHz to 5kHz for output current

From Figure 4.15, one of the obvious significances can be easily observed which is the percentage of THD output current can be reduced easily by increasing the switching frequency. Lower switching frequency would generate higher value THD current but higher switching frequency produced lower value THD current. For switching modulation POD, the THD current was significantly reduced from 2.53% to 0.55% when the switching frequency is increased from 1 kHz to 5 kHz. However, three-level SVPWM does not show a very distinct reduction in THD level compared to the MSPWM switching modulation. The THD current was just drop 0.38% when the switching frequency is increase from 1 kHz to 5 kHz, but the THD current of PD switching was significant drop 1.04%. Besides that, Figure 4.15 also illustrates that the output current of three-level SVPWM has the highest percentages of THD compared with other MSPWM switching modulation. This fact can be explained by the performance of three-level SVPWM is depends on which SVPWM approaches that been adopted, since many approaches of three-level SVPWM had been proposed by many researchers just for simplification, different approaches have different achievement.

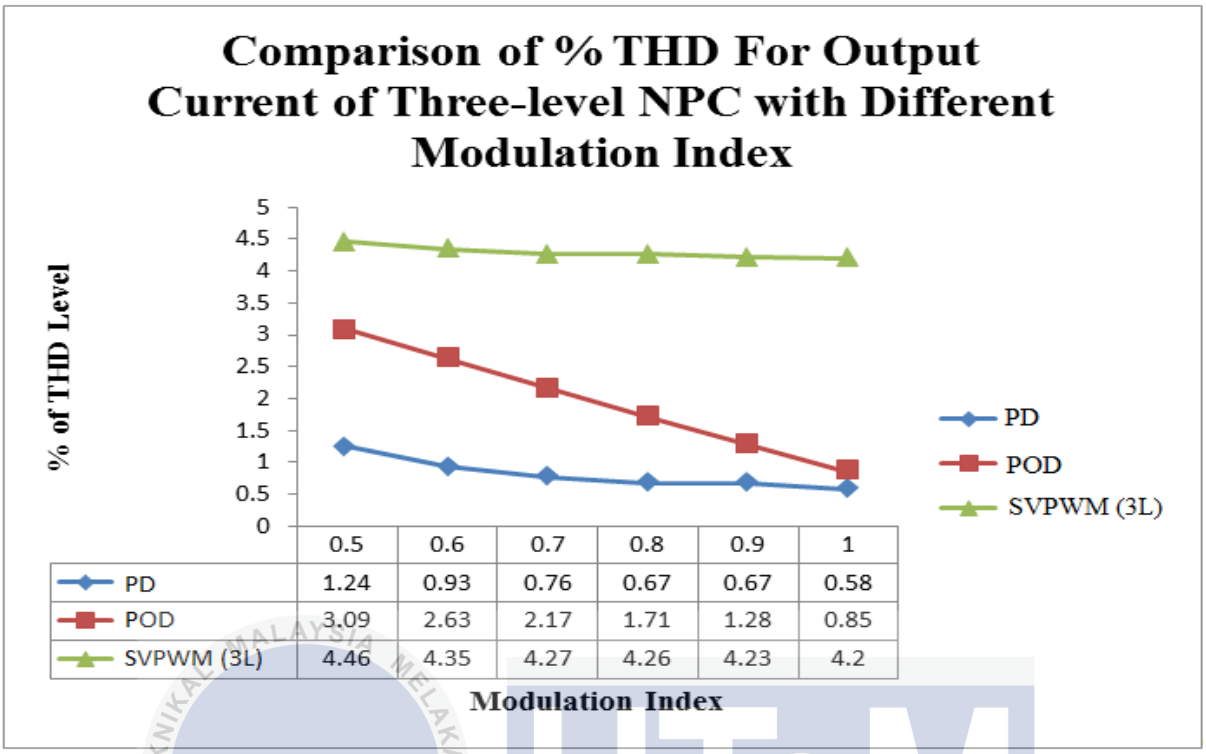
Performances of three-level switching modulation PD, POD and three-level SVPWM in terms of total harmonics distortion (THD) for output line voltage and current with modulation index varied from 0.5 to 1.0 have been observed. Meanwhile, the system is simulated with switching frequency fixed at 2 kHz and connected to a balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.16 and Figure 4.17 shows the comparison of percentages of THD for line voltage and output voltage with different modulation index.



	0.5	0.6	0.7	0.8	0.9	1
PD	69.04	49.54	44.42	42.2	39.35	35.39
POD	115.63	97.08	81.44	67.29	54.15	40.04
SVPWM	52.82	51.06	49.06	47.37	45.6	43.91

Figure 4.16: Simulation with varying modulation index from 0.5 to 1 for line voltage

As can be observed in Figure 4.16, that percentages THD of line voltage can be easily reduced by increasing the modulation index. For PD switching modulation, the THD voltage was significant drop about 33.65% when the modulation index is increased from 0.5 to 1.0. The second observation in Figure 4.16 is the POD switching modulation shows the characteristics of having the highest percentages of THD comparing with other three-level switching modulation and decreases most rapidly by increasing modulation index. For POD switching modulation, the percentage THD voltage is 115.63% during modulation index of 0.5, but THD voltage drop to 40.04% when the modulation index is increased to 1.0; it shows significant decrease about 75.59%



	0.5	0.6	0.7	0.8	0.9	1
PD	1.24	0.93	0.76	0.67	0.67	0.58
POD	3.09	2.63	2.17	1.71	1.28	0.85
SVPWM (3L)	4.46	4.35	4.27	4.26	4.23	4.2

Figure 4.17: Simulation with varying modulation index from 0.5 to 1 for output current

As is clear from Figure 4.17, all the switching modulation shows the characteristics of reduction in percentages of THD level with increases modulation index. For PD switching modulation, the THD current is 1.24% when the modulation index is 0.5, but it reduced to 0.58% when the modulation index is increased to 1.0. Besides that, that a few scenarios been observed from the Figure 4.17; the first scenario is the PD switching modulation shows the characteristics of lower THD current; and second scenario is SVPWM switching modulation shows the higher percentages of THD current. The THD current of three-level SVPWM is 3.56% higher than PD switching modulation during the modulation index is 0.9. But output current of PD switching modulation and three-level SVPWM show the same distinct of slow reduction in THD level with increasing modulation index. The last scenario is POD switching modulation shows the most rapid reduction in THD level with increases modulation index, while other two three-level switching modulation show a slow reduction in THD level.

4.3.2 Balancing Of Three-Level Neutral Point Clamped Multilevel Inverter

The greatest concern of neutral point clamped multilevel inverter is the DC-link imbalanced capacitor voltage problem. Theoretically, the input voltage should divided equally among the capacitors, but somehow the voltage divided unevenly among the capacitors. Different switching modulations have different way to distribute voltage among capacitors. Many solutions have been proposed to deal with this voltage imbalance problem. One of the solutions is adding the additional circuit in front of the capacitors as shown in Figure 4.18 [83]. However, suitable switching technique must work together with an additional semiconductor to solve the voltage imbalance problem as illustrated in Figure 4.19.

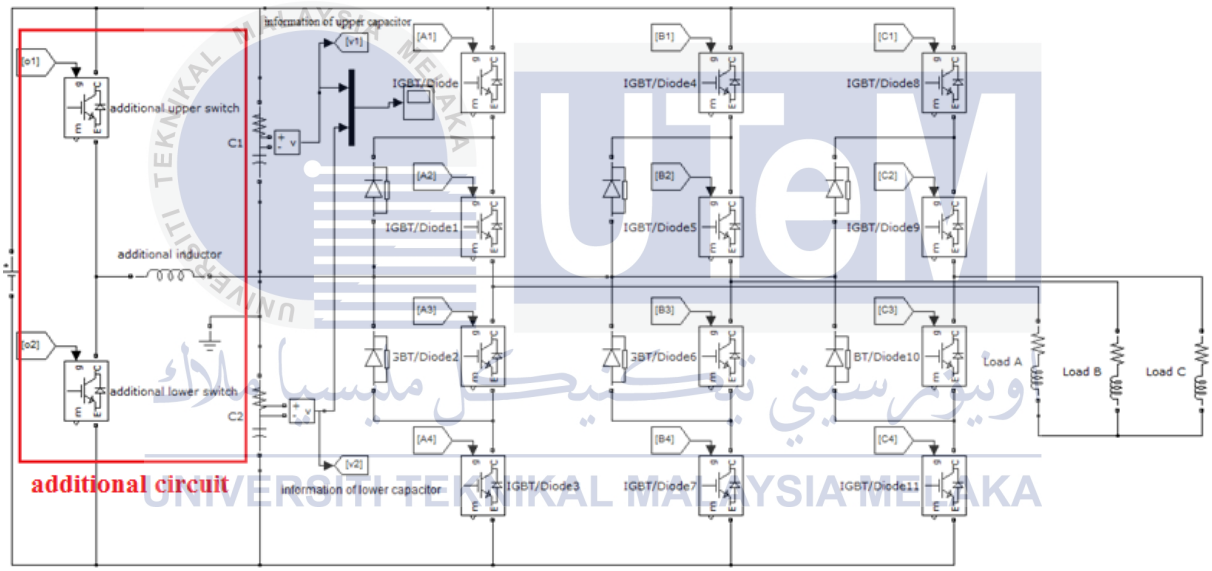


Figure 4.18: Additional circuit on three-level NPC-MLI

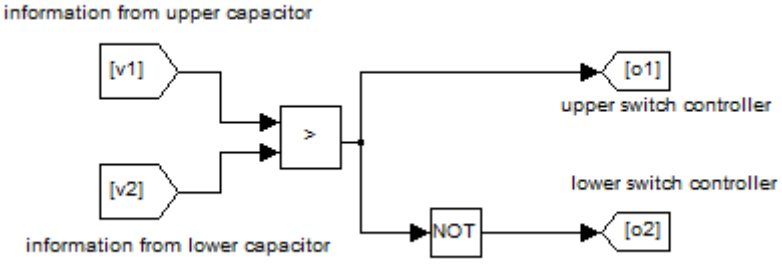


Figure 4.19: Switching technique for additional circuit

The working principle of these additional circuit is combinational of principle of boost and buck converter that based on the information gain from the capacitors voltage. When upper capacitor voltage is greater than lower capacitor voltage, the additional circuit operated as buck converter and upper switch is turned on. The second condition is when the upper capacitor voltage is lower than the lower capacitor voltage; the additional circuit operated as boost converter and lower switch is turned on. This method can regulate lower capacitor voltage and quickly balanced the voltage split among capacitor [83]. The balancing effect of additional circuit for switching modulation PD is shown in Figure 4.20. Before adding the additional circuit, instead oscillated between 400V, the lower capacitor voltage oscillated in 395V; and the upper capacitor voltage oscillated in 405V. However, after adding the additional circuit, both of the upper capacitor and lower capacitor have been re-adjust and oscillated between 400V.

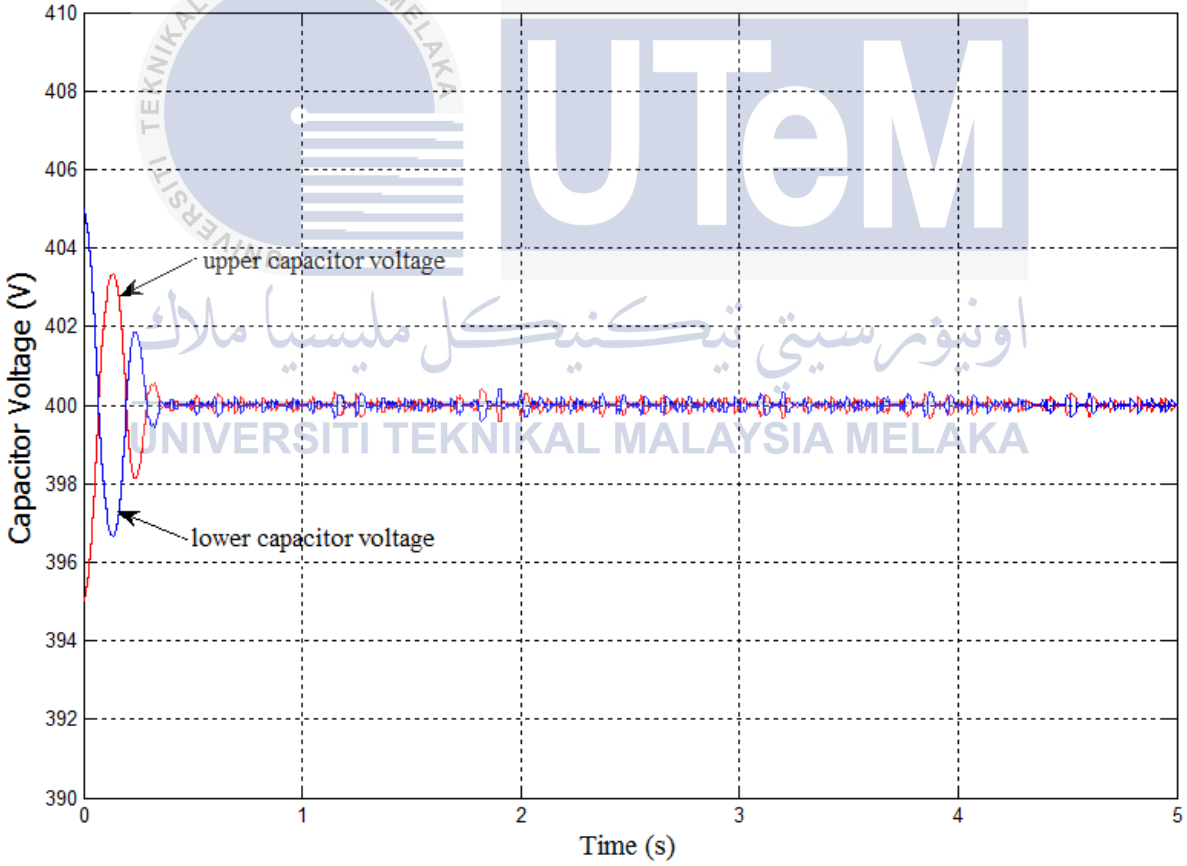


Figure 4.20: Voltage split among the capacitor with method PD after additional circuit

The advantage of this additional circuit not only can regulate the capacitor voltage but also can reduce the DC-link capacitor value from 2200µF to 330µF without effect on output voltage [83]. The output voltage waveform of 330µF DC-link capacitors with and without additional circuit is presented in Figure 4.21. As can be observed in Figure 4.21, without the additional circuit, the output voltage is badly distorted with 330µF DC-link capacitors, but the output voltage of 330µF DC-link capacitors with the additional circuit is same with 2200µF DC-link capacitors.

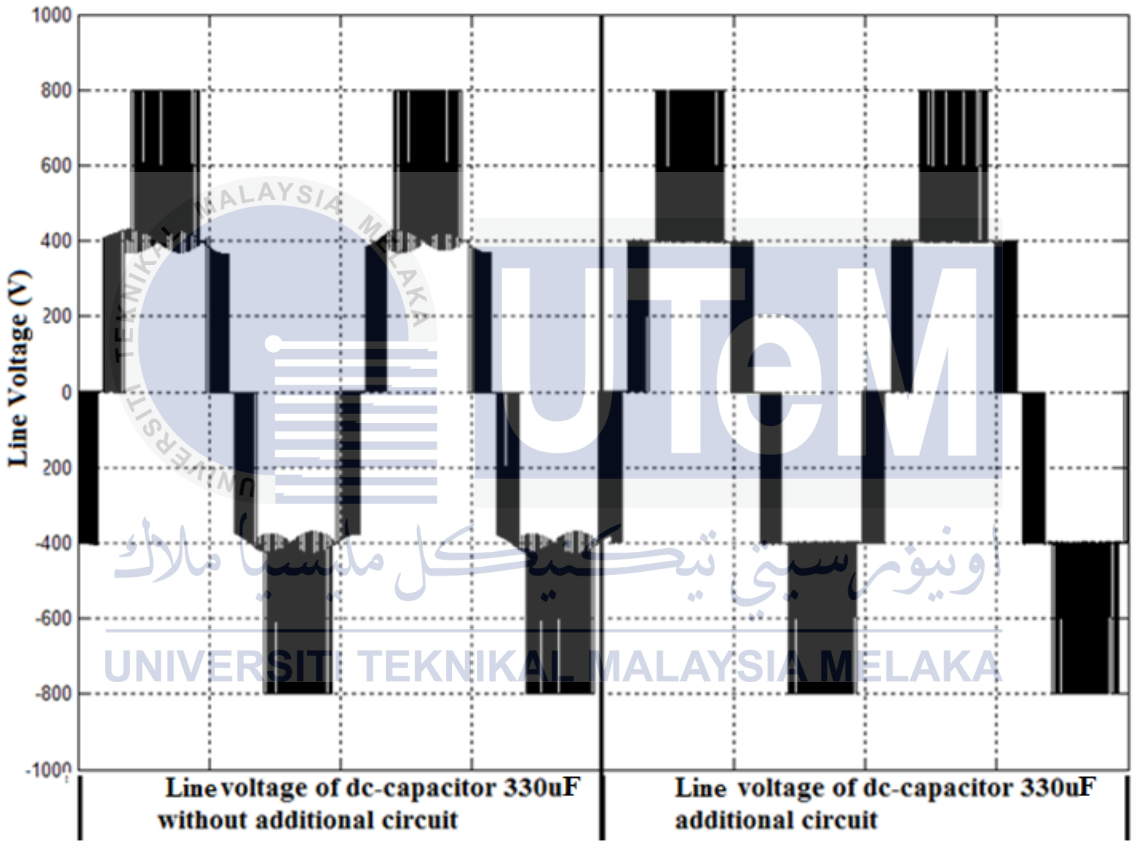


Figure 4.21: Comparison output voltage with 330µF

The simulation balancing result by using the POD modulation technique is shown in Figure 4.22. POD switching modulation is the only three-level SPWM switching method that shows the characteristics of self-balancing, which is obtained the input voltage split equally between capacitor naturally. POD switching modulation is one of the switching techniques that satisfy the natural balancing requirements, even though the THD level is highest among three-level switching method.

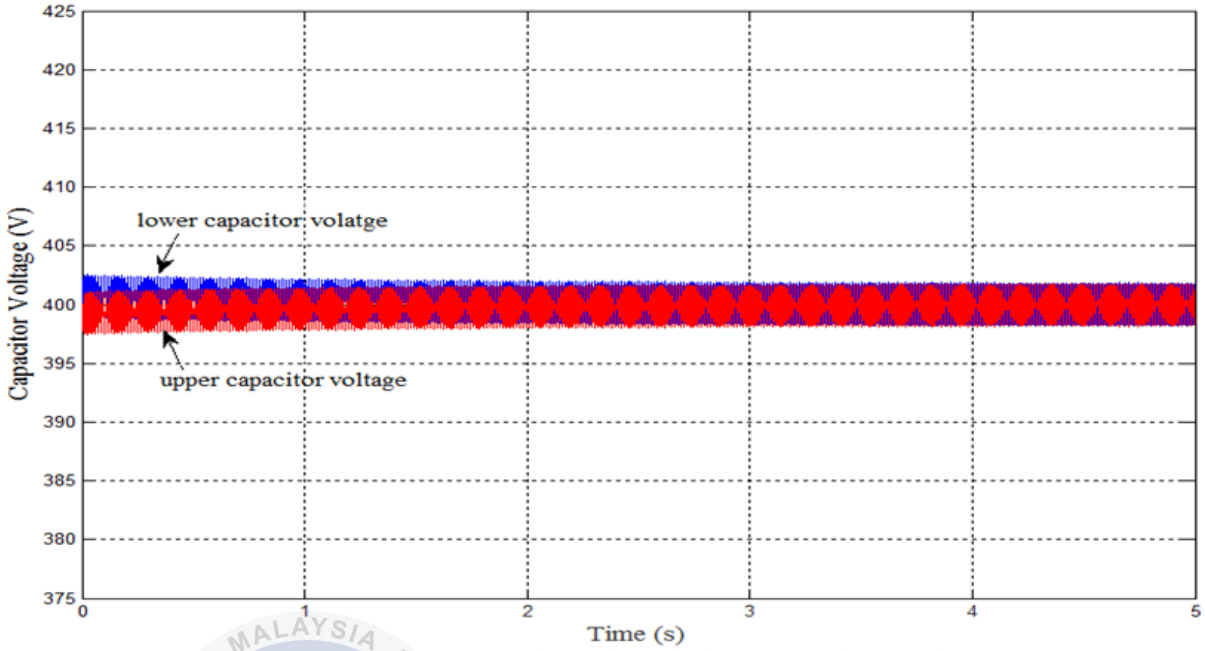


Figure 4.22: Voltage split among capacitor by method POD

The advantage of adopted three-level SVPWM in three-level NPC-MLI is the self-balancing effect without any additional circuit or other approaches. The simulation result by applying three-level SVPWM is shown in Figure 4.23. As shown in Figure 4.23, both the upper capacitor and lower capacitor voltage are oscillated between 400V.

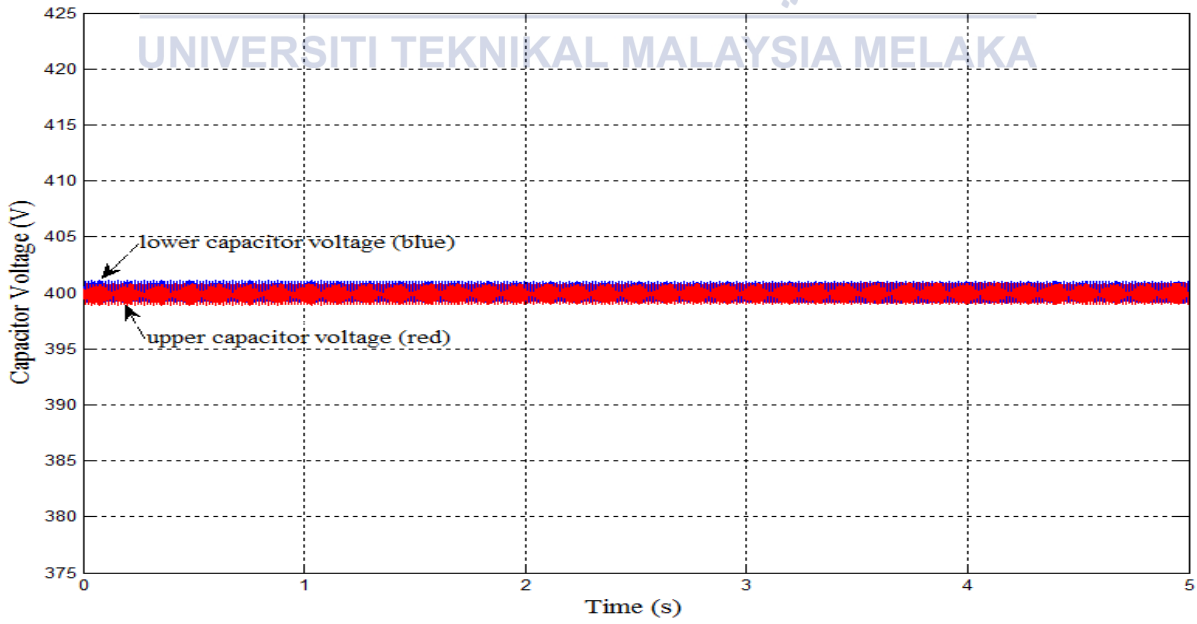


Figure 4.23: Self-balancing effect of three-level SVPWM

4.4 Five-level Neutral Point Clamped Multilevel Inverter

Simulation studies are carried out in Matlab/SIMULINK to analysis performances of the neutral point clamped multilevel inverter (NPC-MLI) that based on five-level and the schematic diagram is illustrated in Figure 4.24. In the analytical studies of five-level NPC-MLI, only the MSPWM switching modulation with PD, POD and APOD switching modulation been implemented to control switches of the five-level NPC-MLI. In the case of five-level NPC-MLI, THD analysis of output voltage and current, and analysis of DC-link balancing have been performed. The main parameters of the system are shown in Table 4.3.

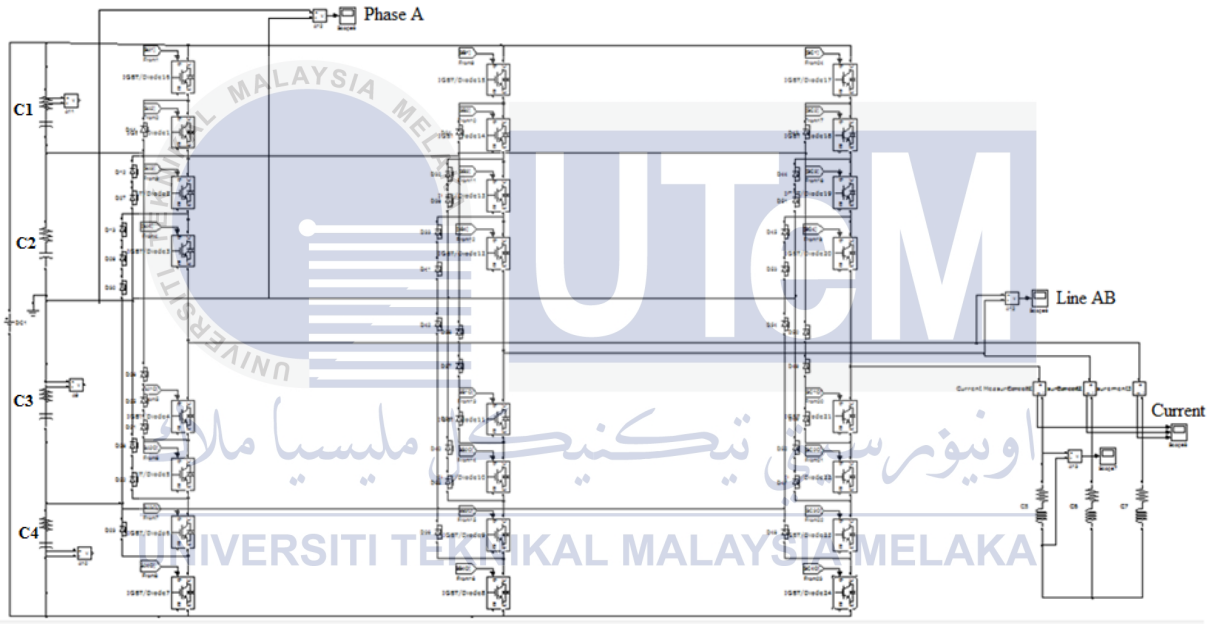


Figure 4.24: Modelling of five-level neutral-point-clamped

Table 4.3: Important simulation parameter of five-level NPC-MLI

Parameters	Values
DC input	800 V
DC – link capacitance	2200μF
Resistive load	5Ω
Inductive load	25mH

The NPC-MLI which contains eight switching IGBTs in one phase is known as five-level NPC-MLI, because the phase output generated is involved in five stages, which is –½ V_{dc}, -¼ V_{dc}, 0, ¼ V_{dc} and ½ V_{dc}. The simulation output result of five-level NPC-MLI based on parameter of Table 4.3 is depicted in Figure 4.25. Phase output values generated by three-level NPC-MLI are -400V, -200, 0, 200 and 400V.

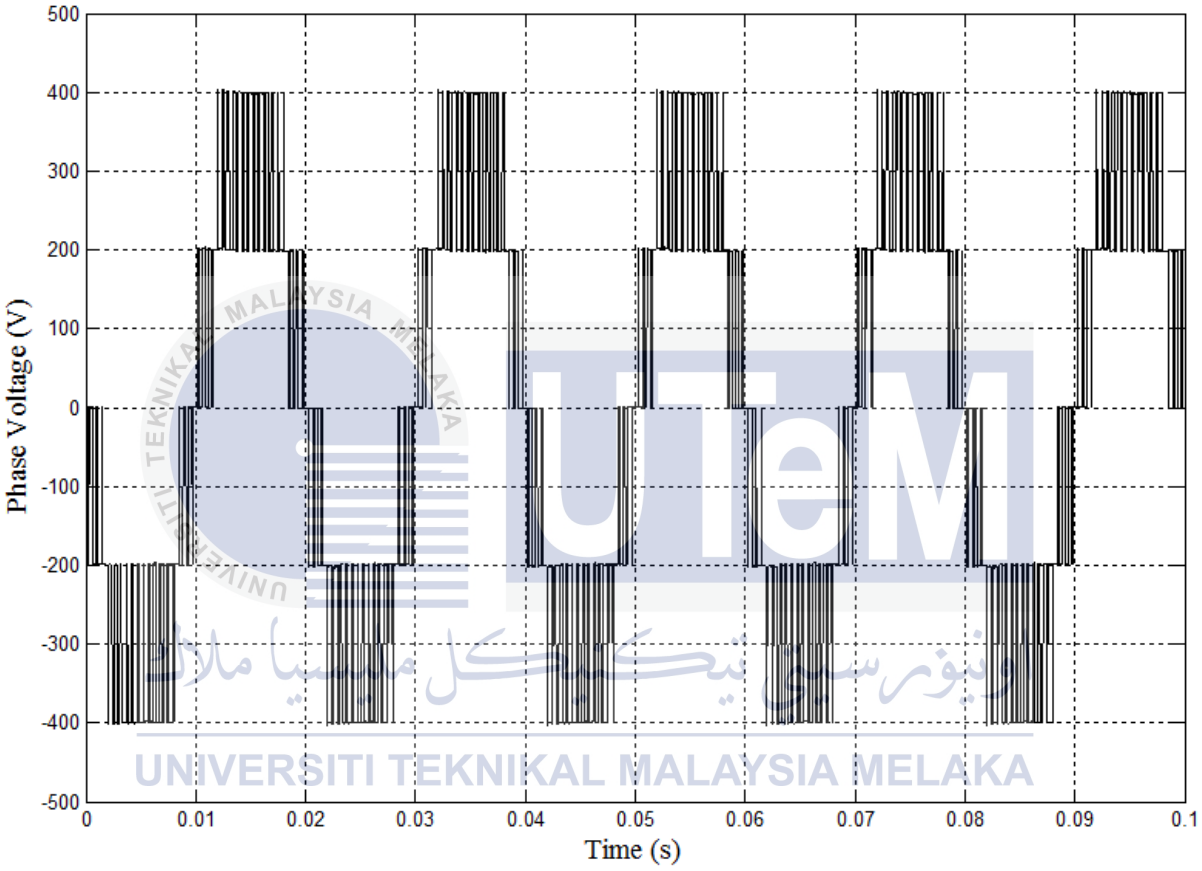
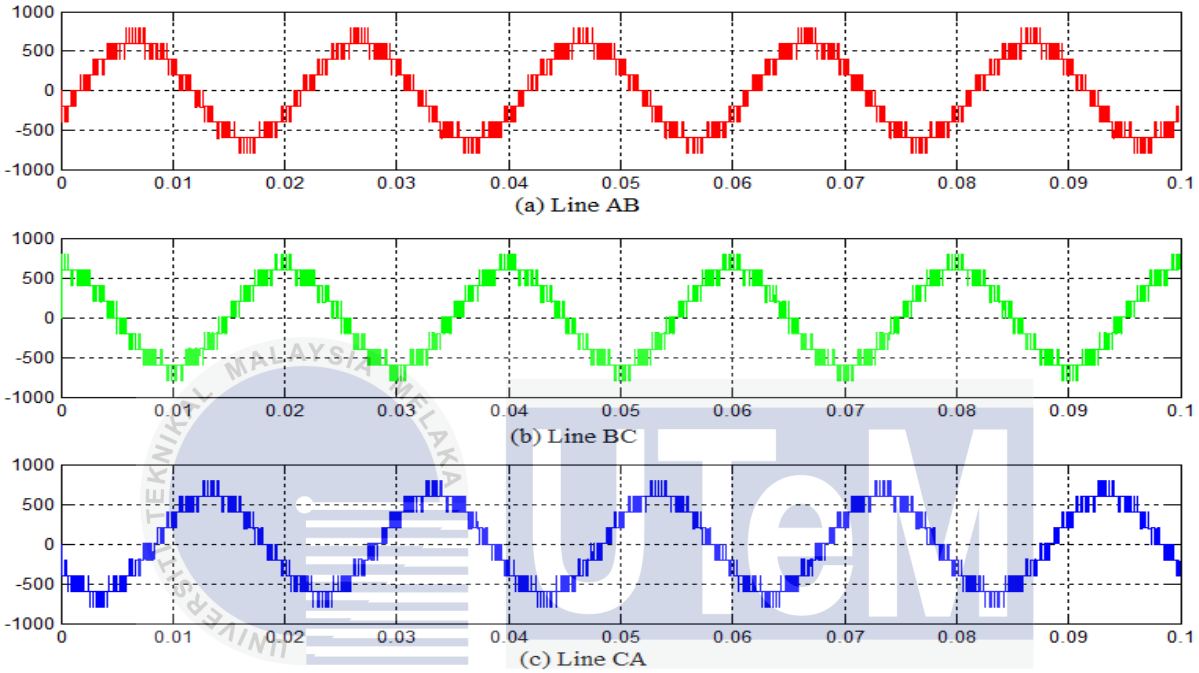
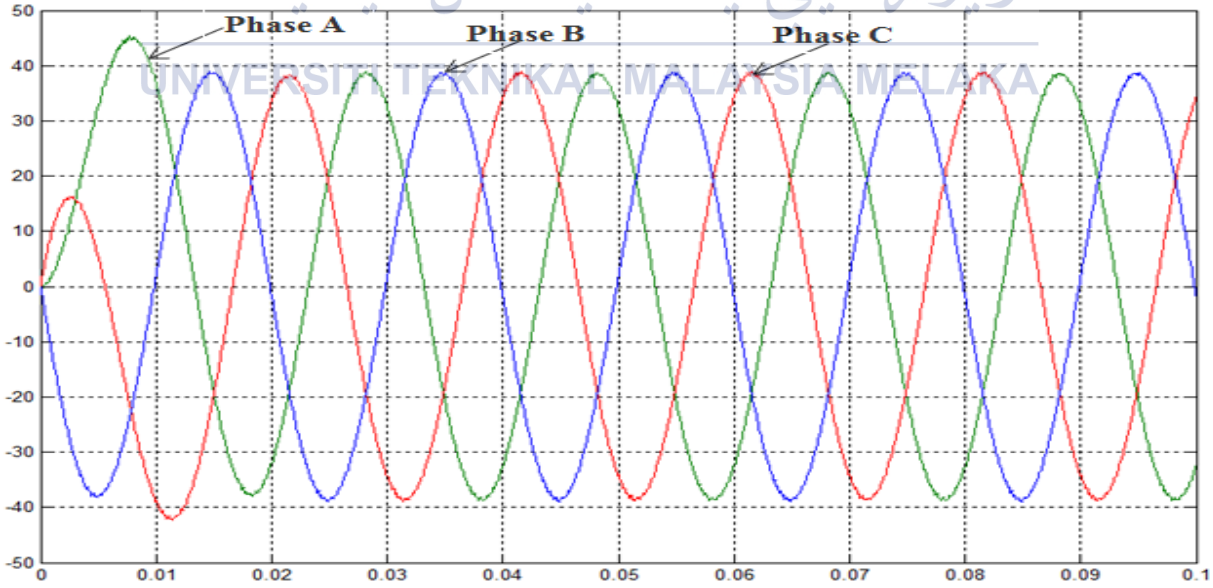


Figure 4.25: Phase voltage of five-level NPC-MLI

Simulated output line voltage and current waveform of five-level MSPWM with control method PD switching modulation on five-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been presented in Figure 4.26. The THD voltage of the simulation is 17.55%; while the THD current of the simulation is 0.39%. FFT of the simulation is illustrated in Appendix F.



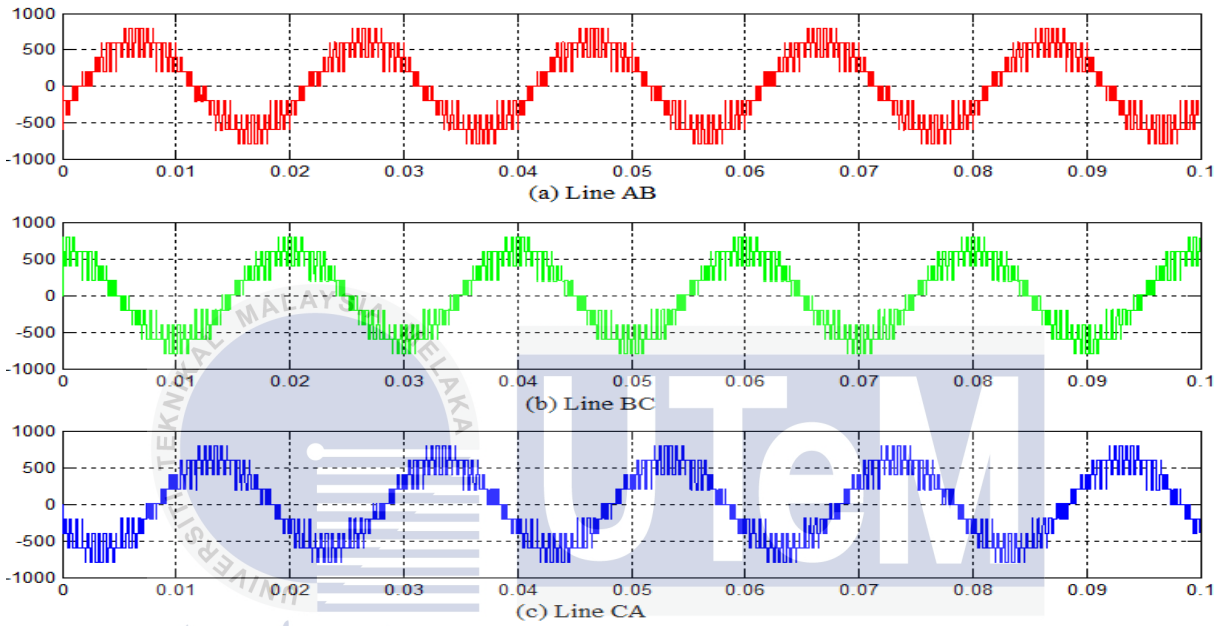
(a) Simulated line voltage waveform of five-level PD switching modulation



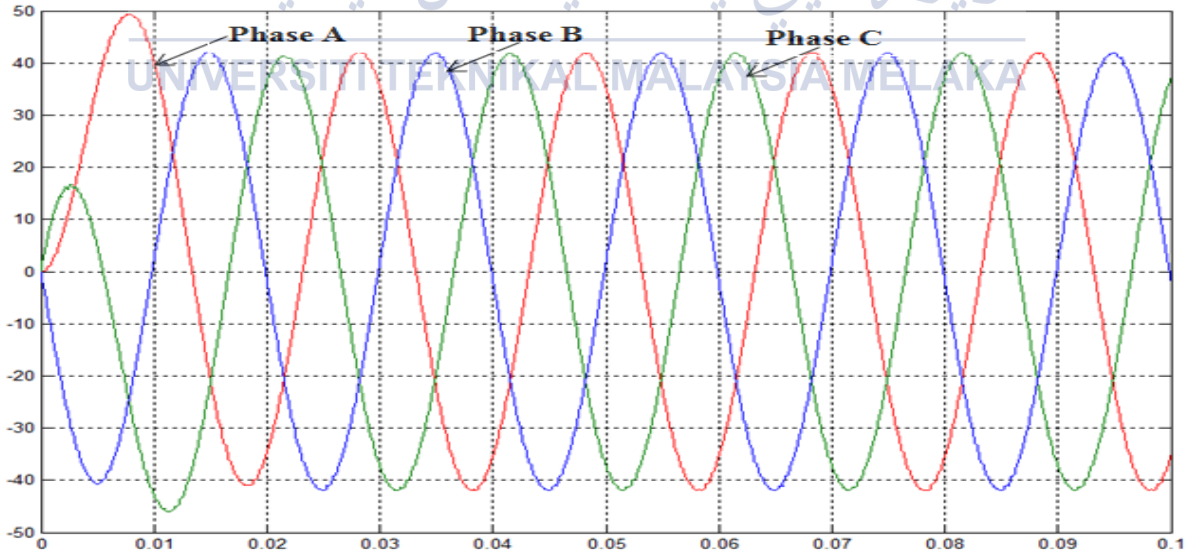
(b) Simulated output current waveform of five-level PD switching modulation

Figure 4.26: Simulation output waveforms of PD switching modulation

Simulated output line voltage and current waveform of five-level MSPWM with control method POD switching modulation on five-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been presented in Figure 4.27. The THD voltage of the simulation is 25.54%; while the THD current of the simulation is 0.69%. FFT of the simulation is illustrated in Appendix G



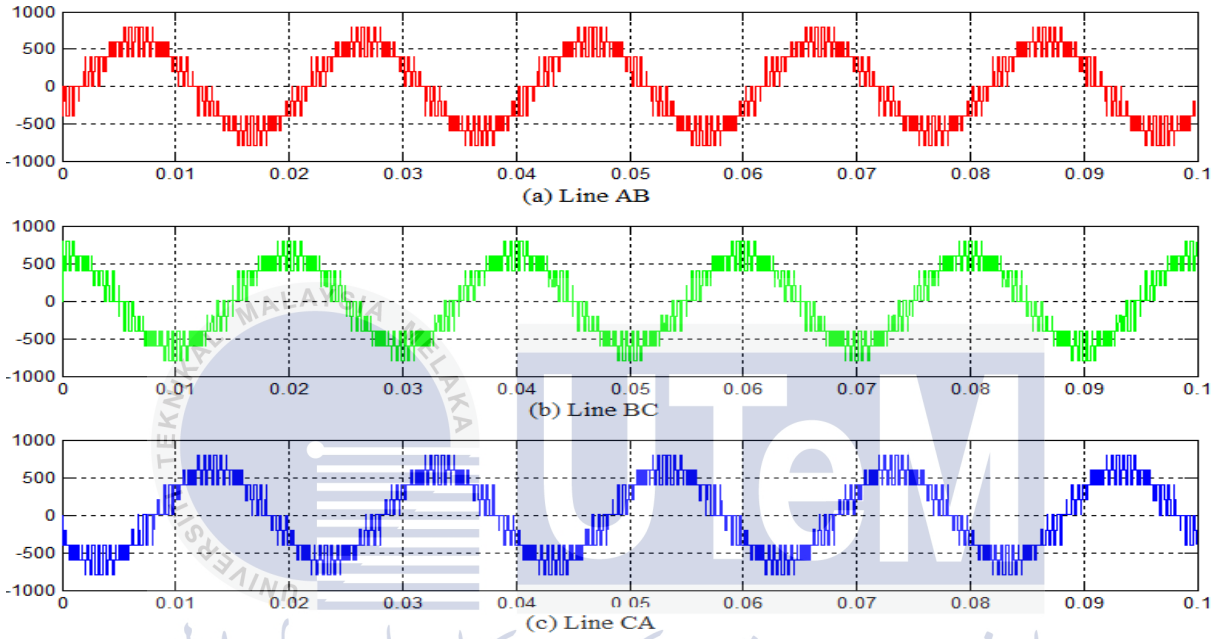
(a) Simulated line voltage waveform of five-level POD switching modulation



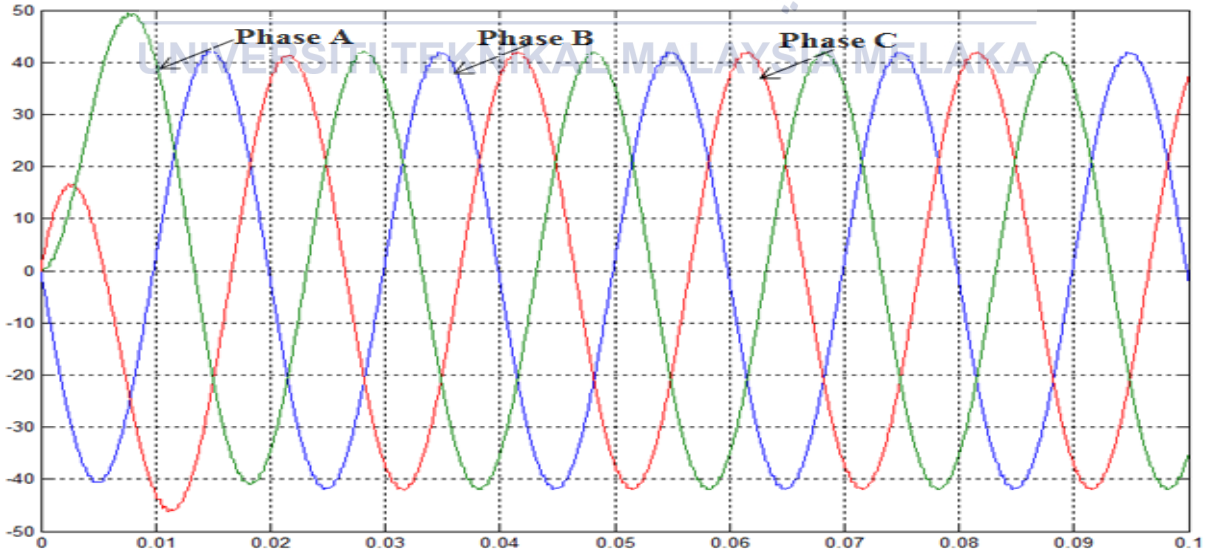
(b) Simulated output current waveform of five-level POD switching modulation

Figure 4.27: Simulation output waveforms of five-level POD switching modulation

Simulated output line voltage and current waveform of five-level MSPWM with control method APOD switching modulation on five-level NPC-MLI with parameters of 2 kHz switching frequency and modulation index of 0.9 have been presented in Figure 4.28. The THD voltage of the simulation is 24.77%; while the THD current of the simulation is 0.58%. FFT of the simulation is illustrated in Appendix H.



(a) Simulated line voltage waveform of five-level APOD switching modulation

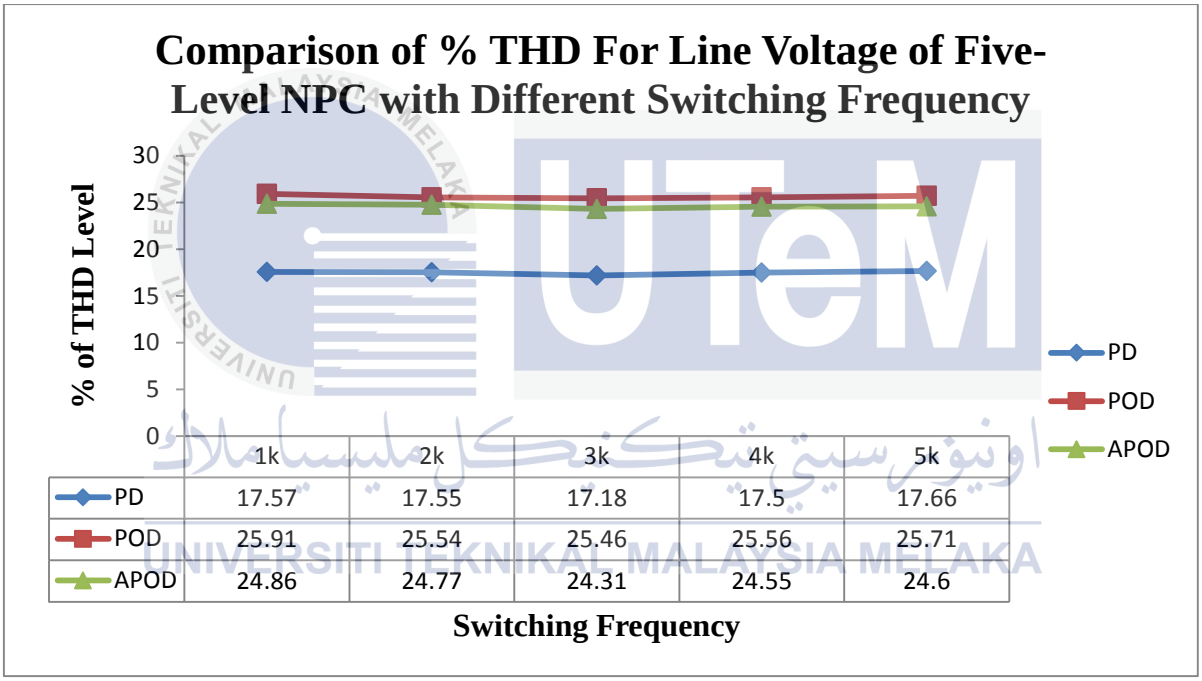


(b) Simulated output current waveform of five-level APOD switching modulation

Figure 4.28: Simulation output waveforms of APOD switching modulation

4.4.1 THD Analysis of Five-Level Neutral Point Clamped Multilevel Inverter

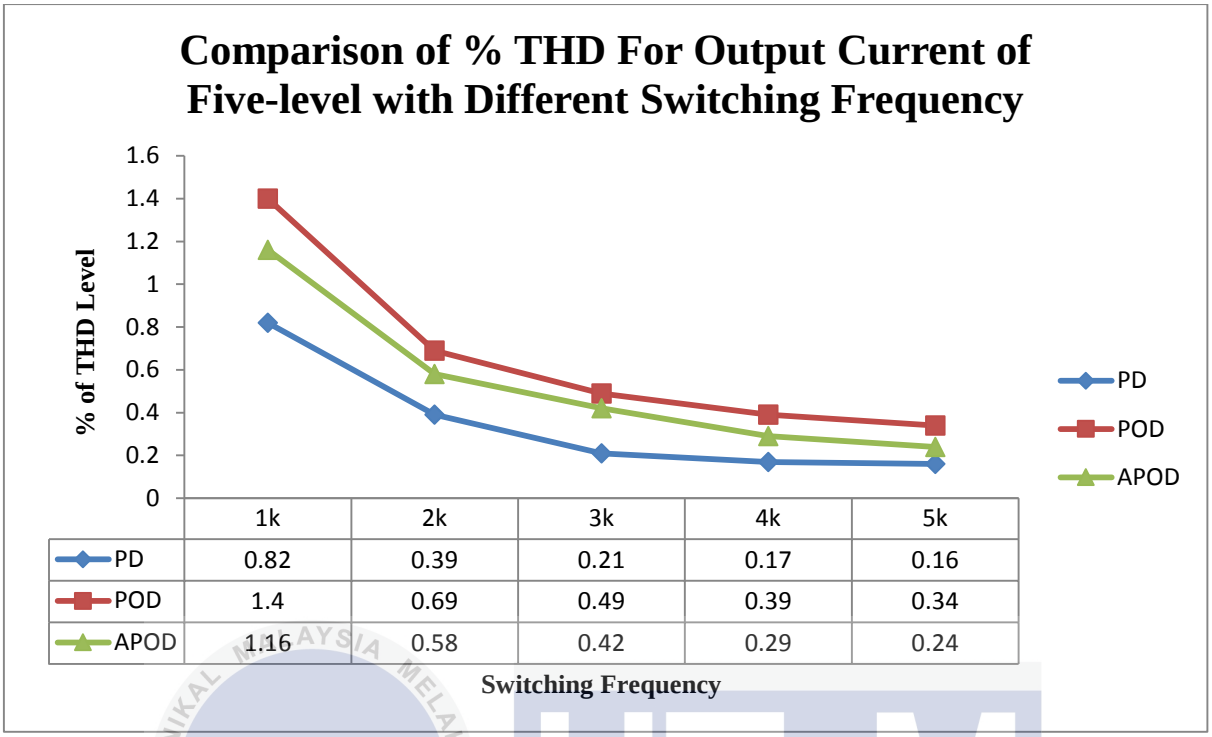
A detailed analysis of five-level MSPWM with five-level PD, POD and APOD in terms of total harmonics distortion (THD) for output line voltage and current with switching frequency increases from 1 kHz to 5 kHz have been performed. Meanwhile, modulation index is set at 0.90 for all switching frequencies and the system is connected to the balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.29 and Figure 4.30 shows the comparison of percentages of THD for line voltage and output voltage with different switching frequency.



	1k	2k	3k	4k	5k
PD	17.57	17.55	17.18	17.5	17.66
POD	25.91	25.54	25.46	25.56	25.71
APOD	24.86	24.77	24.31	24.55	24.6

Figure 4.29: Simulation with varying switching frequency from 1kHz to 5kHz for line voltage

As evident from Figure 4.29, the THD of line voltage is independent with the change of switching frequency from 1 kHz to 5 kHz. In other words, it can be said as even increases the switching frequency, but there is still no much influence on THD voltage and performs almost no changes with increasing in switching frequency. Besides that, as reveal from Figure 4.29 that PD switching modulation would produce the lower THD output voltage quality; while, the POD switching modulation produce higher THD output voltage quality. The average THD voltage of PD, POD and APOD are 17.49%, 25.64% and 24.62%, respectively.



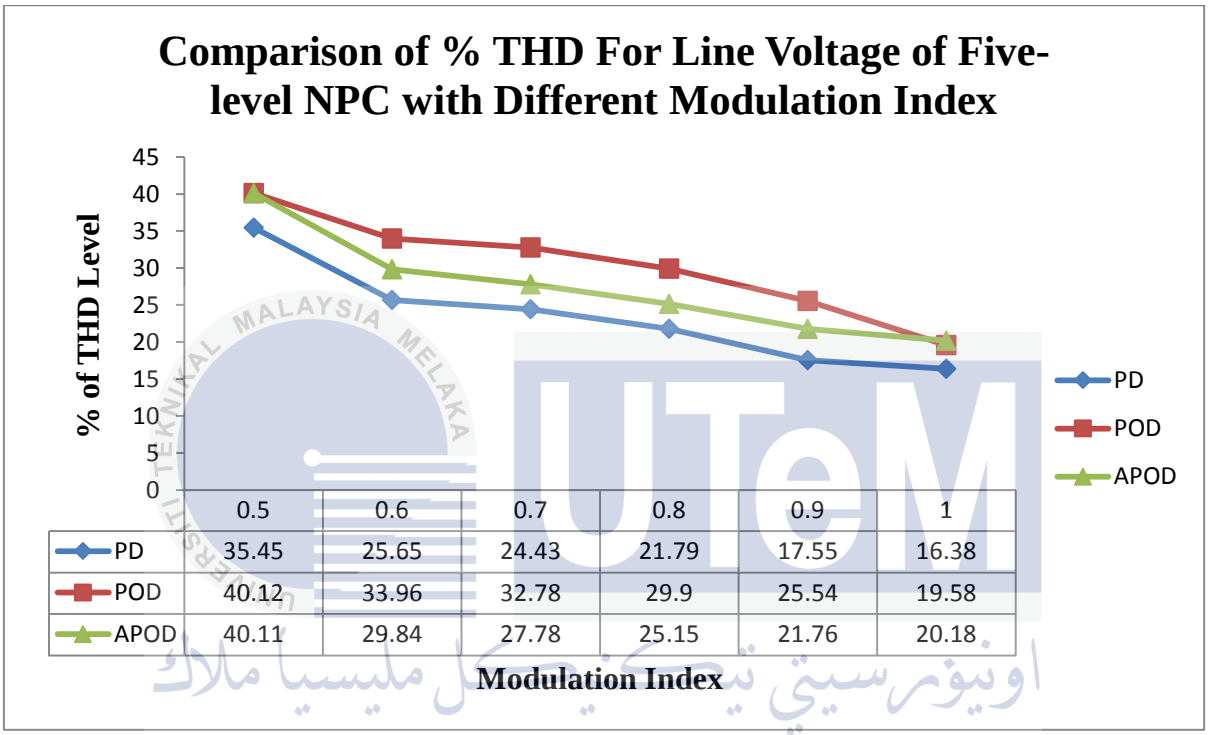
	1k	2k	3k	4k	5k
PD	0.82	0.39	0.21	0.17	0.16
POD	1.4	0.69	0.49	0.39	0.34
APOD	1.16	0.58	0.42	0.29	0.24

Figure 4.30: Simulation with varying switching frequency from 1kHz to 5kHz for output current

From Figure 4.30, one of the obvious significances can be easily observed, which the THD of the output current for all MSPWM switching modulation types were reduced sharply by increasing the switching frequency. In other words, it can describe as higher switching frequency would produce the lower THD current quality; and lower switching frequency would generate higher THD current quality. For APOD switching modulation, the THD current is 1.16% during switching frequency of 1 kHz; but by raised the switching frequency to 5 kHz, the THD current was drop to 0.24%. On the other hand, PD switching modulation gives the lower THD current among other three switching modulations and POD switching modulation produces higher THD current. During switching frequency of 2 kHz and modulation index of 0.9, the THD current of PD is 0.39% but the THD current of POD is achieved 0.69%.

An analytical study of five-level PD, POD and APOD switching modulation in terms of total harmonic distortion (THD) for output line voltage and output current with varied

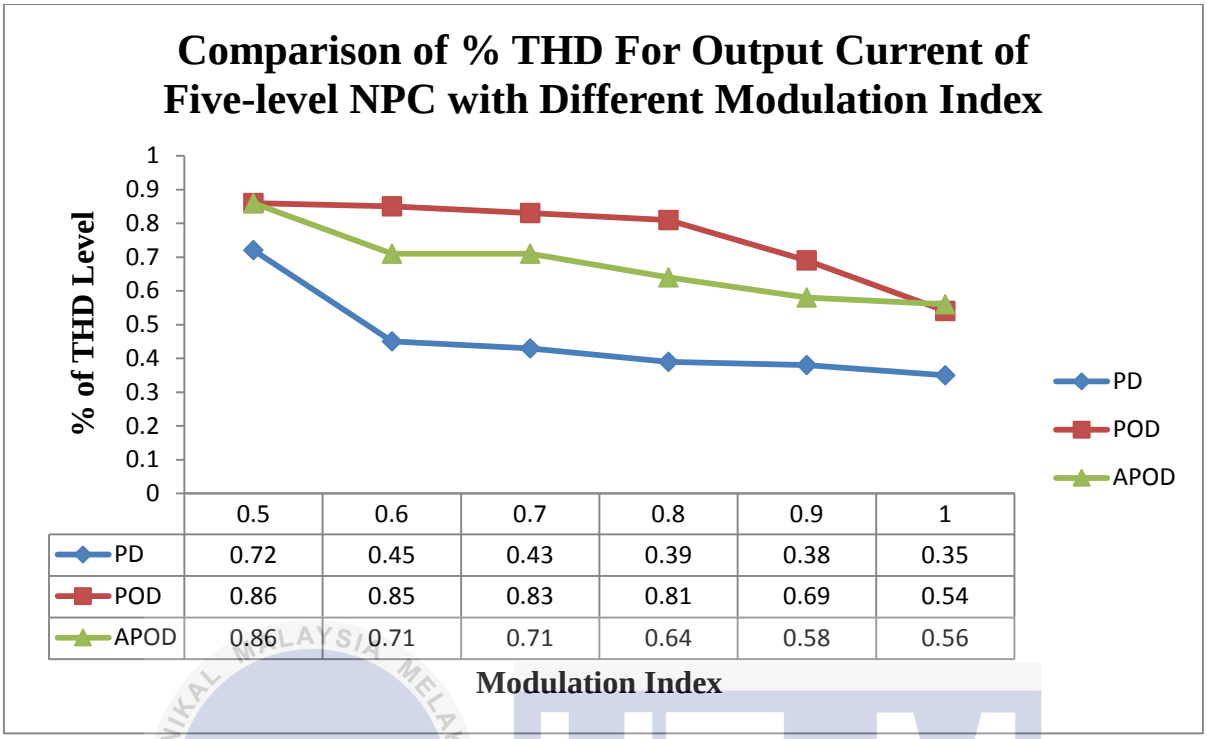
modulation index ranging from 0.5 to 1 and fixed switching frequency 2 kHz were presented in this section. Meanwhile, the system is connected to a balanced three-phase Y-connected RL load with resistive of 5Ω and inductive of 25 mH per phase. Figure 4.31 and Figure 4.32 show the comparison of percentages of THD for line voltage and output current with different modulation index.



	0.5	0.6	0.7	0.8	0.9	1
PD	35.45	25.65	24.43	21.79	17.55	16.38
POD	40.12	33.96	32.78	29.9	25.54	19.58
APOD	40.11	29.84	27.78	25.15	21.76	20.18

Figure 4.31: Simulation with varying modulation index from 0.5 to 1 for line voltage

Results of output line voltage for five-level NPC-MLI with varying modulation index from 0.5 to 1.0 obtained from Matlab/SIMULINK are presented in Figure 4.31. As can be seen in Figure 4.31, it is observed the fact that THD of line voltage can be easily reduced by increasing modulation index. For switching modulation APOD, the THD voltage was reduced from 40.11% to 20.18% when the modulation index is increased from 0.5 to 1.0. The second perception is the POD switching modulation shows the characteristics of higher percentages of THD level and PD switching modulation show the characteristics of lower percentages of THD level among three control methods.



	0.5	0.6	0.7	0.8	0.9	1
PD	0.72	0.45	0.43	0.39	0.38	0.35
POD	0.86	0.85	0.83	0.81	0.69	0.54
APOD	0.86	0.71	0.71	0.64	0.58	0.56

Figure 4.32: Simulation with varying modulation index from 0.5 to 1 for output current

As can be observed from Figure 4.32, the simulation results verify the fact that all the switching modulation shows reduction in THD current when the modulation index is increased. For APOD switching modulation, the THD current is decreased from 0.86% to 0.54% when the modulation index is increased from 0.5 to 1.0. Next, PD switching modulation shows the characteristics of most promising control method since it will produce the lower percentages of THD current. In contrary to PD switching modulation, POD switching modulation indicated the higher percentages of THD level. During switching frequency of 2 kHz and modulation index of 1.0, the THD current of POD switching modulation is 0.19% higher than PD switching modulation.

4.3.2 Balancing Problem of Five-Level Neutral Point Clamped Inverter

Same with the three-level NPC-MLI, five-level NPC-MLI also facing the DC-link capacitor imbalance problem and the imbalance problem even worse than three-level NPC-MLI. Balancing of the DC-link capacitor voltage is one of the important key features that used to determine the performance of the neutral point clamped multilevel inverter. This issue has always a biggest concern for the researches.

In this study, five-level NPC-MLI multilevel inverter is supplied with 800V input sources and the input voltage sources should distributed equally among the capacitors. A five-level NPC multilevel inverter has four dc-link capacitors. Hence, each capacitor should be oscillated at value of 200V, but somehow input voltage of five-level NPC-MLI would unequally distribute among the capacitors. The unequally distribution pattern of the capacitors voltage for disposition switching modulation of PD, POD and APOD are almost the same, the distribution of imbalance capacitors voltage for PD switching modulation is illustrated in Figure 4.33. The same situation will happened on switching modulation POD and switching modulation APOD.

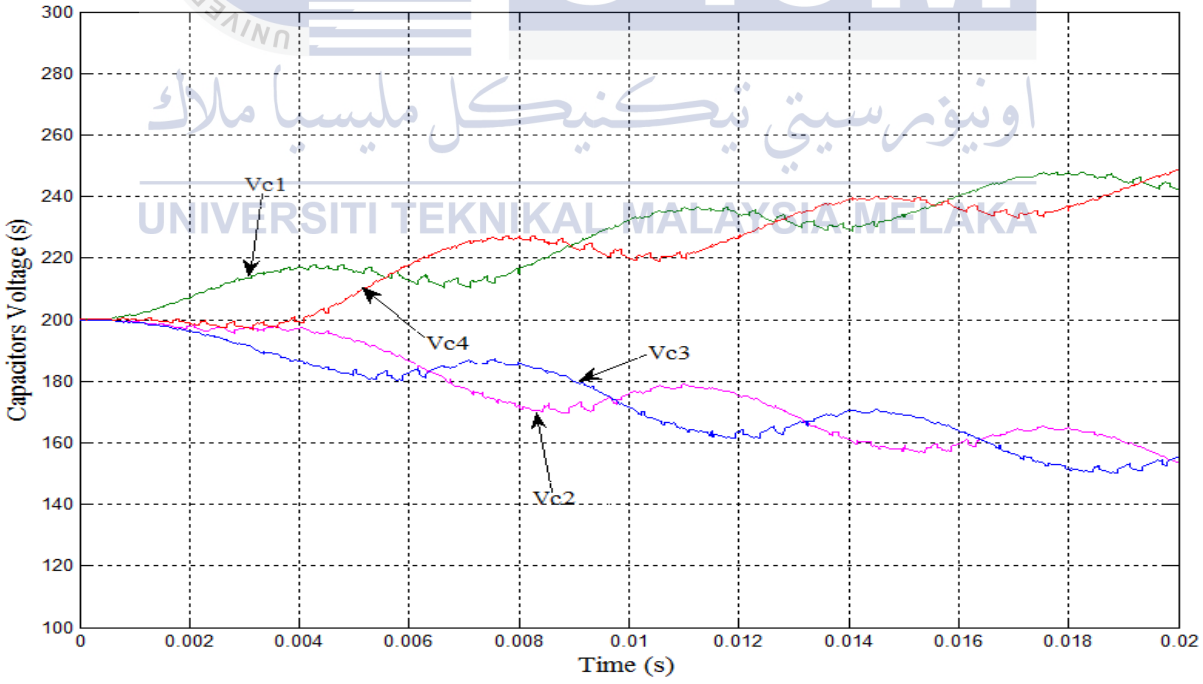


Figure 4.33: Imbalance capacitors voltage of five-level NPC-MLI

Figures 4.33 have clearly demonstrated that the voltages distribute among the capacitors of the disposition switching modulations of PD have been seriously deviated from 200V. This unbalance scenario in the DC-link capacitor voltage can result in a very serious distortion in the output voltage as shown in Figure 4.34 for PD switching modulation, Figure 4.35 for POD switching modulation and Figure 4.36 for APOD switching modulation.

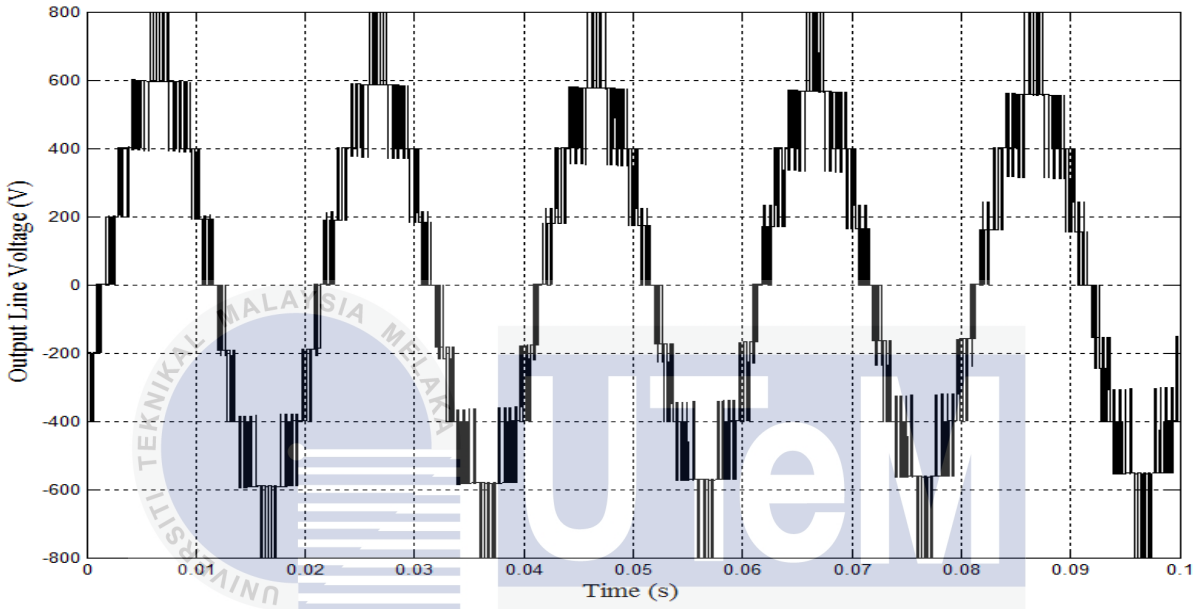


Figure 4.34: Distorted line voltage of PD switching modulation

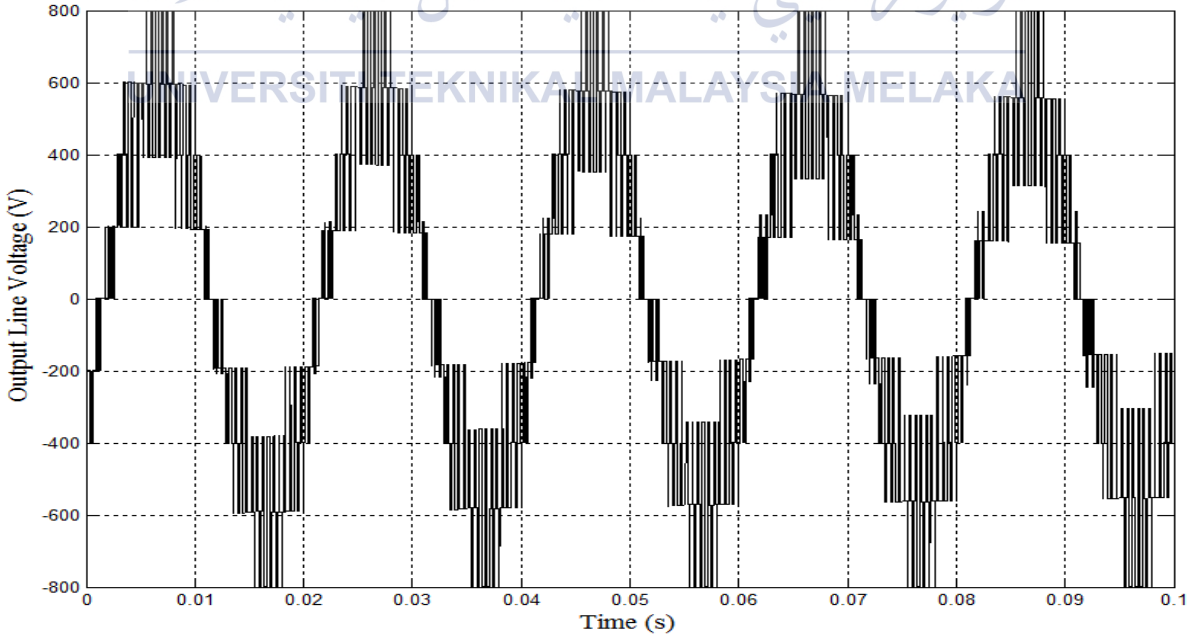


Figure 4.35: Distorted line voltage of POD switching modulation

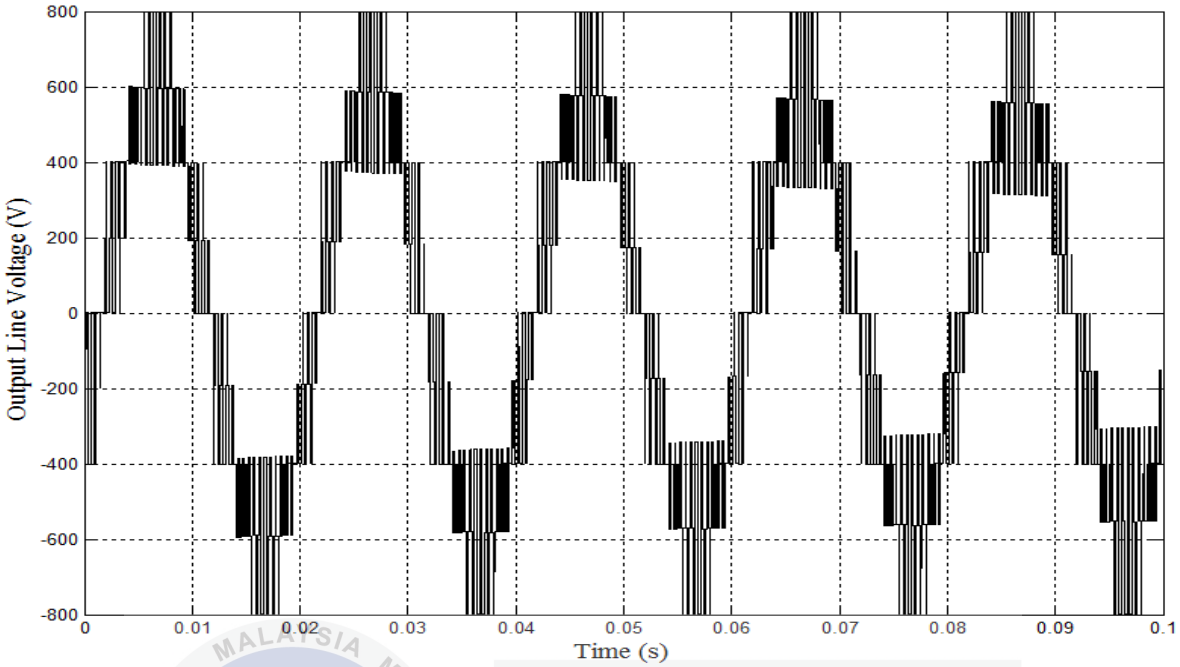


Figure 4.36: Distorted line voltage of APOD switching modulation

Recent years, these balancing capacitor voltage problems have been widely reviewed by many researchers. Many methods have been proposed in order to address this voltage balancing problem, such as inducing zero-sequence voltage, controllers, space-vector pulse width modulation (SVPWM) [35-41], and additional power circuit [83]. In this study, an additional power circuit design that consists of three additional inductors and four additional switching IGBTs that place in front of the DC-link capacitor has been proposed as shown in Figure 4.37. The working principle of this proposed additional power circuit design mainly based on the principle of buck and boost convertor.

The first step in designing additional power circuit is applying the buck convertor in front of the first capacitor, C1 and the last capacitor, C4. When V_{c1}> 200V or V_{c4} > 200V, the switching IGBT start to operate and regulated the DC-link capacitor voltage to 200V. After first capacitor, V_{c1} and the last capacitor, V_{c4} have been regulated to 200V, the imbalanced condition still existed within the medium capacitors, C_2 and C_3. The second step in balancing the capacitor voltage is apply buck and boost converter to medium capacitors. When V_{c2}>V_{c3}, the second switching IGBT start to operate and regulate the voltage of second capacitor, V_{c2}. When V_{c3}>V_{c2}, the third switching IGBT start to operate and regulate the voltage of third capacitor, V_{c3}.

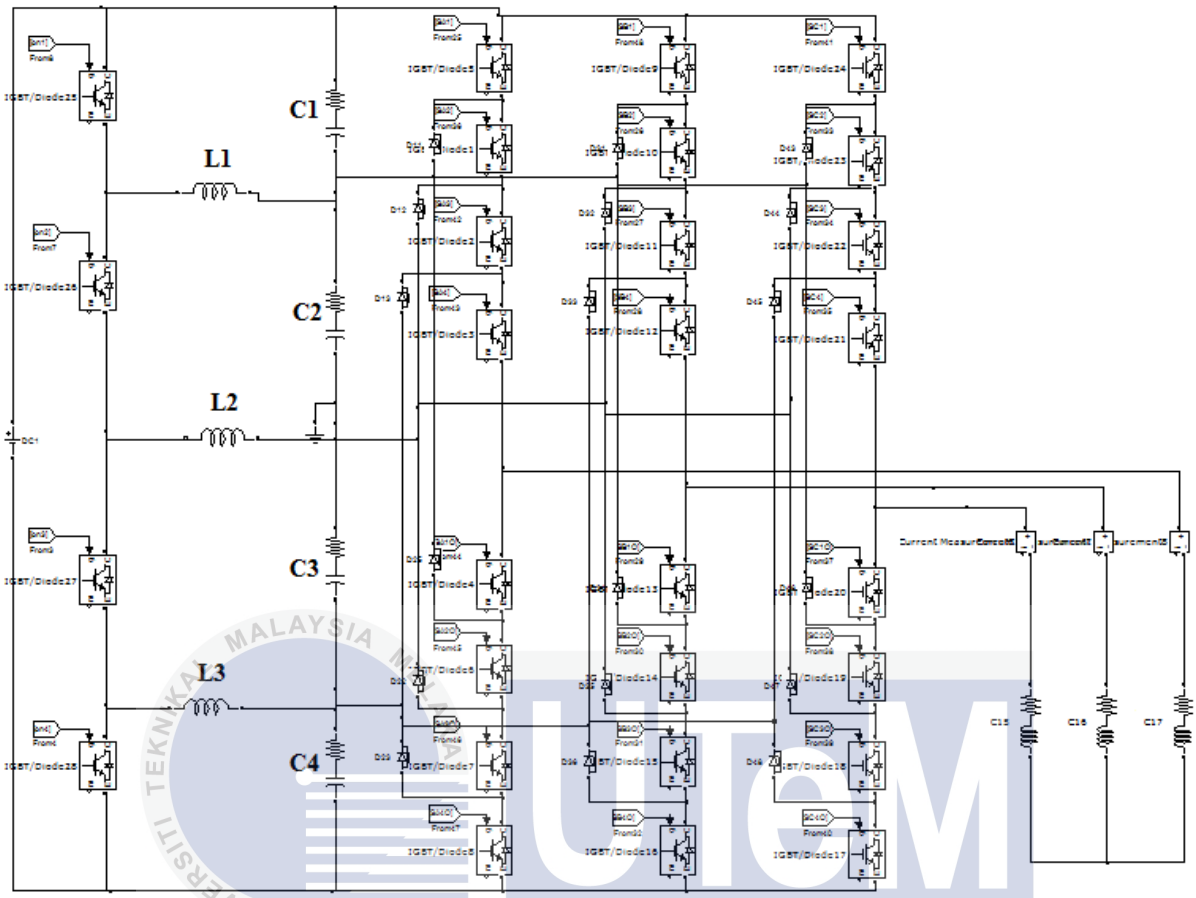


Figure 4.37: Additional power circuit of five-level NPC-MLI

After adopted the additional power circuit in five-level NPC-MLI, all the capacitors voltage, V_{c1}, V_{c2}, V_{c3}, and V_{c4} of disposition switching modulation have been regulated to a constant value of 200V as illustrated in Figure 4.38 for PD switching modulation, Figure 4.39 for POD switching modulation, Figure 4.40 for APOD switching modulation.

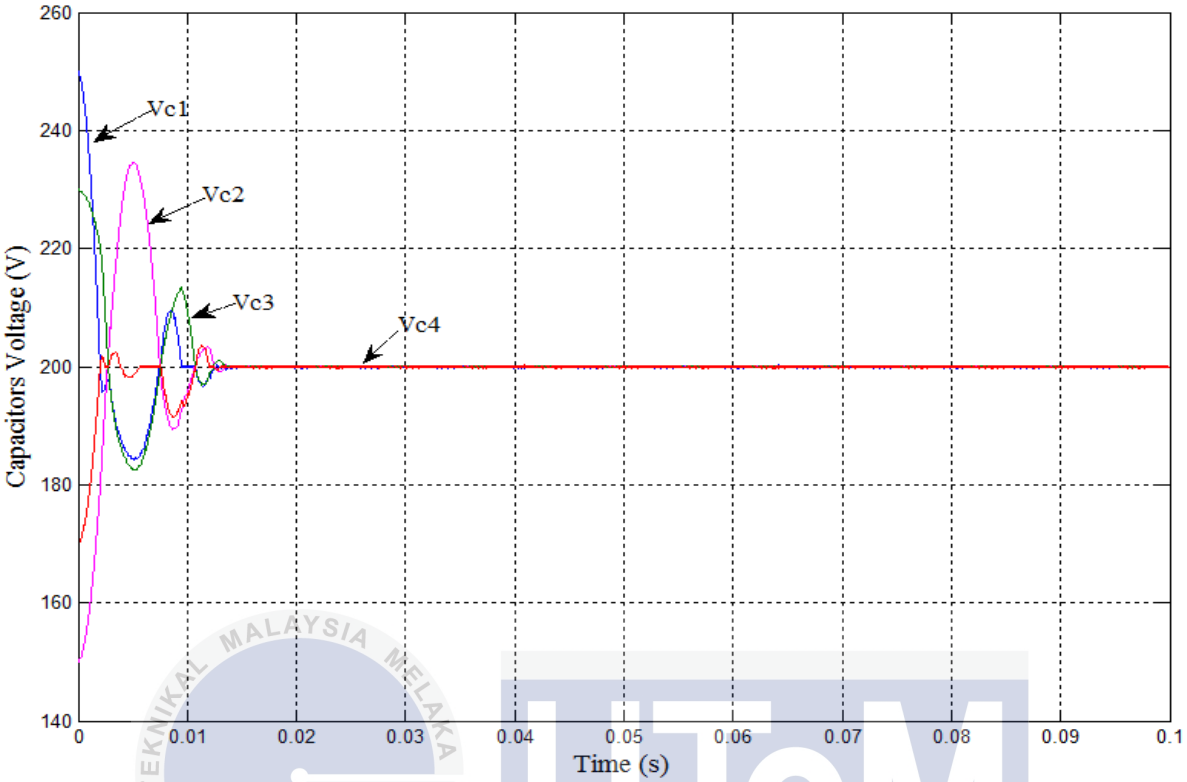


Figure 4.38: Balancing of PD after adding the additional circuit

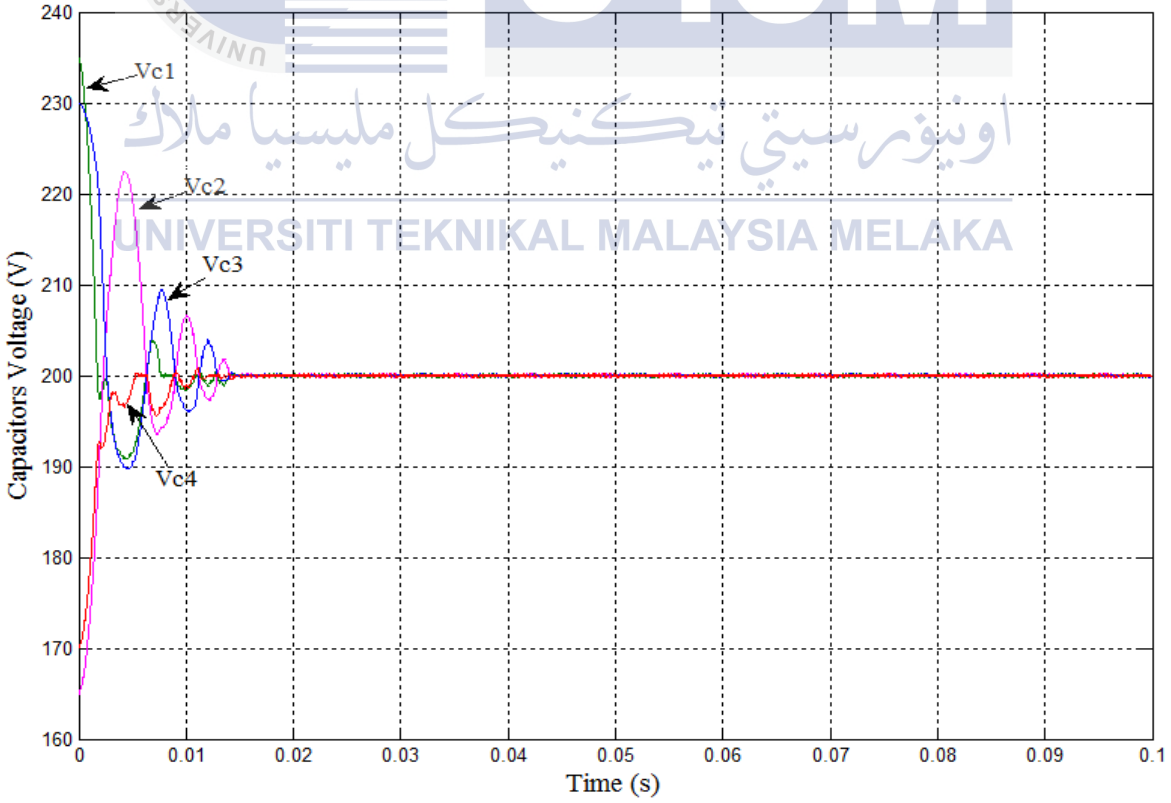


Figure 4.39: Balancing of POD after adding the additional circuit

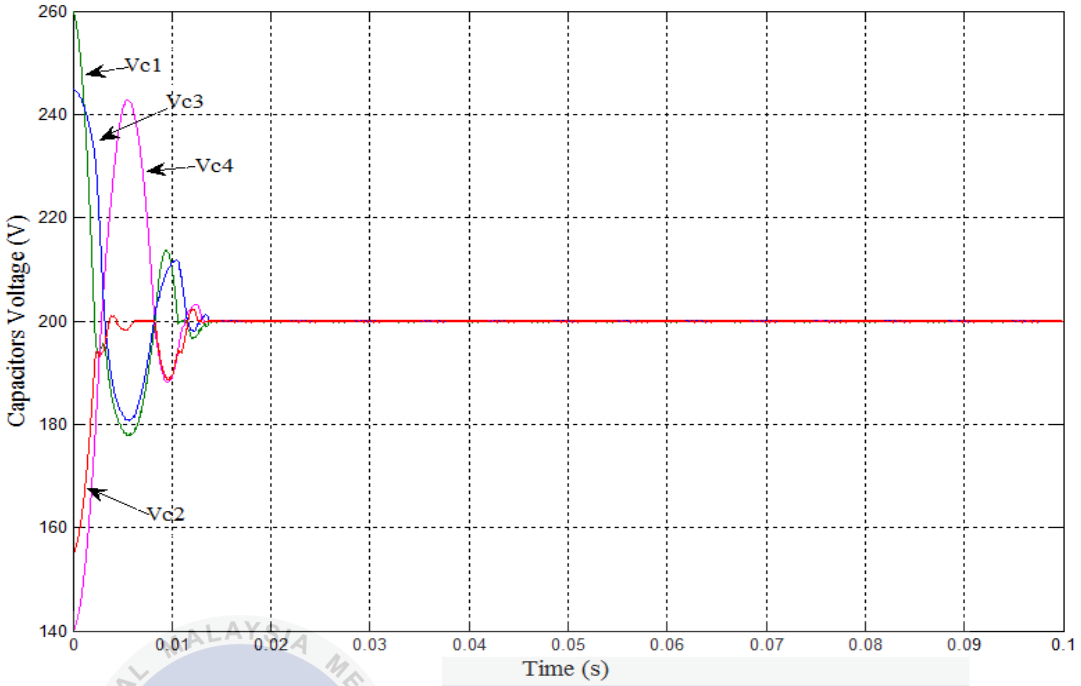


Figure 4.40: Balancing of APOD after adding the additional circuit

After the proposed regulated power circuit is being added in front of five-level NPC multilevel inverter, the convergent trend of voltage output waveform has been eliminated. The repaired output line voltage waveform of PD switching modulation is illustrated in Figure 4.41.

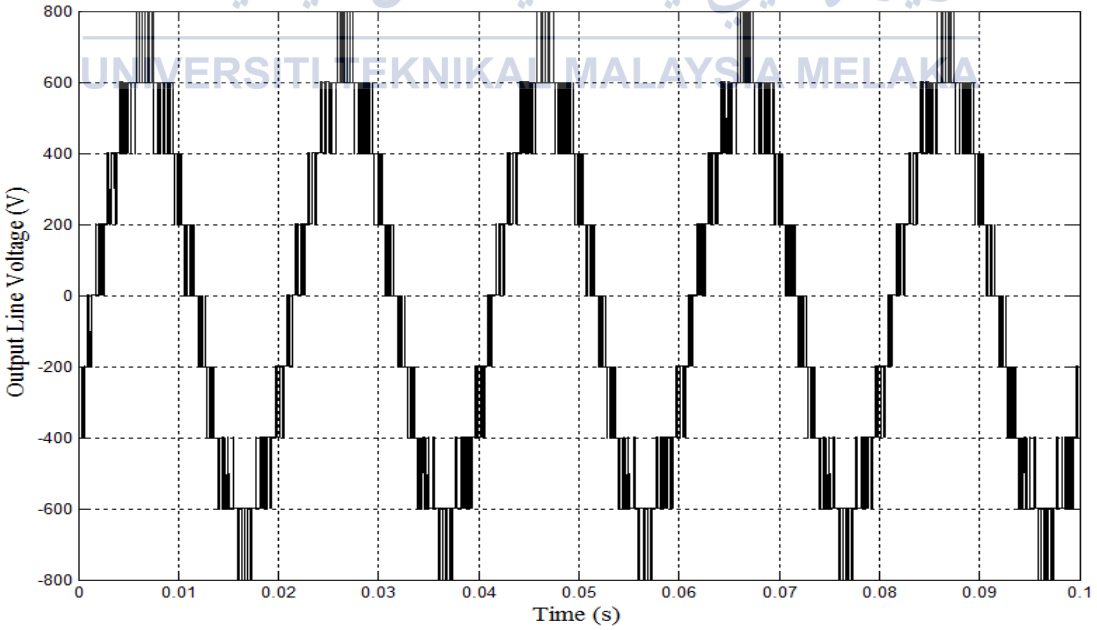


Figure 4.41: Balancing line voltage of PD after adding the additional circuit

The same condition also happened in POD switching modulation and APOD switching modulation. The repaired output voltage waveform of POD and APOD switching modulation are illustrated in Figure 4.42 and Figure 4.43, respectively.

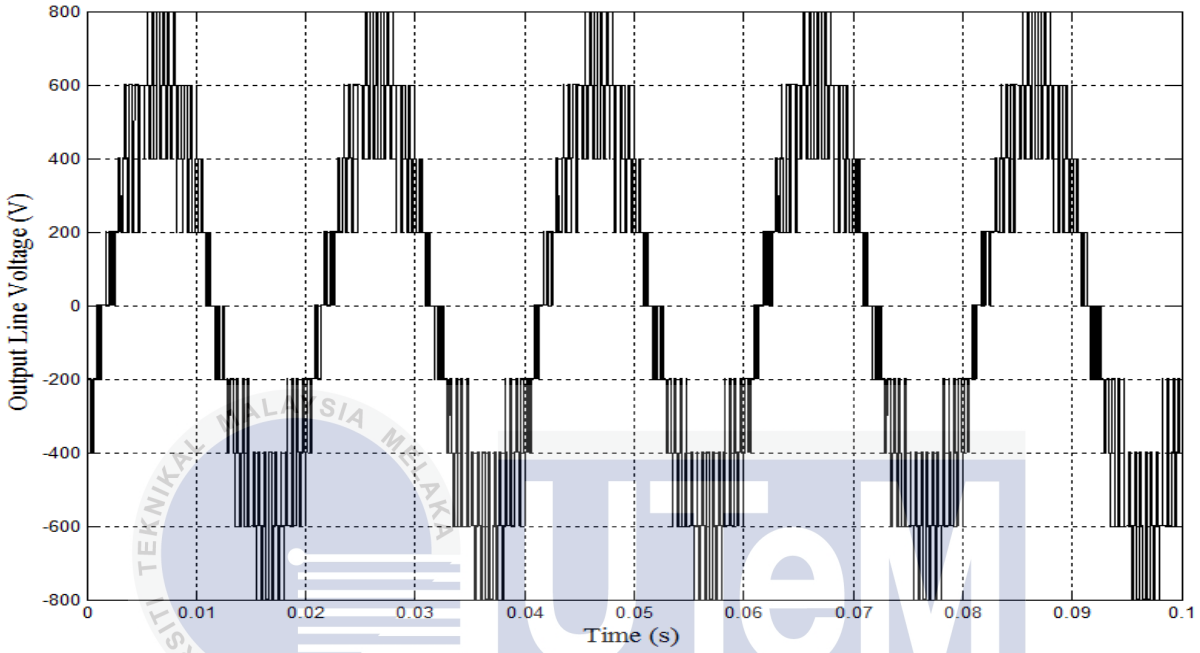


Figure 4.42: Balancing line voltage of POD after adding the additional circuit

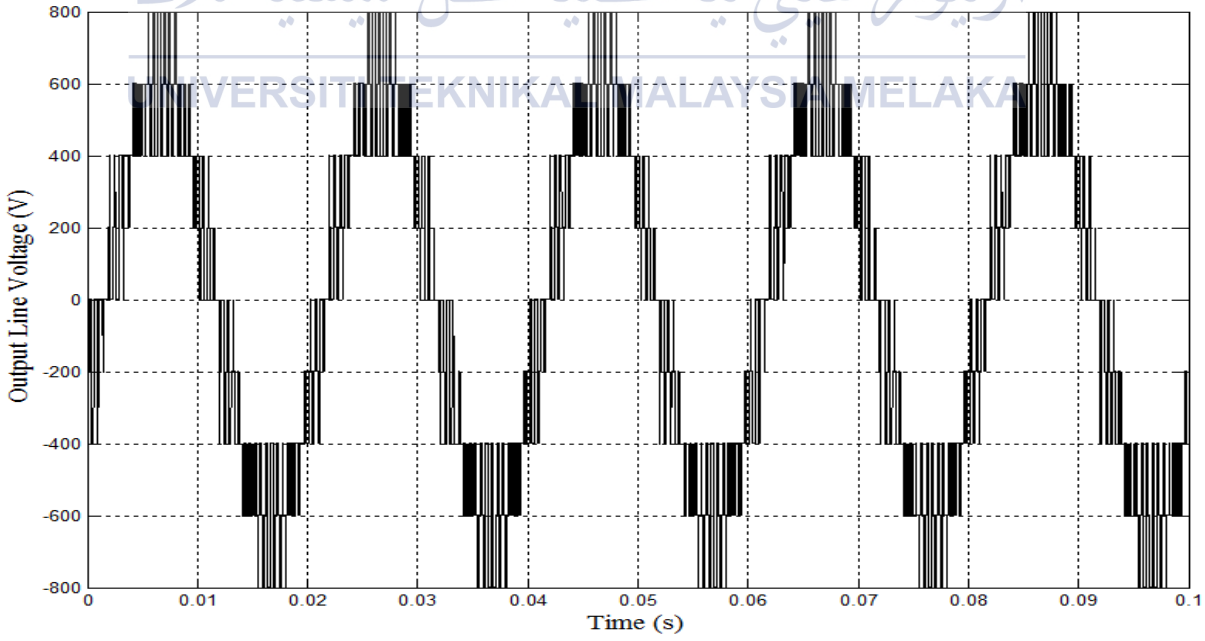


Figure 4.43: Balancing line voltage of APOD after adding the additional circuit

The advantages of adding an additional power circuit not only can balanced the capacitor voltage value to a desired value but also adding benefit of reducing the capacitor value from 2200µF to 1500µF without affect the THD of output voltage. The result of comparison has been shown in Figure 4.44. Without the additional circuit, the output voltage is badly distorted with 1500µF DC-link capacitors, but the output voltage of 1500µF DC-link capacitors with the additional circuit is same with 2200µF DC-link capacitors.

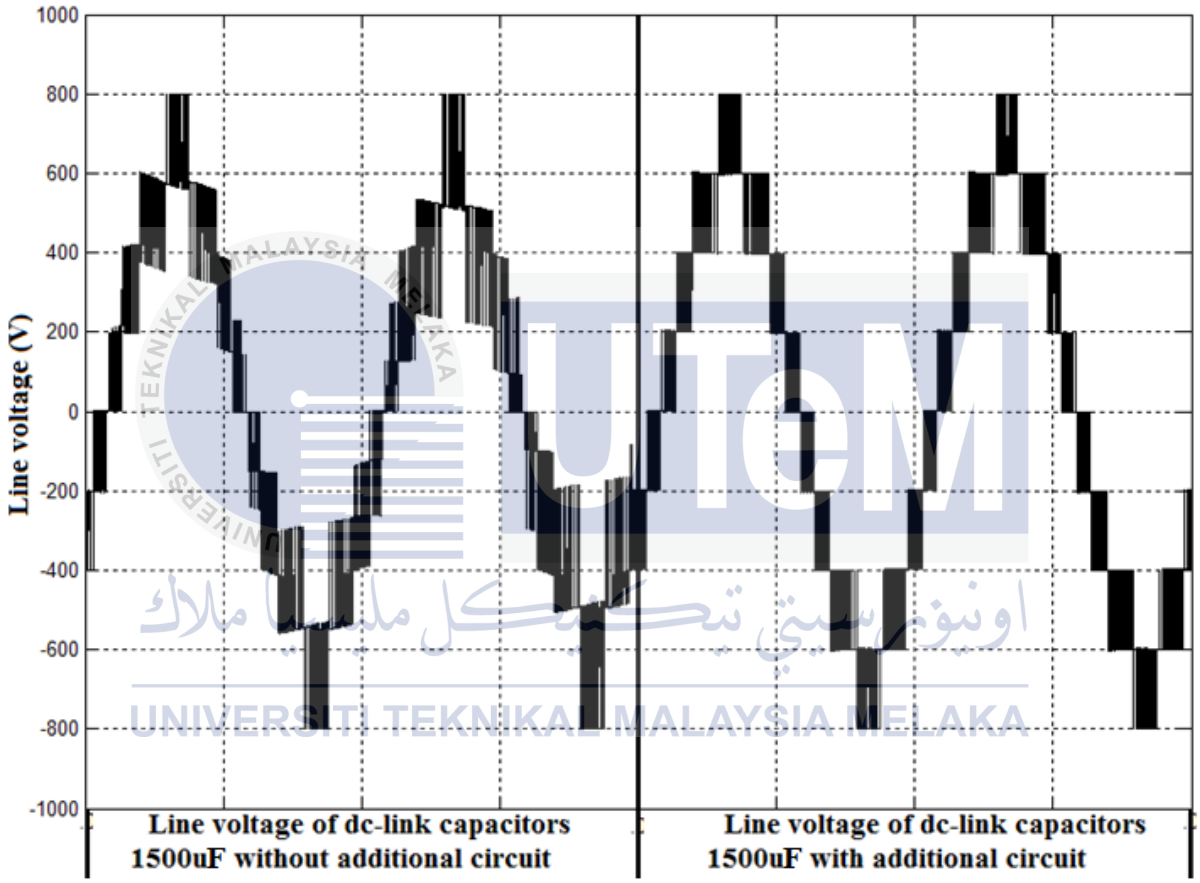
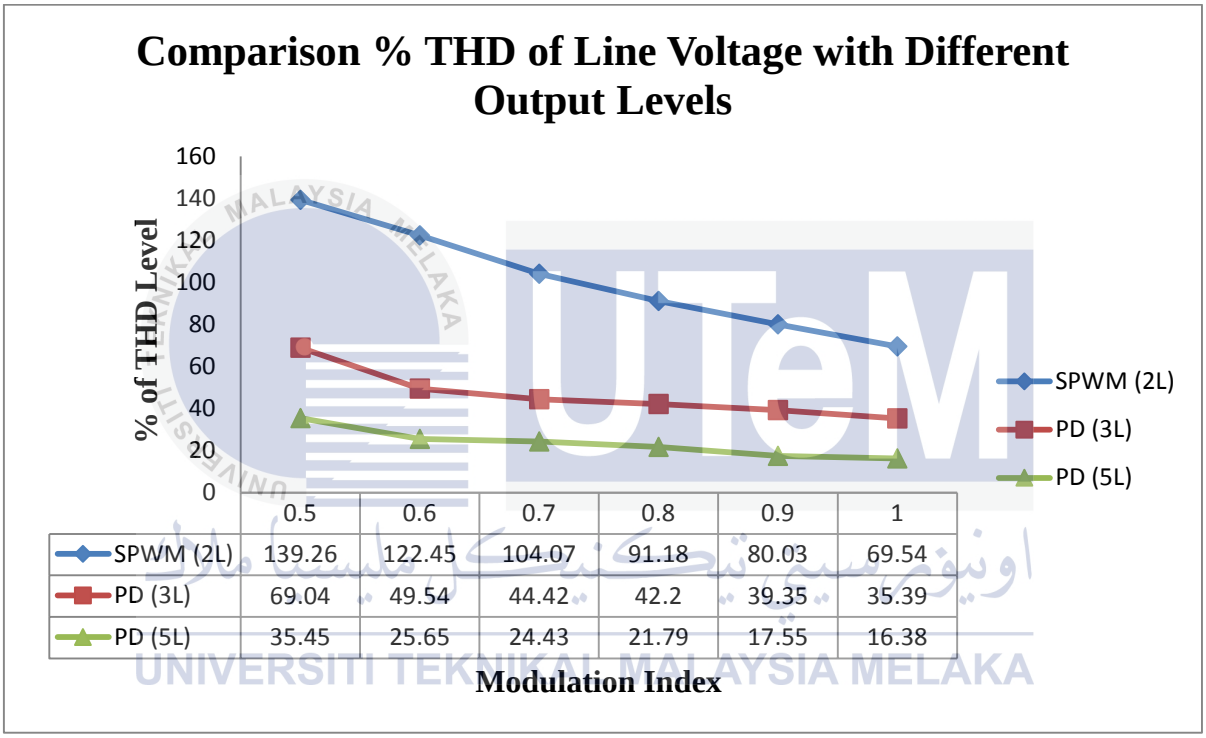


Figure 4.44: comparison of line voltage with 1500µF

4.5 Comparison Performances of the Topologies

The higher levels of multilevel topologies contributed a very important feature which is lower the THD content. This statement can be verified by comparing the THD voltage of different output level topologies as presented in Figure 4.45. The simulation in Figure 4.41 is based on three-phase balance load; resistive 5Ω and inductive 25 mH, with fixed modulation index 0.9 and switching frequency of 2 kHz.



	0.5	0.6	0.7	0.8	0.9	1
SPWM (2L)	139.26	122.45	104.07	91.18	80.03	69.54
PD (3L)	69.04	49.54	44.42	42.2	39.35	35.39
PD (5L)	35.45	25.65	24.43	21.79	17.55	16.38

Figure 4.45: Comparison % THD of different output level topologies

Figure 4.45 has clearly reveal the fact that five-level NPC-MLI will generated the most lower THD voltage compared with the two-level conventional inverter and three-level NPC-MLI. Besides that, two-level conventional inverter indicated the higher THD voltage among three different output level topologies. During modulation index of 0.9, two-level conventional inverter indicated THD voltage of 80.03%, three-level NPC-MLI shows the THD voltage of 39.35%; while, THD voltage of five-level NPC-MLI just only 17.55%.

Next, another advantage of higher levels topologies is output waveform that generates will be presented in more sinusoidal waveform. The comparison of output line waveform with different output levels is shown in Figure 4.46. As clearly demonstrated in Figure 4.14, the output line voltage levels are increased when the higher levels topologies is adapted.

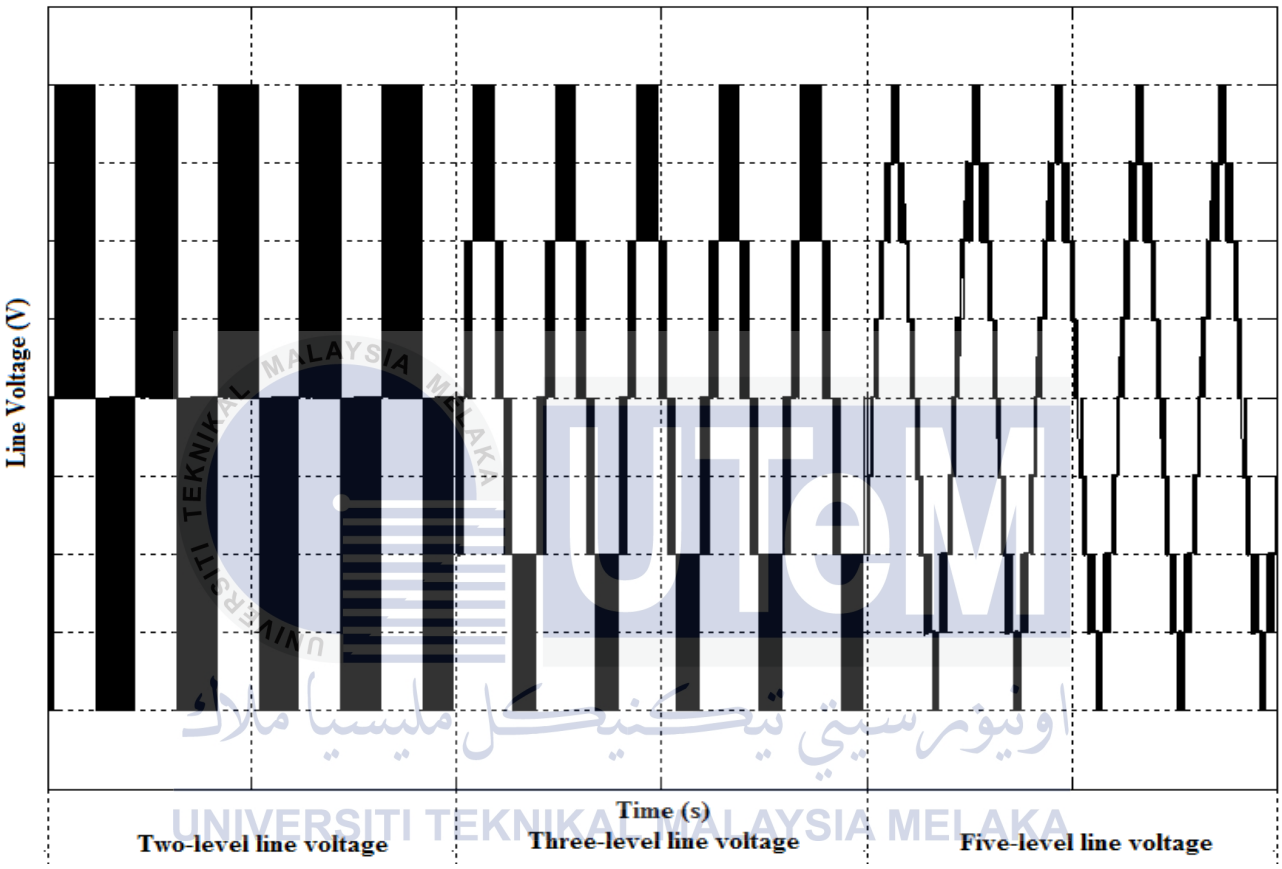


Figure 4.46: Output line output waveform with different output levels

It is undeniable that higher output levels or lower output levels involved in a particular topology have its own advantages and disadvantages. Table 4.4 shows the summaries and comparison of different output level topologies, in terms of number of switches adopted, output levels, percentages of THD, DC-link balancing, switching modulation.

Table 4.4: Summaries and comparison of the characteristics

	Two-level conventional inverter	Three-level NPC-MLI	Five-level NPC-MLI
Number of switches	6	12	24
Number of output levels	2	3	5
% of THD	Higher	Intermediate	Lower
DC-link balancing	No balancing problem	Balancing problem	Most serious balancing problem
Switching modulation	Easier	Complicated	Very complicated

As can be tell from the Table 4.4, higher output levels or lower output levels involved have its own pros and cons. For the case of two-level conventional inverter, it only adopted six switches and does not facing any DC-link balancing problem, but the output THD content is the most higher among three different output levels topologies. In the other hands, for the case of five-level NPC-MLI, number of switches that required is the most many and the DC-link balancing problem is the most serious among three different types topologies; but the output THD content that generated is the most promising.

4.6 Summary

As a conclusion from this chapter, line voltage shows the linear characteristics even increases in switching frequency; but the THD content of output current will decreases with increasing in switching frequency. On the other hand, THD content of both output line voltage and current would reduce with increasing modulation index.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

As a conclusion from this study, every topology has its own advantages and disadvantages. Different topologies with different switching modulation would come out different performances. Important parameters that used to evaluate performance of the inverter are output THD content, DC-link balancing and switching losses. For two-level conventional inverter, SVPWM is the most effective switching compared to the SPWM, because it will produce lower THD content output. Besides that, two-level inverter does not involve in any DC-link balancing problem.

For three-level NPC-MLI, among all the switching methods, three-level SVPWM and three-level PD switching modulation can be concluded as most suitable to control the switches of three-level NPC-MLI. Three-level PD switching modulation produces lower THD level output than three-level SVPWM, but it will cause the topologies involved in imbalance DC-link problem. Hence, with three-level PD switching modulation, three-level NPC-MLI required additional power circuit to regulate and maintained the DC-link voltage; which indirectly adding more cost. THD output of the three-level SVPWM is a bit higher than three-level PD switching modulation, but it provides self-balancing characteristics for three-level NPC-MLI. Another switching method that shows the ability of self-balancing is POD switching modulation, but the major drawback of this switching method is produced the higher percentages THD level.

Next, for five-level NPC-MLI, five-level PD switching modulation was found to produce the lower percentages THD output among disposition switching modulation. On the other hands, five-level NPC-MLI is facing the most serious imbalance DC-link problem, this problem is even much more worsen than the balancing problem faced by three-level NPC-MLI.

Hence, extra components are required to construct the balancing additional power circuit. The advantage of adopted five-level NPC-MLI is generated the lower percentages THD output compared with the two-level conventional inverter and three-level NPC-MLI, but the major disadvantages of this topologies are number of switches required is the most and the imbalance DC-link problem is the most worse.

All three topologies show the same features when dealing with increasing switching frequencies and increasing modulation index. Keep increases the switching frequency form 1kHz to 5kHz, the percentages THD of the output line voltage will show the linear pattern but the output current will indicated the reducing characteristics with increasing switching frequency. For modulation index, the percentages THD of both the output current and voltage decrease with increasing the modulation index from 0.5 to 1.0.

The switching methods used for analysis in this study are SVPWM and SPWM/MSPWM; the advantages of adopted SVPWM are self-balancing characteristics and lower percentage THD, but the major defect of SVPWM is complexity in constructed, the level complexity is increases when the output levels involved is increasing. The main advantages of using SPWM/MSPWM are the methodical construction is easier than SVPWM and the complexity is maintaining even the output level required increases, but it will cause imbalance DC-link problem and higher percentages THD output. Last but not the least, even adoption of the additional power circuit will increase the cost of construction; but from another viewpoint, the adoptee of this additional power circuit will reduce the DC-link capacitor value without influence in output voltage.

5.2.1 Recommendation

There are several suggestions to further understand the performances of the neutral point clamped for future studies. First, analysis of switching losses should be performed and other switching modulations should be implemented. Next, in order to verify the results of the simulations, the hardware of three-level and five-level neutral point clamped should be constructed.

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APPENDICES

Appendix A: FFT analysis for two-level SPWM

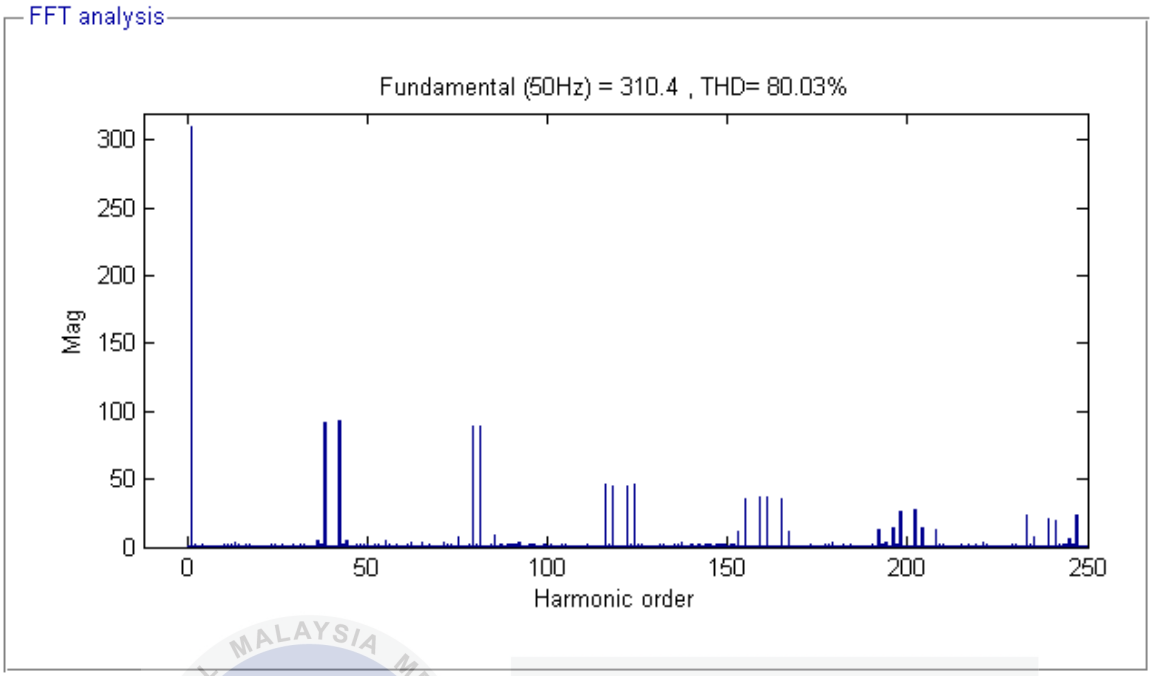


Figure A1: FFT analysis of line voltage for two-level SPWM

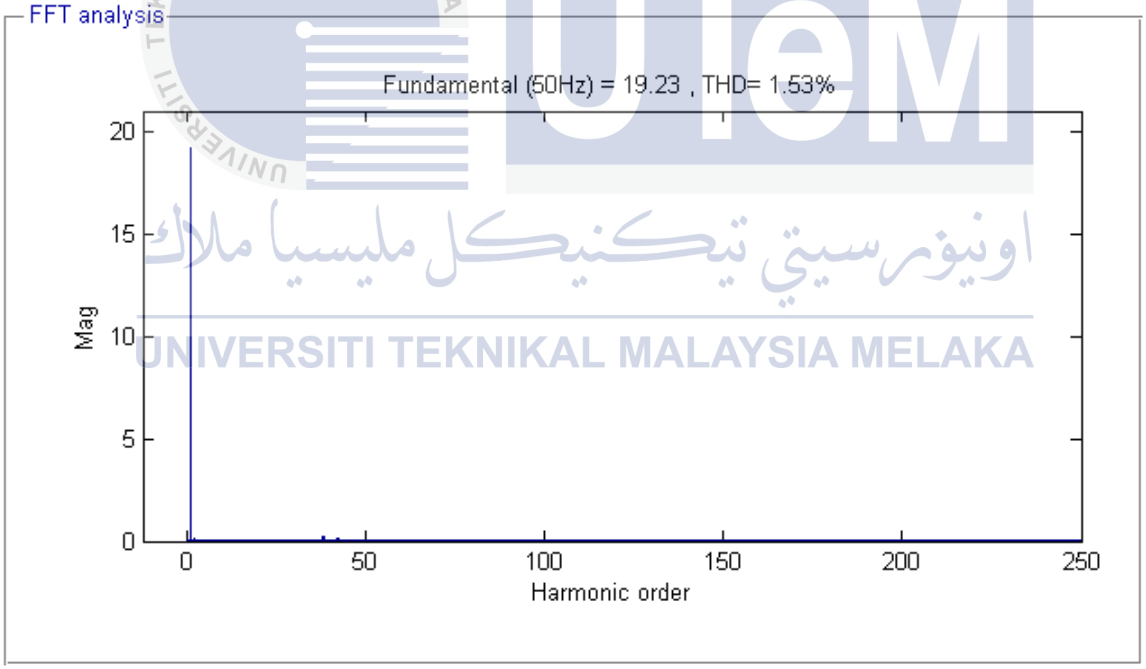


Figure A2: FFT analysis of output current for two-level SPWM

Appendix B: FFT analysis of two-level SVPWM

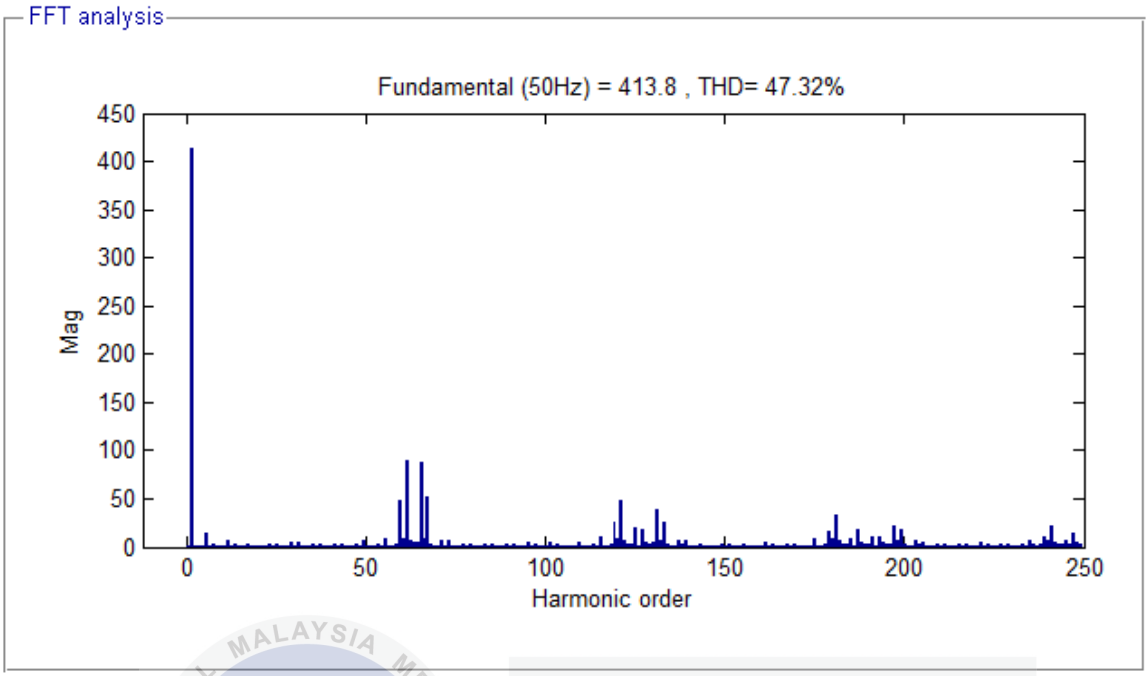


Figure B1: FFT analysis of line voltage for two-level SVPWM

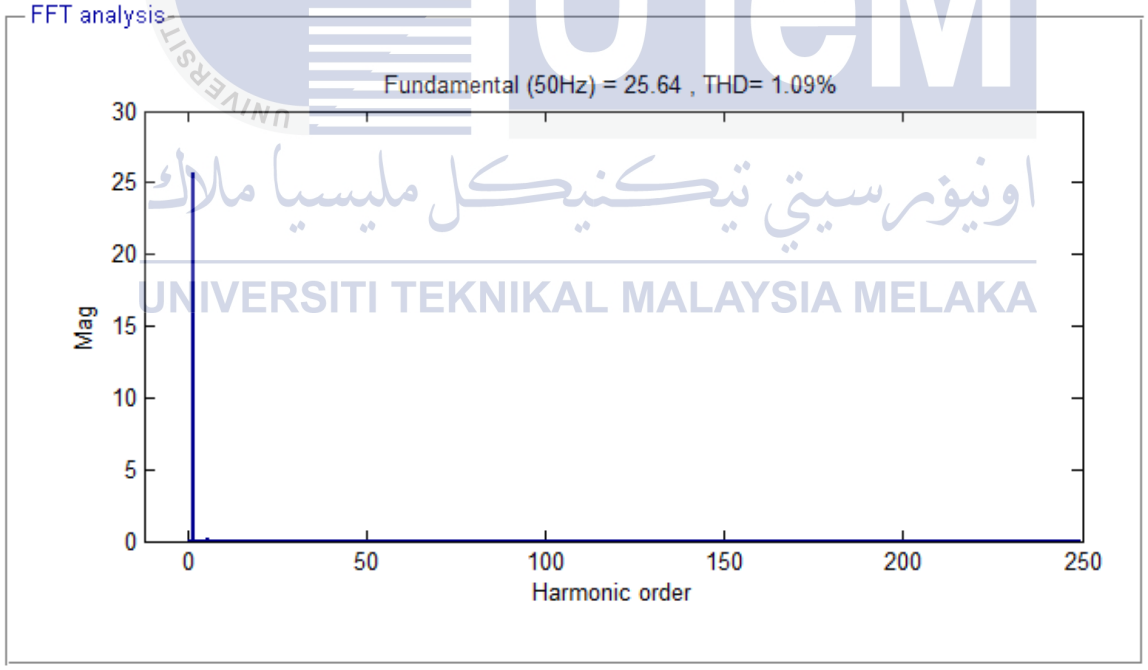


Figure B2: FFT analysis of output current for two-level SVPWM

Appendix C: FFT analysis of three-level PD switching modulation

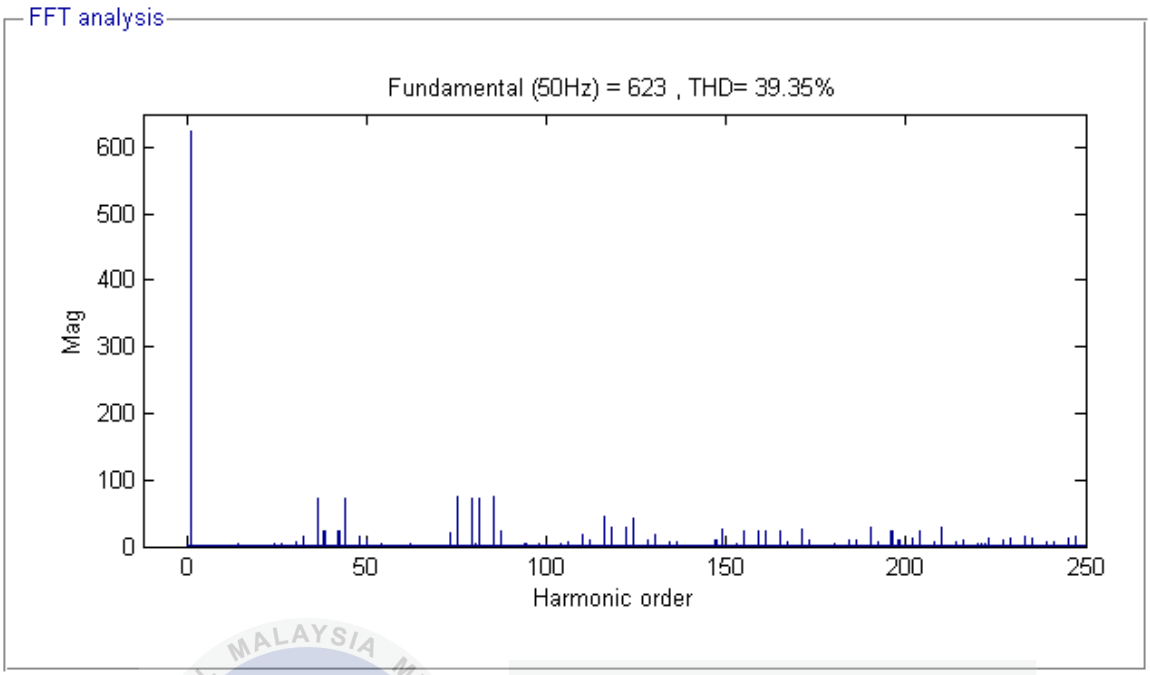


Figure C1: FFT analysis of line voltage for three-level PD switching modulation

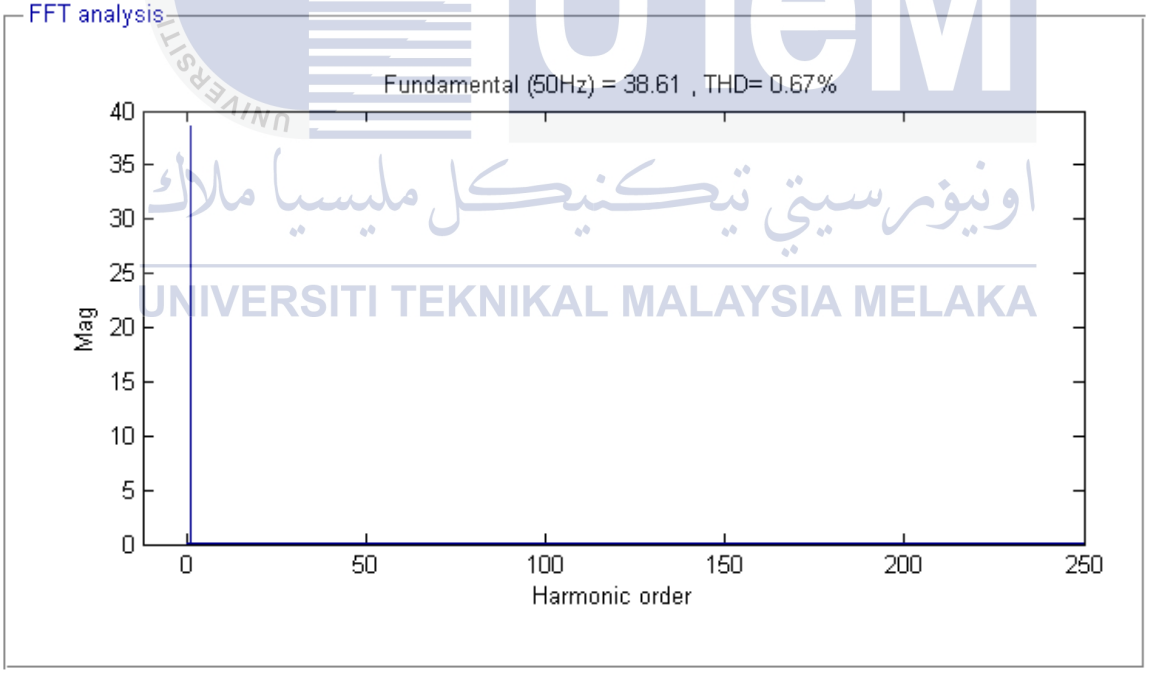


Figure C2: FFT analysis of output current for three-level PD switching modulation

Appendix D: FFT analysis of three-level POD switching modulation

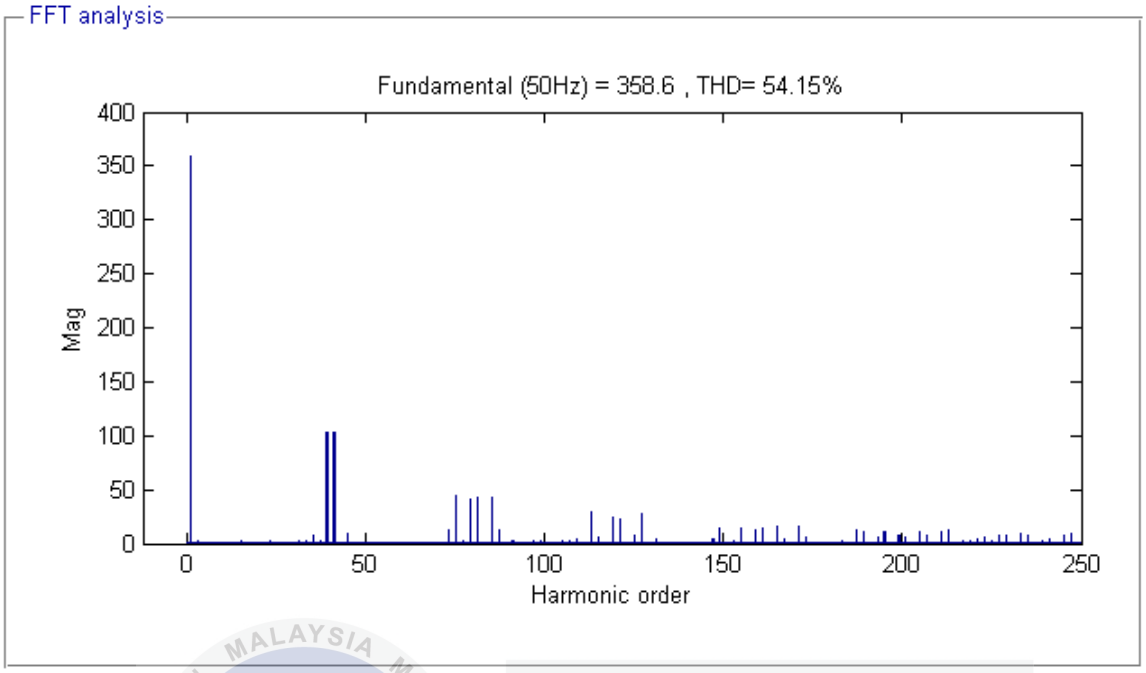


Figure D1: FFT analysis of line voltage for three-level POD switching modulation

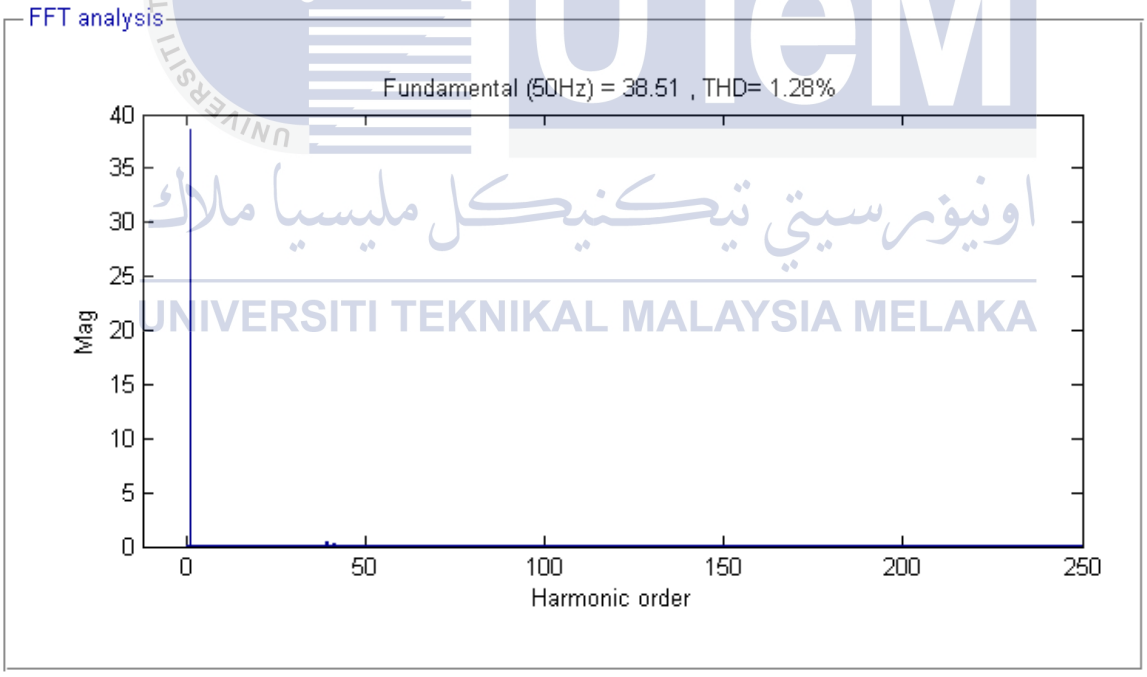
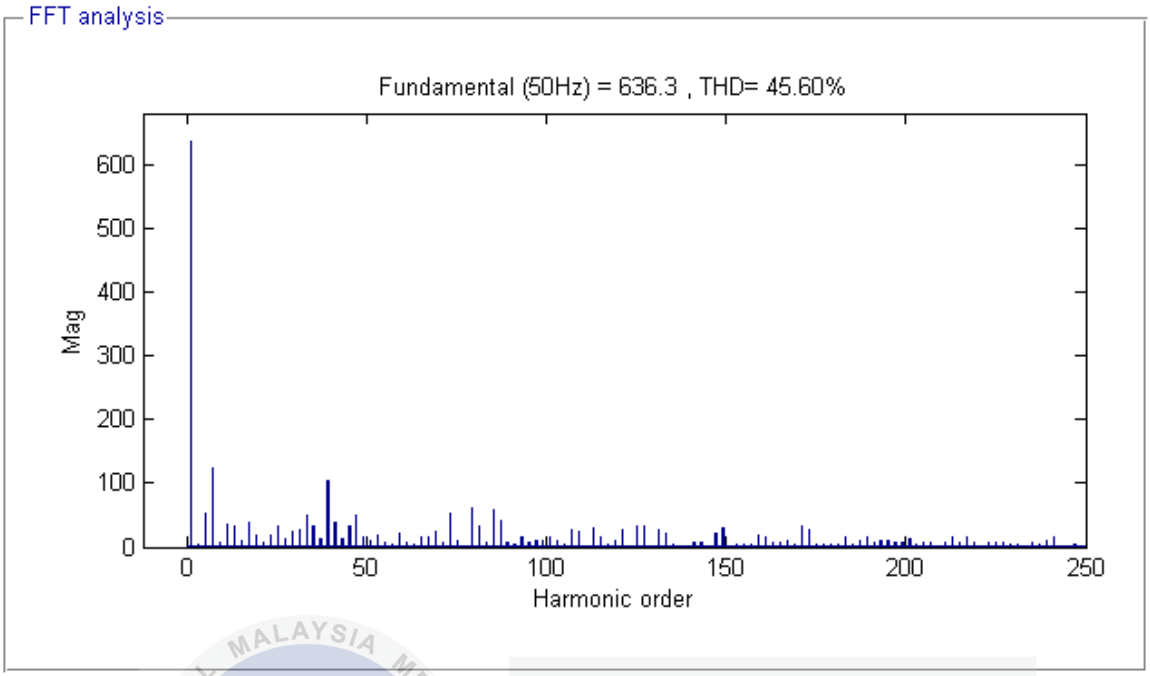


Figure D2: FFT analysis of output current for three-level POD switching modulation

Appendix E: FFT analysis of line voltage for three-level SVPWM



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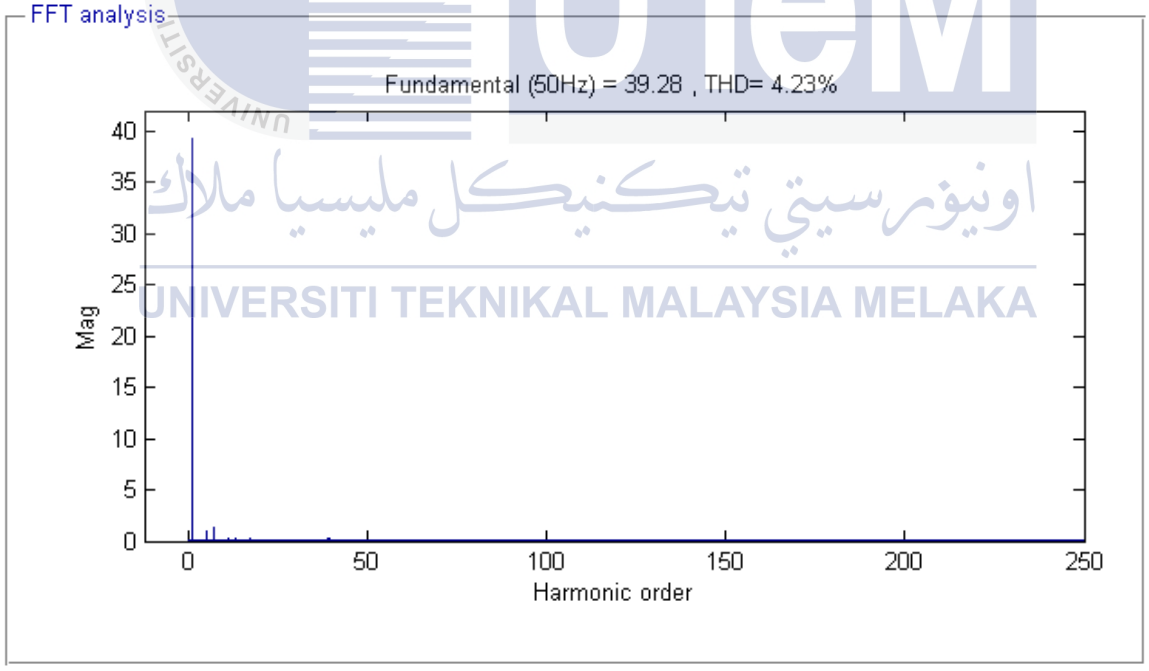


Figure E2: FFT analysis of output current for three-level SVPWM

Appendix F: FFT analysis of five-level PD switching modulation

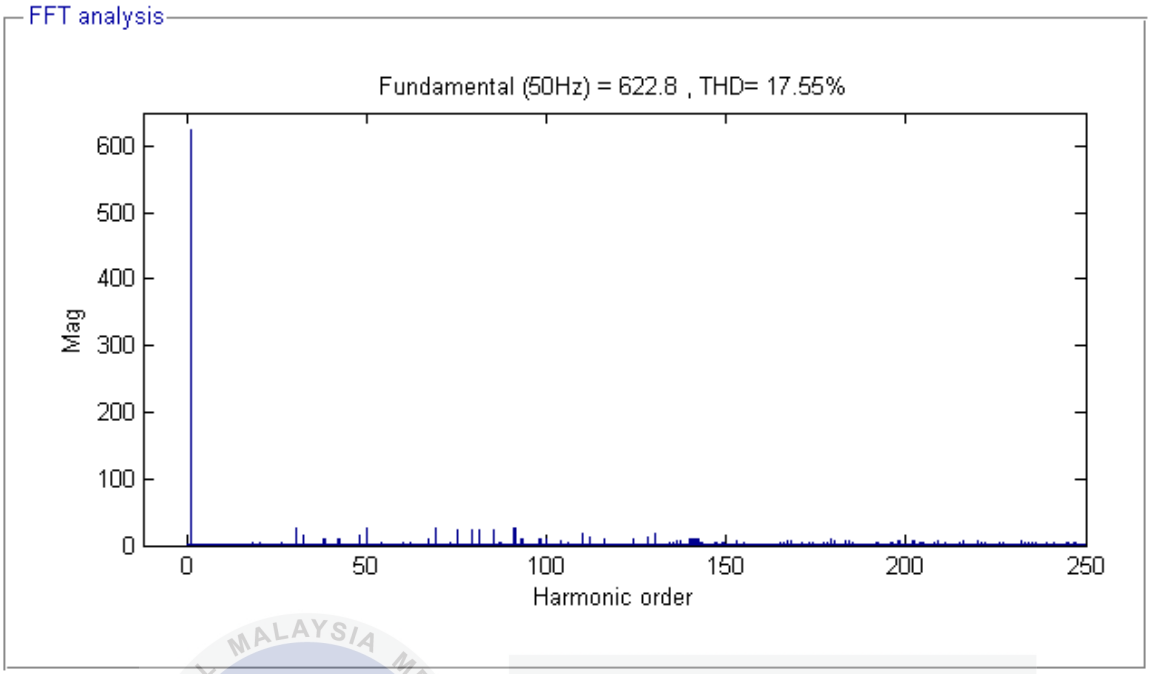


Figure F1: FFT analysis of line voltage for five-level PD switching modulation

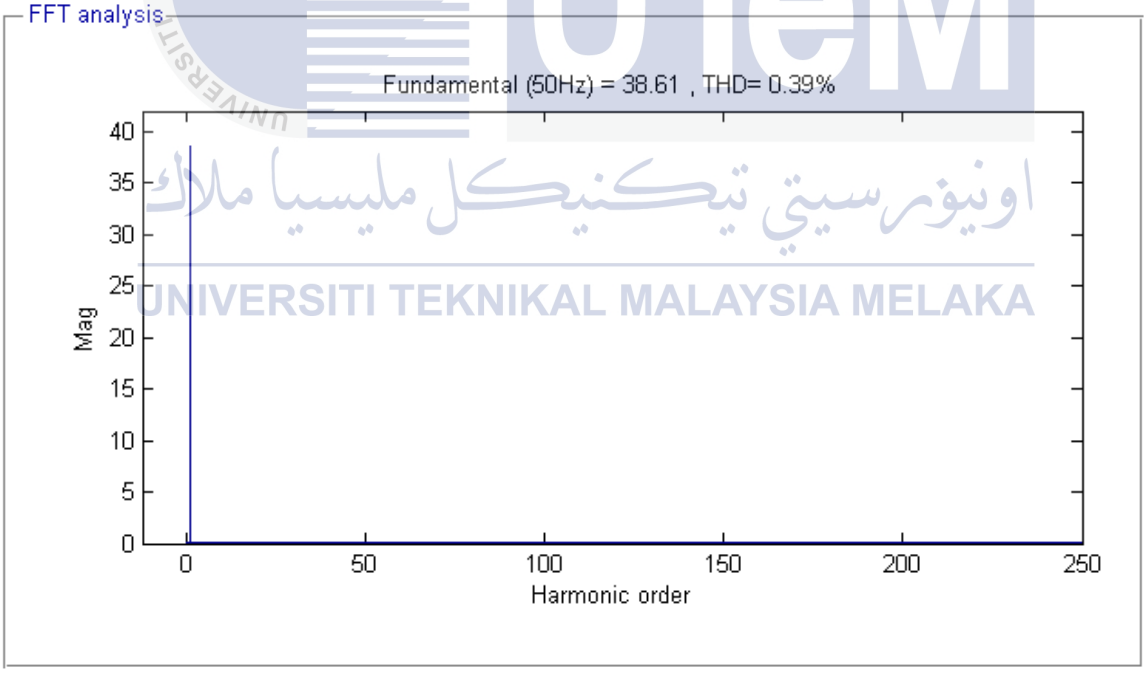
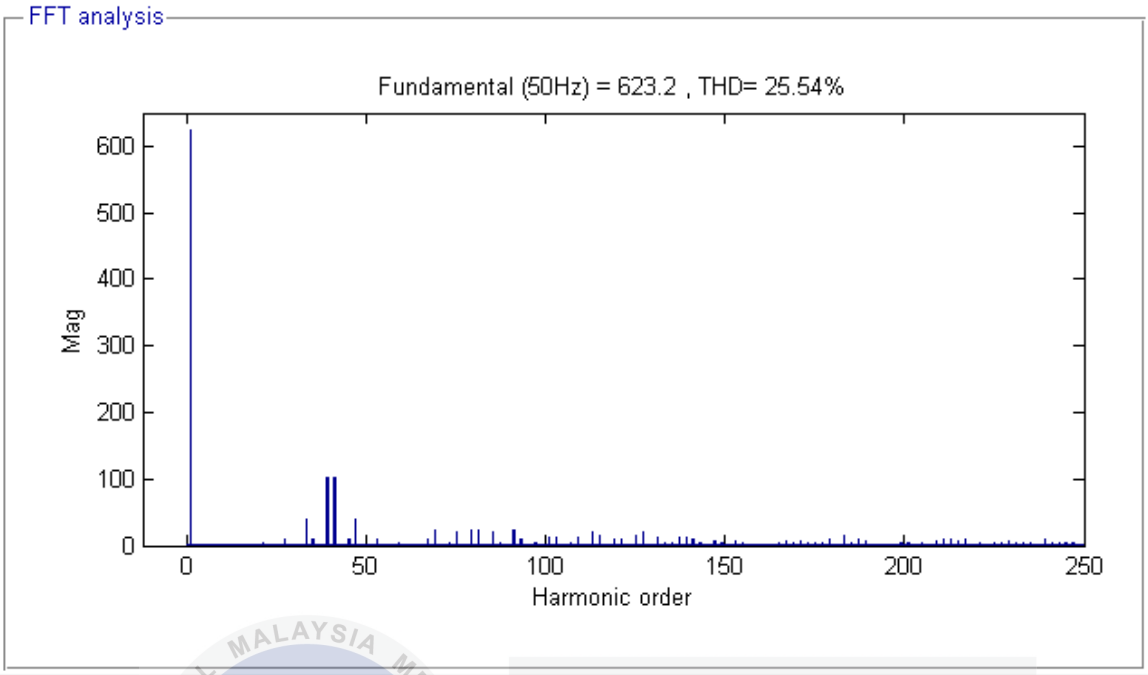


Figure F2: FFT analysis of output current for five-level PD switching modulation

Appendix G: FFT analysis of five-level POD switching modulation



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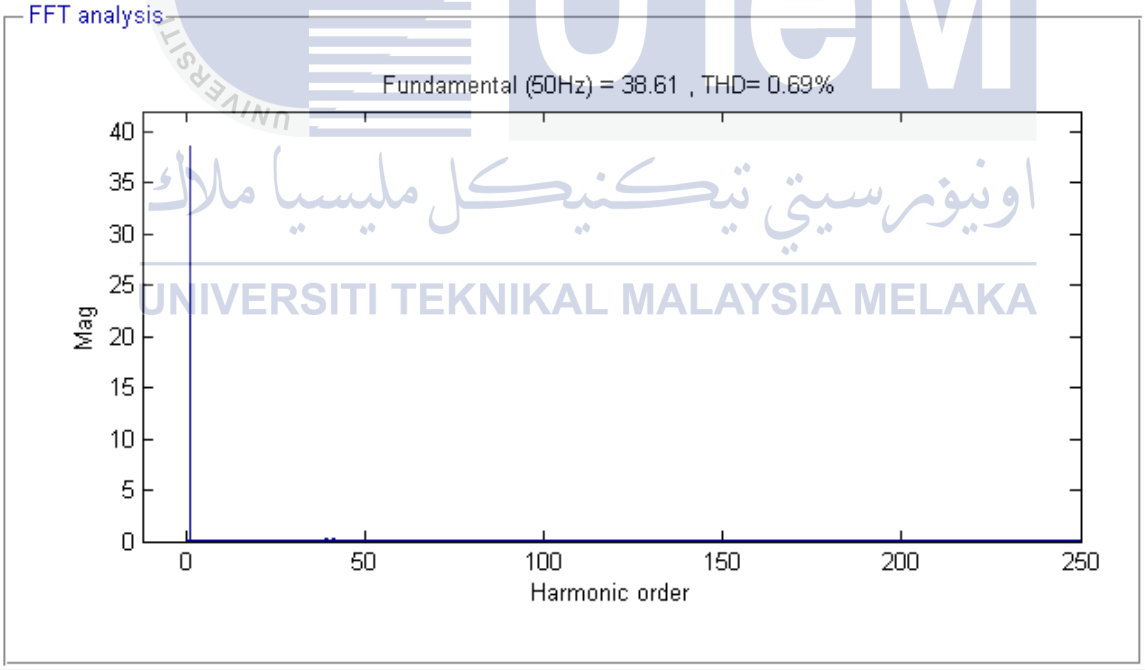

Figure G2: FFT analysis of output current for five-level POD switching modulation

Appendix H: FFT analysis of five-level APOD switching modulation

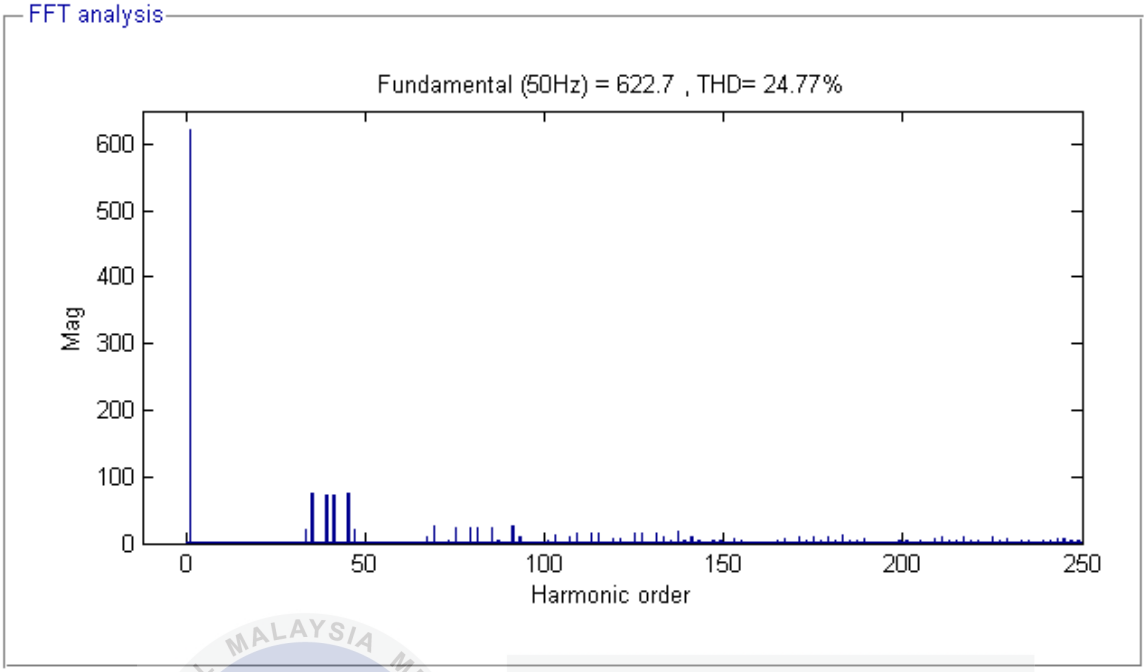

Figure H1: FFT analysis of line voltage for five-level APOD switching modulation

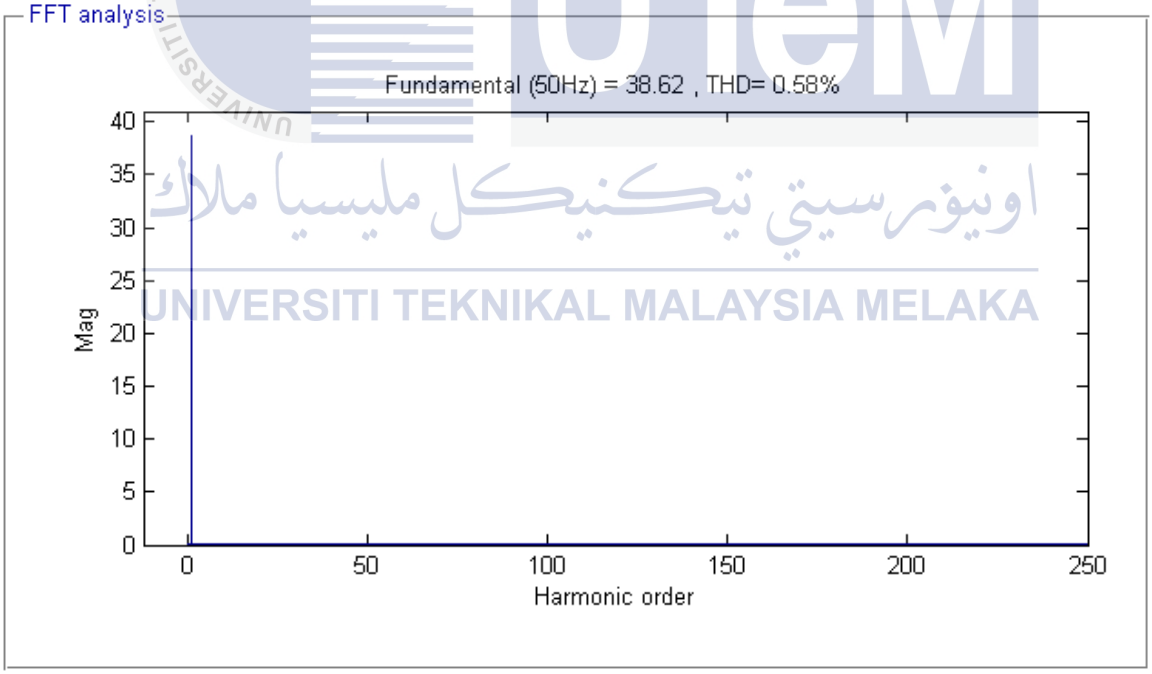

Figure H2: FFT analysis of output current for five-level APOD switching modulation