THE IMPACT OF GATE-INDUCED DRAIN LEAKAGE (GIDL) ON SCALED MOSFET FOR LOW POWER APPLICATION

THAILIS BOUNYA ANAK NGELAYANG

This Report Is Submitted In Partial Fulfilment of Requirements for the Bachelor Degree of Electronic Engineering (Computer Engineering) With Honours

FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

JUNE 2013

UNIVERSTI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN PROJEK SARJANA MUDA II

Tajuk Projek : THE IMPACT OF GATE-INDUCED DRAIN LEAKAGE ON SCALED MOSFET FOR LOW POWER APPLICATION

Sesi Pengajian : 2012/2013

Saya THAILIS BOUNYA ANAK NGELAYANG mengaku membenarkan laporan Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (√) :

☐	**SULIT***	(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐	**TERHAD***	(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)
☑	**TIDAK TERHAD**	

Thailis Bounya

(TANDATANGAN PENULIS)

Alamat Tetap: D/A LADAI ANCHALI,
SK NG PEDAI,
96700 KANOWIT,
SARAWAK.

Tarikh: 14TH JUNE 2013

Disahkan oleh:

(COP DAN TANDATANGAN PENYELIA)

Tarikh: 14TH JUNE 2013

"I hereby declare that this report is the result of my work except for quotes as cited in the references."

Signature : 

Author : THAILIS BOUNYA ANAK NGELAYANG

Date : 14TH JUNE 2013

"I hereby declare that I have read this report and in my opinion this report is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering (Computer Engineering) with Honours."

Signature : .....

Supervisor's Name : DR. ANIS SUHAILA BINTI MOHD ZAIN

Date : 14TH JUNE 2013

Special dedication for my beloved family especially to my parents,

Mr. Ngelayang Anak Asun and Mdm. Ladai Anchali.

Also for my kind hearted supervisor Dr. Anis Suhaila Binti Mohd. Zain.

ACKNOWLEDGEMENT

First and foremost, I would like to thank my highest gratitude to God for His blessing I have now completed my final year project for my Bachelor of Electronic Engineering (Computer Electronic) with Honours. Special thanks also to my supervisor Dr. Anis Suhaila Binti Mohd Zain for her willingness to take and supervise me for the duration of two semesters completing this project. She had helped me a lot on guiding and giving useful information regarding the needs of my project.

Special thanks also to the authority of my faculty, Faculty of Electronic and Computer Engineering for providing me with useful facilities especially in Microelectronic laboratory. I have spend a lot of times in this laboratory as my project can only be design and simulated using an authorised access account in the computer inside this laboratory.

Besides that, I would like to thank my family and friends who had provide me with numerous help in terms of financial aid and moral support. In time I am having breakdowns during the process of completing this project, they always be there giving me support and comforting me with useful advices.

ABSTRACT

This project is aimed to study the impact of Gate-Induced Drain Leakage (GIDL) on scaled Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for low power application. Nowadays, technology is growing rapidly with the increase demand from consumers all around the world. Microchip industries also undergo an evolution where the size of a device is getting smaller, but the performance is great. Thus, this project studies the leakage mechanism in terms of the GIDL current on MOSFET that operates for low power and its physical size had been reduced. The output of this project will determine on what is the implications of GIDL on the performance of MOSFET with various sizes that been supplied with low voltage power. The characteristic of GIDL was studied and from those characteristics, MOSFET design parameters were proposed by refer to International Technology Roadmap for Semiconductors (ITRS), 2011 edition. DEVEDIT and Atlas application in Silvaco TCAD software was used for this project. Three MOSFET with different physical gate length and several other parameters were designed in DEVEDIT application, then being simulated for data extraction in Atlas application. From the data extracted, it shows that as the size of MOSFET physical gate length become smaller, the leakage current tends to be higher. Apart from GIDL current (I_{GIDL}) value, the "ON" current (I_{ON}) value and threshold voltage (V_{TH}) value also been extracted for all MOSFET designs.

ABSTRAK

Projek ini bertujuan untuk mengkaji kesan Gate-Induced Drain Leakage (GIDL) pada Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) skala kecil yang dihubungkan dengan punca kuasa rendah. Hari ini, teknologi telah berkembang pesat sejajar dengan permintaan pelanggan yang tinggi. Industri microchip turut mengalami evolusi di mana saiz microchip semakin mengecil tetapi fungsinya masih di tahap optimum. Kajian projek ini berkisar mengenai mekanisma pembocoran dalam aspek arus GIDL pada MOSFET yang beroperasi menggunakan punca kuasa rendah dan saiz fizikalnya telah dikurangkan. Hasil kajian dalam projek ini akan menentukan apakah kesan GIDL terhadap fungsi MOSFET berkuasa rendah yang mempunyai pelbagai saiz. Ciri-ciri GIDL telah dikaji terlebih dahulu dan berdasarkan ciri-ciri ini, parameter reka bentuk MOSFET telah dicadangkan sejajar dengan garis panduan yang dikeluarkan oleh hala tuju teknologi semikonduktur antarabangsa (ITRS) edisi tahun 2011. Aplikasi DEVEDIT dan Atlas di dalam perisian Silvaco TCAD telah digunakan sepanjang penghasilan projek ini. Tiga reka bentuk MOSFET yang mempunyai panjang gate yang berbeza-beza dan beberapa parameter lain telah direka pada aplikasi DEVEDIT dan kemudiannya diuji pada aplikasi Atlas untuk tujuan pengekstrakan data. Berdasarkan data yang diekstrak, apabila saiz panjang gate semakin mengecil, nilai kebocoran arus semakin tinggi. Selain mengekstrak nilai arus GIDL, nilai arus pembuka dan nilai voltan ambang juga turut diekstrak untuk setiap reka bentuk MOSFET yang dibina.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

NO	TITLE	PAGE

LIST OF APPENDIX

CHAPTER 1

INTRODUCTION

1.1 Project Background

Gate-Induced Drain Leakage (GIDL) current is one of the major contributors to the overall Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) leakage. The sub-threshold conduction increases exponentially to the threshold voltage that is being reduced. Minimization of transistor off-state leakage current is important in designing MOSFETs for low power application. In this project, the characteristics of GIDL was studied to understand more on how did it happen and the analysis comparing GIDL current on several proposed MOSFET designs were carried out. Then, scaling criteria of MOSFETs was determined in order to know the types of scaling that is suitable to be conducted and on the same time, the impact of GIDL can be reduced with operation of using low power applications. Apart from that, the parameters that influence the impact of GIDL on scaled MOSFETs for low

power application was determined and discussed. Finally, the MOSFETs design following the parameters studied was constructed and been simulated by using SILVACO TCAD software. The impact of GIDL current on scaled MOSFETs for low power application was being discussed.

1.2 Problem Statement

Over four decades, semiconductor industry have undergoes various transformation in the improvement of its product. The electronic evolution had been really fast especially in this modernization era. It is due to the advancement of modern invention and technologies in the whole world. One of the electronic devices that also undergo fast evolution process is the Microchips.

Moores' Law stated that processor speed or an overall processing power for computers will double for every two years. [1] It specifically states that the number of transistors of an affordable Central Processing Unit (CPU) would double for every two years.

The early basic concept of the integrated circuit was to pack in multiple transistors, the devices that regulate current in a circuit, into a single, tiny chip, which would almost eliminate the distance between the circuits and therefore increase the speed with which electronic instructions flow through a computer. Today, most of the transformation is due to the ability of the industry to exponentially minimize the future sizes of the fabricated integrated circuit. The integration level is the most frequent cited trend. Companies worldwide invested more on their Research and Development due to the improvement trend which is the scaling of MOSFETs.

As the improvement of MOSFETs develops through times, the innovation of microchips had been evolved in many forms. The size of the microchips is getting smaller. As it goes smaller, it would save more production cost which wills benefits the producer. Apart from that, the performance of every microchips is undeniable had been improved a lot. Microchips today even operated using a very low power. This means that the power consumptions of each microchip were reduced.

However, despite of all those benefits, the engineers and scientists are having a hard time to solve several problems in order to make sure the newly invented microchip can perform well. One of the problems that they always encounter is the Gate-Induced Drain Leakage (GIDL) current. GIDL is a crucial issue for scaling of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). It is induced by the Band-to-Band Tunnelling (BTBT) effect in strong accumulation mode and generated in the gate-to-drain overlap region.[1] The surface BTBT or GIDL increases exponentially due to the reduced gate oxide thickness. Thus, this project investigates the impact of GIDL on scaled MOSFETs for low power application.

1.3 Aim and Objectives

The aim of this project is to study and investigate the impact of Gate-Induced Drain Leakage (GIDL) current on scaled Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for low power applications. In order to achieve this aim, there are several objectives that will be focussed on.

The first objective is to study the characteristics GIDL current and the implication of scaling MOSFETs on low power applications. The characteristics of GIDL current will be discussed to know on how it happens and what the impact towards the performance of MOSFET is. Besides that, the effect of scaling

MOSFETs on low power applications must be known to propose the suitable MOSFET design simulated with minimized impact of GIDL current.

Secondly, the objective is to propose the design parameters for scaled MOSFET for low power application. After the characteristics of GIDL and implications of scaling MOSFETs on low power application is known, the design parameters of MOSFET will be determine and proposed for the simulations.

Finally, the objective of this project is to investigate the impact on GIDL on scaled MOSFET based on the design parameters proposed. The MOSFET design will be carried out according to the design parameters that have been determine earlier. Through this designed MOSFET, the impact of GIDL current will be known and investigated.

1.4 Scope of Project

The purpose of implementing this project is to determine and investigate the impact of Gate-Induced Drain Leakage (GIDL) on scaled Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for low power applications. The first phase involves the research and study on the impact of Gate-Induced Drain Leakage (GIDL) current and it is only focused on low power application MOSFETs. The study includes the characteristics of GIDL current and the implications of scaling MOSFETs on low power applications. The second phase of this project is to propose suitable scaling parameters for MOSFET design and the impact of GIDL will be investigate. The designing and simulation process is carried out by using SILVACO TCAD software.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction to MOSFET

Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is a common type of transistor which carries charges such as electrons that flows along the channels. An electrode called the gate is controlling the width of the channel. It determines on how the devices is conducted. The gate is separated from channels by a thin layer of oxide insulation. [2] This insulation keeps the current from flowing between the gate and channels. MOSFET is useful for high speed switching applications and also on the integrated circuits in a computer.

The structure of MOSFET has two opposite doping regions of substrate. It is located at each edge of the MOS structure. The regions are called as the source and drain. A junction called as pn-junction exists between the source and drain region and the substrate.

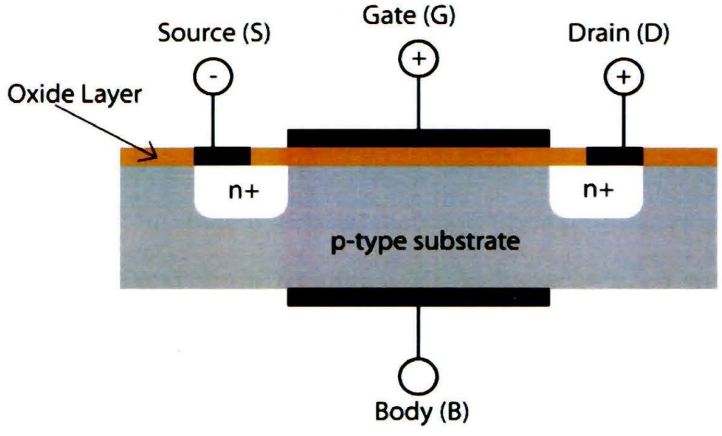

Figure 1: The structure of MOS device. [2]

If there is a connection at the terminals to all regions on the MOSFET, four subsequent terminals will exist. The terminal is designated as G (gate), S (source), D (drain) and B (substrate). One of these terminals can be designated as the common terminal. Thus, three independent terminal voltages can be applied to the MOSFET. [2] Somehow, there will be only one significant current will exists in an ideal MOSFET.

Assume the gate current is zero ($I_G = 0$) and the source and drain junctions are always kept under reverse bias during normal MOSFET operation. As in pn-junction, the reverse bias current can be considered negligible (and $I_G = 0$), the substrate current will also be inconsequential ($I_{sub} = 0$). Only the drain current (I_D) flow between the source and drain in MOSFET is needed to be considered. Thus, one current (I_D) and three independent terminal voltages is generally associated with the operation of an ideal MOSFET.

2.1.1 Basic Operation of MOSFET

The operation of MOSFET involves the application of an input voltage to the gate electrode. The result will be a perpendicular electric field to the Si-SiO_2 interface in the channel region of the device. This electric field can be varied by modulating the conductance of the channel region. Field - Effect Transistor (FETs) is an electric field that responsible for controlling the output of current flow.

Ren-Ji theory states that the drain current (I_D) will flow if voltage (V_{DS}) is applied between source and drain terminal. [3] Voltage induced n-type channel is assumed that it does not form unless the voltage applied to the gate exceeds the threshold voltage (V_{TH}).

In case of there is no gate bias been applied, two series of back-to-back pn-junctions exist between the source and drain circuit path.[4] If this be the case, when (V_{DS}) is applied, (I_D) will only consist of reverse-bias diode leakage current that can be negligible. However, when an NMOS transistor gate is applied with positive bias, electrons will tend to attach to the channel region and thus will repel the holes. When the positive gate voltage become optimum enough to form an inversion layer, an n-type channel will form, connecting the source and drain regions.

The Enhancement mode or normally OFF transistor refers to $V_{GS} = 0$, where there is no conducting channel exists. For NMOS enhancement mode transistor, positive gate voltage, V_{GS} applied must be greater than V_{TH} in order to create the channel or to turn it ON. However, for PMOS enhancement mode transistor, negative gate voltage with magnitude greater than V_{TH} needed to be applied. It is known that in NMOS transistor, positive voltage must also be applied to keep the drain-substrate reversed-biased, while in PMOS devices, the voltage need to be negative.

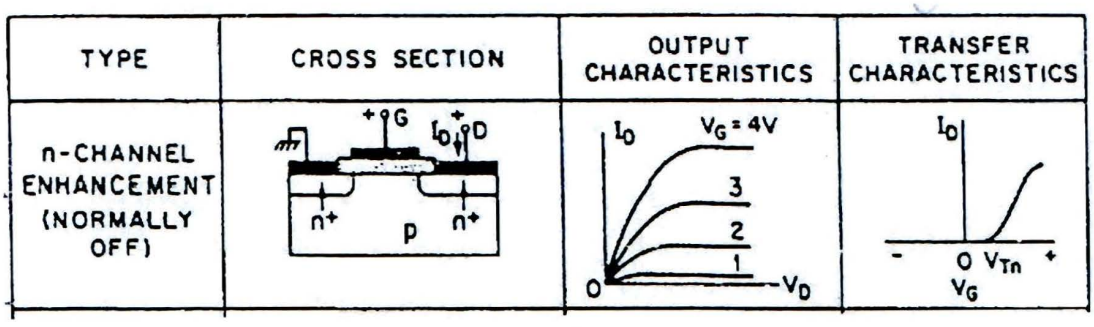

Figure 2: N-channel enhancement mode. [2]

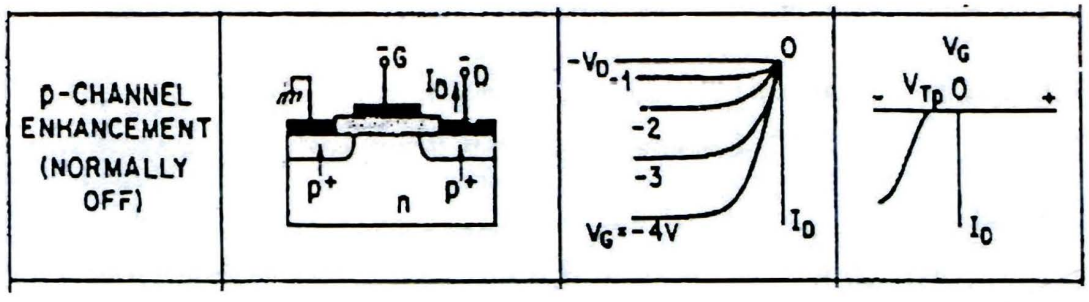

Figure 3: P-channel enhancement mode. [2]

Building MOS devices where the conduction region exists when $V_{GS} = 0$ is possible where this devices is normally ON. In order to turn them OFF, the channel region of majority carriers needed to be depleted. Bias voltage of the gate electrode is needed for the depletion. This device requires a negative gate voltage to turn it OFF. On the other hand, the corresponding PMOS device requires a positive gate voltage.