NOVEL STRUCTURE METHOD FOR REDUCING PUNCH THROUGH CURRENT IN DECANANO MOSFETS.

AYUNI FATEEHA BINTI MUDA

A thesis submitted in partial fulfillment of the requirements for the award of the degree of Bachelor of Electronic Engineering (Computer Engineering)

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka

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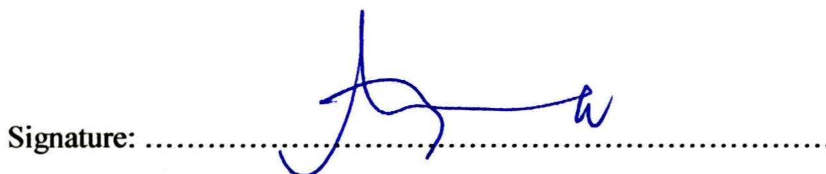

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Special dedicated to my late beloved father, my beloved mother, sister, brother and little sister

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ABSTRACT

Currently, the demand of faster and smaller devices, the researchers and semiconductor manufacturers are putting a lot of effort to face difficulties and challenges of improving of the performance of semiconductor devices from the conventional one. One of the solutions is to apply delta doping process to the conventional devices so that the punch through current is reduced and the devices performances are improved. In order to increase the mobility and the speed of the electronic devices, semiconductor technology researcher face the limitations such as punch through current in MOSFET device as it is unavoidable in scaling. The aim of this project is to reduce the punch through current in decanano MOSFET through delta doping process. Delta doping process is adding the Galium Arsenide (GaAs) in at the middle of junction depth to avoid depletion layer occurs. Technology Computer Aided Design (TCAD) tool from Silvaco's International® was to simulate the structure designed in this project. Silvaco's DevEdit software will be used to design a structure of MOSFET according to the steps, then, Silvaco's ATLAS software used to obtain its characteristics. The characteristics and result analysis such as transfer characteristics (Id-Vgs), sub threshold curves (log Id-Vgs) and output characteristics (Id-Vd) were obtain to compare the punch through current before delta doping and after delta doping process by adding the GaAS. Results analyzed in reducing punch through current in MOSFET give better performance in leakage current, speed and power consumption.

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ABSTRAK

Pada masa kini, bagi memenuhi permintaan yang semakin meningkat terhadap peranti elektronik yang cepat dan kecil, para penyelidik dan pengilang semikonduktor berusaha untuk menghadapi cabaran ini. Hal ini disebabkan peningkatan prestasi peranti semikonduktor daripada yang konversional merupaka satu tugasan yang sukar. Salah satu penyelesaian bagi masalah ini ialah proses pendopan ke dalam MOSFET konvensional supaya arus "punch through" dapat dikurangkan dan prestasi elektriknya bertambah baik. Selain itu, kajian terhadap peningkatan dalam mobiliti dan kepantasan peranti elektronik telah dilaksanakan oleh penyelidik teknologi semiconductor kini bagi melepasi batasan dalam MOSFET, contohnya, kesan arus "punch through" yang tidak boleh dielakkan semasa penskalaan. Tujuan projek ini adalah untuk mngurangkan arus "punch through" dalam MOSFET decanano melalui proses pendopan. *Technology Computer Aided Design (TCAD)* dari *Silvaco's International®* digunakan dalam projek ini untuk mensimulasi struktur yang dibina. Perisian *Silvaco's DevEdit* digunakan untuk membuat lakaran struktur MOSFET berdasarkan langkah dan arahan yang diberi, manakala perisian ATLAS digunakan untuk mendapatkan pencirian elektriknya. Pencirian dan analisis keputusan seperti pencirian pemindahan (Id-Vgs), lengkungan subthreshold (Id-Vgs) dan pencirian keluaran (Id-Vds) dilakukan untuk mendapatkan perbezaan arus "punch through" sebelum dan selepas proses pendopan dengan penambahan GaAs. Analisis keputusan yang diperolehi dari pengurangan arus "punch through" dari segi pengurangan kebocoran arus, kelajuan dan juga kurang pengambilan kuasa.

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LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal Oxide Semiconductor
MOSFET	-	Metal-Oxide-Semiconductor Field Effect Transistor
nm	-	nanometer
GaAs	-	Galium Arsenide
NMOS	-	N-channel MOSFET
PMOS	-	P-channel MOSFET
DIBL	-	Drain-Induces Barrier Lowering
TCAD	-	Technology Computer Aided Design
VLSI	-	Very Large Scale Integrated Circuits
C-V	-	Capacitance Voltage
DC	-	Direct current

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LIST OF SYMBOLS

Id	-	Drain Current
Vds	-	Drain to source Voltage
Vgs	-	Gate to source voltage
Vth	-	threshold Voltage
C	-	Capacitance
Ioff	-	Off current
Ion	-	On current
Isub	-	subthreshold leakage current
Ibtbt	-	reverse biased diode junction band to band tunnelling current

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CHAPTER I

INTRODUCTION

1.0 Project Introduction

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is large known as a popular device and is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications. The relative small size of MOSFET causes thousand of devices that can be fabricate into single integrated circuit design in other advantage to the electronic industry.

First and foremost, a basic understanding of the fabrication, operation, advantages, and applications of each device was needed before any simulations or optimizations could commence. This understanding of the devices was gained through extensive research conducted on each device.

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Various sources were consulted and resultant understanding of the devices was key in the creation of optimized device configurations.

MOSFET technology is an industry standard. This technology has been around for many years, and the fabrication methods are continually improving, yet they are well established. There has been a consistent gain in the performance of these devices every few years since their creation.

The cost and size are main advantages of MOSFET devices. Since the technology is well established, fabrication methods have been relatively inexpensive. Therefore, the device itself is physically smaller than other technologies, allowing for the placement of more devices on a silicon wafer during fabrication. MOSFET devices are mainly used in the creation of CMOS logic chips, which are at heart of every computer. An enhancement-type NMOS transistor was used during the course of this project.

Furthermore, punch through current in MOSFET occurs when the depletion layer between drain and source regions is merge into a single depletion region.When the punch through current occur, it will affect the current and drain-source volatge. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Iife the current is directly proportional to the drain-source voltage. The situation must not have be happened because it will increase the output conductance and the maximun operating volatage of the devices will limits. For this project, the effects of pucnhtrough current will be studied to understand more on how did it happens and finding solution to reduce it. Besides, also determine how to reduce the leakage. Then, will be determine the best solution to reduce punch trough current and at the same time reduce leakage.

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1.1 Problem Statement

In recent years, the demand for power sensitive designs has grown significantly due to the fast growth of battery-operated portable applications. As the technology scaling continues unabated, sub threshold device design has gained a lot of attention due to the low power and ultra-low-power consumption in various applications. Design of low-power high-performance submicron and deep submicron CMOS devices and circuits is a big challenge. One of the problems is punch through current that will be effect the function of the transistor. Punch trough current will make the leakage will occur. This causes the threshold voltage to be undesirably high since the gate silicon dioxide cannot be arbitrarily thin due to the concern over the direct tunnelling current. Moreover, the leakage must be avoided another effects such as it will the power consumption. The power dissipation also reduced and the speeds of the devices become slow. In addition, the most important is it will disturb the performances such as AC performance.

1.2 Aim and Objective

Aim: To reduce the punch through current in decananometre MOSFET.

Objectives:

1. To learn TCAD Silvaco software.
2. To design the MOSFET devices in 24, 16 & 9.8 decananometre scaling for reducing punch through current and leakage.
3. To determine and propose methods for reducing punch through current.

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1.3 Scope Of Project

This project is focused on designing the structure which is delta doping for reducing punch trough current in decananometre MOSFET. Besides, the parameters for these designs are 24nm, 16nm and 9.8nm. Furthermore, this project is conducted by using Silvaco's TCAD simulation tools which is DEVEDIT and ATLAS. The Silvaco's TCAD simulation tool is computer simulation software and used to design the proposed device structures.

1.4 Methodology

In this project, TCAD simulation are used to design MOSFET for gate length 24 nm, 16 nm and 9.8 nm and delta doping Galium Arsenide (GaAs). There are two important tools that have been used which are known as DEVEDIT and ATLAS. During the process to complete this project, the first step is to identify the punch through current, effects of the punch through current to the devices and method to reduce punch through current. After that, the devices are design by using DEVEDIT which is to design the structure and content of material that can be choosing according to the library tool. The next step is exact delta and device simulation by using ATLAS. From the ATLAS, the graph current and voltage curve can be determined. Lastly, analyze the graph from ATLAS which is can determine the performance of the punch through current. The result was compare between before and after adding delta doping (GaAs).

1.5 Project Outlined

This project consists of 6 chapters which are Chapter 1 will discuss about and introduction, objectives, scope project, methodology and problem statement. The chapter 2 contains theories and literature review part which is information about other relevant researches. For Chapter 3, the discussion will be on methodology and software implementation of this project. This chapter

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will show the flow of the project from the beginning of data collection until the acceptable results. Chapter 4 discussed about the result from the simulation Silvaco TCAD tool and punch through current characterization. Finally, the conclusion of this thesis is in Chapter 5 will include which is concluding the result and recommendation for the project.

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CHAPTER II

BACKGROUND STUDY

2.1 Punch through current

Punch through in a MOSFET is an extreme case of channel length modulation where the length reduces to zero. Punch through current occurs when depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

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