THREE BIT SUBTRACTION CIRCUIT VIA FIELD PROGRAMMABLE GATE ARRAY (FPGA)

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For father and mother dearest

Specially dedicated to my beloved parent, En Arasid bin Mohd Yasin and Pn. Siti Noraini binti Omar and also to my siblings who give the encouragement and support for me to completely this thesis. Not forgotten to my supervisor En Anuar bin Jaafar who gave me a lot of guidance and advices throughout this project until successful. I also want to thank to En Sani Irwan bin Md Salim who supported me a lot in finishing my final year project. Thank you very much to all of you.

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ABSTRACT

This project is about to design the software and hardware simulator for a Three Bit subtraction Circuit via FPGA. By design the Three bit subtraction circuit are involved in performing the subtraction for each bit by performs operation the arithmetic and logic unit, called the Arithmetic Logic Unit (ALU). All this operation is to display at seven segment using FPGA board by using Verilog language. A FPGA is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions such as additional, subtraction, multiplication, and divisions (+, -, x, ÷). In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memories. Combination of FPGA and ALU will produce the design of three bit subtraction circuit via FPGA.

ABSTRAK

Projek ini adalah untuk mereka bentuk perisian dan perkakasan untuk Tiga Bit penolakan melalui FPGA. Rekabentuk litar yang dihasilkan akan melaksanakan operasi penolakan yang melibatkan operasi aritmetik dan logik unit, yang dipanggil Unit Aritmetik logik (UAL). Semua operasi ini adalah untuk dipaparkan pada tujuh segmen menggunakan papan FPGA dengan menggunakan bahasa Verilog. FPGA adalah peranti semikonduktor yang mengandungi komponen logik boleh atur cara yang dipanggil "blok logik", dan diprogramkan. Blok logik boleh diprogramkan untuk melaksanakan fungsi get asas logik seperti logic DAN atau bahasa sintefiknya adalah “AND Gate”, dan juga menggunakan logic ATAU bahasa sintefiknya “XOR”, atau fungsi gabungan yang lebih kompleks seperti pengekod atau fungsi matematik yang mudah contohnya operasi penambahan, penolakan, darab dan operasi bahagi (+, -, x, ÷). Dalam kebanyakan FPGA, blok logik juga merangkumi elemen-elemen memori, yang mungkin mudah flip-flop atau lebih blok lengkap kenangan. Gabungan FPGA dan ALU akan menghasilkan reka bentuk tiga bit penolakan litar melalui FPGA.

TABLE OF CONTENTS

CHAPTER II: LITERATURE REVIEW

CHAPTER III: METHODOLOGY

CHAPTER IV: RESULT AND ANALYSIS

CHAPTER V: CONCLUSION AND RECOMMENDATIONS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

FPGA	-	Field Programmable Gate Array
ASIC	-	Application-Specific Integrated Circuit
UCF	-	User Constraints File
ISE	-	Integrated Software Environment
DSP	-	Digital Signal Processor
SOC	-	Systems on Chips
CLBs	-	Configurable Logic Blocks
LUT	-	Lookup Table

LIST OF APPENDIX

CHAPTER I

INTRODUCTION

1.1 Project Overview

This chapter will cover the introduction of the project. The chapter starts with a brief background of the project. Then, it provides the problem statements that are addressed by this project, followed by the objectives and scope. Finally, the organization of this thesis is given.

1.2 Problem Statement

This project is to design the software and a hardware simulator for a Three Bit subtraction Circuit Via FPGA. By design the Three bit subtraction circuit are involved in performing the subtraction for each bit by performs operation the arithmetic and logic unit, called the Arithmetic Logic Unit (ALU) example Addition, Subtraction, Multiplication and Division.

All this operation is to display at seven segment using FPGA board by using Verilog language. A FPGA is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions (+, -, x, ÷). In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memories. Combination of FPGA and ALU will produce the design of three bit subtraction circuit via FPGA.

The purpose of designing three bit subtraction is because if we want to do operation of subtraction we need three bit example 2 – 0 = 2 the integer is representing as bits. These three bits will be implemented as logic gates in order to obtain the result of subtraction. The process of subtraction will be latter discuss in chapter III.

The problem before this was FPGAs are usually slower than their application-specific integrated circuit (ASIC) counterparts, as they cannot handle as complex a design, and draw more power. If we represent two bits for subtraction it will not give any result. Therefore to obtain the result the minimum number of bits to be used is three bits.

1.3 Objectives

The main objective of this project is to design the three bit subtraction circuit via field programmable gate array (FPGA). To develop Verilog program for doing basic arithmetic instruction concept and basic information about the FPGA. Moreover, to design the Three bit subtraction involved in performing the subtraction for each bit by performs operation the arithmetic and logic unit, called the Arithmetic Logic Unit (ALU).

1.4 Scope of project

The main goal of this project is design Three Bit Subtraction Circuit Via FPGA. There is two scope will be cover in this project.

Firstly is to design circuit using structure model of verilog. Then simulation design with is to develop the coding of three bit subtraction circuit using the Verilog language. Simulate design will be run whether coding successful or not.

Secondly is to testing on the board which is trainer board FPGA Spartan II. Once coding of three bit subtraction is fully finish. The coding will be testing on board FPGA.

1.5 Chapter overview

This thesis comprises five chapters and that is Introduction, Literature Review, Methodology, Result and Analysis, and Conclusion and Recommendations.

Introduction has been provided in this chapter whereby it serves as the background for understanding the project described in this thesis.

Next, Chapter II reviews the theory on subtraction and research about work related to the project.

For, Chapter III discusses about the methodology that was followed during the course of this project.

Experimental results and analysis is presented in Chapter IV and finally, this thesis ends with Chapter V that concludes the project followed by a number of recommendations for future research.

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

In this chapter, reviews of the previous researches project that are related with this project will be discussed. The information becomes additional source for the project in becoming more successful.

To have a brief understanding of the researches related to the project, a few literature reviews had been done. This chapter will describe the related literature reviews.

2.2 Literature Review

A field-programmable gate array is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects [1]. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions [2].

In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memories. A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function hence the name "field-programmable"[1].

FPGAs are usually slower than their application-specific integrated circuit (ASIC) counterparts, as they cannot handle as complex a design, and draw more power. But their advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The designs are developed on regular FPGAs and then migrated into a fixed version that more resembles an ASIC. Another alternative are complex programmable logic devices (CPLDs). For this project, I have used the Xilinx Sparta-II FPGA.

2.2.1 Applications of FPGA

Applications of FPGAs include digital signal processor DSP, software-defined radio, aerospace and defense systems, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation and a growing range of other areas. FPGAs originally began as competitors to CPLDs and competed in a similar space, that of glue logic for PCBs. As their size, capabilities, and speed increased, they began to take over larger and larger functions to the state where some are now marketed as full systems on chips (SOC).FPGAs especially find applications in any area or algorithm that can make use of the massive parallelism offered by their architecture. One such area is code breaking, in particular brute-force attack, of cryptographic algorithms.

FPGAs are increasingly used in conventional High Performance Computing applications where computational kernels such as FFT or Convolution are performed on the FPGA instead of a microprocessor. The use of FPGAs for computing tasks is known as reconfigurable computing [1].

The inherent parallelism of the logic resources on the FPGA allows for considerable compute throughput even at a sub-500MHz clock rate. For example, the current (2007) generation of FPGAs can implement around 100 single precision floating point units, all of which can compute a result every single clock cycle. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. This has driven a new type of processing called reconfigurable computing, where time intensive tasks are offloaded from software to FPGAs. The adoption of FPGAs in high performance computing is currently limited by the complexity of FPGA design compared to conventional software and the extremely long turn-around times of current design tools, where 4-8 hours wait is necessary after even minor changes to the source code [2].

2.2.2 FPGA Architecture

The typical basic architecture consists of an array of configurable logic blocks (CLBs) and routing channels. Multiple I/O pads may fit into the height of one row or the width of one column in the array. Generally, all the routing channels have the same width (number of wires).

An application circuit must be mapped into an FPGA with adequate resources. A classic FPGA logic block consists of a 4-input lookup table (LUT), and flip-flop, as shown below. In recent years, manufacturers have started moving to 6-input LUTs in their high performance parts, claiming increased performance.