DESIGN OF SHALLOW SOURCE / DRAIN EXTENSION (SDE) PROFILES IN IMPROVING SHORT CHANNEL EFFECT (SCE_S) IN NANOSCALE DEVICES

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A thesis submitted in partial fulfillment of the requirements for the award of the degree of Bachelor of Electronic Engineering (Computer Engineering)

Faculty of Electronic and Computer Engineering
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This thesis is special dedicated to

My beloved family for their supports
and guide me throughout my academic career

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ABSTRACT

In this era globalization, the technology of world is growth fast especially in electronic revolution. The companies compete with each other to invent the new devices that can be multitasking and many applications. The engineers become smart to design the chip with small sizes. Besides, the architecture of the chip must be concern for the better performance of the electronic devices. One of the solutions is to design of shallow source/drain extension (SDE) alternative to the conventional devices so that the performance are improved. In order to increase the mobility and the speed of the electronic devices, semiconductor technology researchers face the limitations such as short channel effect in MOSFET device as it is unavoidable in scaling. The aim of this project is to improve the short channel effect in nanoscale devices. Technology Computer Aided Design (TCAD) tool from Silvaco's International® was used to design and simulate the structure designed in this project. Silvaco's DEVEDIT software was used to design the structure of MOSFET according to the steps, while Silvaco's ATLAS software was used to simulate the structure to obtain the output graph. The output graph and result analysis such as graph for transfer curves (I_D $-V_{GS}$) and graph for subthreshold curves (log I_D $-V_{GS}$) were obtain to compare the scaling the junction depth between the standard International Technology Roadmap Semiconductor (ITRS) structure with shallow source/drain extension (SDE) structure. Results analyzed in this project show the design of shallower junction depth structure improved the short channel effect for devices. Finally, this conventional NMOS has lower resistance and lower power consumption.

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ABSTRAK

Dalam era globalisasi kini, teknologi dunia semakin berkembang pesat terutama dalam revolusi elektronik. Kebanyakan syarikat bersaing antara satu sama lain untuk mencipta suatu alat peranti elektronik yang baru yang boleh melakukan pelbagai kerja dan mempunyai banyak aplikasi. Jurutera-jurutera semakin bijak dalam mereka bentuk cip bersaiz kecil. Selain itu, seni bina cip mestilah diberi perhatian untuk meningkatkan prestasi alat-alat elektronik. Salah satu cara penyelesaiannya adalah dengan mereka bentuk sumber/cerat yang cetek pada alat elektronik konvensional supaya prestasi alat tersebut meningkat. Dalam peningkatan mobiliti dan kelajuan alat elektronik, penyelidik teknologi semikonduktor berdepan dengan masalah seperti kesan saluran pendek dalam alat elektronik MOSFET kerana ia tidak dapat dielakkan dalam skala. Projek ini bertujuan untuk memperbaiki kesan saluran pendek dalam alat elektronik berskala nano. Technology Computer Aided Design (TCAD) tool dari Silvaco's International® telah digunakan untuk mereka bentuk dan mensimulasi reka bentuk yang telah di bina dalm projek ini. Perisian Silvaco's DEVEDIT telah digunakan dalam mereka bentuk binaan MOSFET berdasarkan langkah-langkah manakala perisian Silvaco's ATLAS telah digunakan untuk mensimulasi reka bentuk untuk mendapatkan keluaran graf. Keluaran graf dan analisis keputusan seperti graf bagi lengkungan pemindahan (I_D –V_{GS}) dan graf bagi lengkungan subthreshold (log I_D –V_{GS}) dikenalpasti untuk perbandingan skala kedalaman simpang antara reka bentuk standard International Technology Roadmap Semiconductor (ITRS) dengan reka bentuk sumber/cerat yang cetek. Analisis keputusan dalam projek ini menunjukkan reka bentuk kedalaman simpang yang cetek dapat memperbaiki kesan saluran pendek untuk alat elektronik. Oleh itu, konvensional NMOS mempunyai rintangan dan penggunaan kuasa yang rendah.

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and standard structure (ITRS)

LIST OF ABBREVIATIONS

MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
nm	-	nanometer
ITRS	-	International Technology Roadmap Semiconductor
TCAD	-	Technology Computer Aided Design
SCE_s	-	Short Channel Effects
VLSI	-	Very Large Scale Integrated Circuits
SDE	-	Source/Drain Extension
TED	-	Transient Enhance Diffusion
NMOS	-	N-channel MOSFET

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LIST OF SYMBOLS

I_D	-	Drain Current
V_D	-	Drain Voltage
V_{GS}	-	Gate-To-Source Voltage
V_{TH}	-	Threshold Voltage
L_G	-	Gate Length
I_{ON}	-	Drive Current

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CHAPTER I

INTRODUCTION

This project use SILVACO TCAD tools to design MOSFET structure process and device simulation. The introduction of the study is thoroughly elaborated. This chapter also outlined on the objectives and scope of the research.

1.1 Project Background

More than 30 years, the Metal - Oxide - Semiconductor Field-Effect Transistor (MOSFET) has continually been scale down in size in channel length from micrometres to sub - micrometres and then to sub - micrometres range following Moore's Law. The channel length of MOSFET is reducing from 100nm to 45nm. The size reduction of the device makes great improvement to MOSFET operation.

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However, there have many effects when reduction the scale size of the MOSFET. The one of the effect is short channel effect.

Short channel effect is an effect of the channel length of a MOSFET is the same order of magnitude as the depletion-layer widths of the source and drain junction, behaves differently from other MOSFETs. There are two physical phenomenon of the short channel effect. The first is the limitation imposed on electron drift characteristics in channel and the second is the modification of the threshold voltage due to the shortening channel length. In this project, the source/drain extension has been selected to be studied. The concept that influence for scaling the shallow source/drain extension (SDE) must be known for improving the short channel effect. Finally, the design of shallow source/drain extension (SDE) will be proposed.

1.2 Problem Statement

Nowadays, MOS device technologies have been improving at a dramatic rate. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The ability to improve performance consistently while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. Transistor delay times have decreased by more than 30% per technology generation resulting in a doubling of microprocessor performance every two years. In order to maintain this rapid rate of improvement, aggressive engineering of the source/drain and well regions is required. As the MOSFET technology is approaching nano scaling, short channel effect becomes more considerable as the channel length is reduced. Thus, one of the important parts is to design the shallow source/drain extension profiles in improving the short channel effect in nanoscale devices.

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1.3 Objectives

Aim: To improve the short channel effect (SCE_S) in nanoscale devices.

The main objective of this project is:

i. To design the shallow source/drain extension (SDE) profiles for gate length 24nm, 16nm & 9.8nm.
ii. To analyze and simulate the results of improving short channel effect using the SILVACO Software.

1.4 Scope of Project

This project focus on the design the shallow source/drain extension (SDE) profiles for improving the short channel effect. Design of the NMOS transistor is carried out using Silvaco's DEVEDIT software while the simulation was done using Silvaco's ATLAS software.

From the project, the required parameters of every fabrication steps and order of fabrication steps are very important to ensure a proper MOSFET device was fabricated. On the other hand, it also highlighted some MOSFET characteristics that need to be studied such as transfer characteristics ($I_d - V_{gs}$) and subthreshold curves ($\log I_d - V_{gs}$). After that, this MOSFETs design gate length 24nm, 16nm and 9.8nm is propose for nanoscale devices.

1.5 Summary of Work

This project will be carried out in two semesters. The first part of the project is done in the first semester where the understandings of literature review and methodology that will use are done. Gathering information is needed in order to

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