

**DESIGN OF A UWB AMPLIFIER BASED ON CSSDA FOR UWB
APPLICATIONS**

ASREEN ANUAR BIN ABD AZIZ

**This report is submitted in partial fulfillment of requirements for the award of
Bachelor of Electronic Engineering (Telecommunication Electronics) with honors**

**Fakulti Kejuruteraan Elektronik Dan Kejuruteraan Komputer
Universiti Teknikal Malaysia Melaka**

MAY 2007



UNIVERSITI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN
PROJEK SARJANA MUDA II

Tajuk Projek : DESIGN A UWB AMPLIFIER BASED ON CSSDA FOR
UWB APPLICATION
Sesi Pengajian : 2006/2007

Saya ASREEN ANUAR BIN ABD AZIZ

mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan () :

SULIT*

(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)

TERHAD*

(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)

TIDAK TERHAD

(TANDATANGAN PENULIS)

Alamat Tetap: LOT 987, KG. TANJONG PAGAR,
16450 KETEREH, KOTA BHARU,
KELANTAN.

Tarikh: 11 MEI 2007


Disahkan oleh:

MORAMAD ZAINAL ABDIN BIN ABD AZIZ


Pensyarah
Fakulti Kej. Elektronik dan Kej. Komputer (FKEKK),
Universiti Teknikal Malaysia Melaka (UTeM),
Karung Berkunci 1200,
Ayer Keroh 75450 Melaka

Tarikh: 15/05/07

“I hereby declare that this report is the result of my own work except for quotes as cited
in the references.”

Signature :..........
Author : Asreen Anuar Bin Abd Aziz
Date : 11 May 2007

“I hereby declare that I have read this report and in my opinion this report is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering (Telecommunication Electronics) with honors.”

Signature : 

Supervisor's Name : Mohamad Zoinol Abidin Bin Abd Aziz

Date : 11 May 2007

Specially Dedicated:
To my beloved mom and dad
and of course to all my supportive friends...

ACKNOWLEDGEMENT

First and foremost, thank the gracious Allah, the God All Mighty for all his numerous blessings bestowed upon me in various ways. My great thanks to my supervisor Mr. Mohamad Zoinol Abidin B. Abd Aziz for his constant support, effort and patience in helping me to finish this project. His motivation makes me work extra hard to complete this project, and all his effort is priceless.

Also my appreciation to all my classmates who always give their effort to teach me how to use Advance Design System (ADS2004A) and Microwave Office software, all yours idea and helps are prices. My special gratitude to my past supervisor, Mr. Adlishah B. Zakaria who introduced me this project.

Last but not least, my sincere thanks to all those who have helped me to complete this project thanks to all those helping to finish this project. Special regards to my parents, sister and brother whose encouragement, support and understanding have me the strength and courage to successfully complete this project.

ABSTRACT

Ultrawideband (UWB) is a wireless technology that transmits an extremely low-power signal over a wide radio spectrum. Ultrawideband systems operate across a wide range of frequencies from 3.1 GHz to 10.6 GHz. As no carrier wave is needed, ultrawideband consumes extremely low power and a long battery life is possible. In this report, the UWB amplifier has been designed and simulated with Radio Frequency (RF) Computer Aided Design (CAD) TOOLS - the Advanced Design System 2004A (ADS 2004A) for operation frequency between 3 GHz and 10 GHz. This UWB amplifier was designed by using the Pseudomorphic High Electron Mobility Transistor (PHEMT) device, the FPD6836P70 produced by Filtronic Semiconductor UK Company. The main specifications requirement for the circuit was to get a flat gain around $15 \text{ dB} \pm 5 \text{ dB}$ and overall with a reflection coefficient below 10 dB. The first stage of designing the broadband amplifier is to select the type of transistor which is suitable for low noise amplifiers. After that, the biasing circuit input matching network and output matching network were designed. The simulations for the design in ADS2004A include the DC analysis and also S-parameter simulation. Optimization for the circuit was done by changing the lengths and widths values of the microstrip lines.

ABSTRAK

Ultra Jalur-Lebar (UWB) adalah teknologi tanpa wayar yang menghantar isyarat kuasa rendah melalui satu jalur lebar bagi spectrum radio. Sistem Ultra Jalur-Lebar beroperasi merentasi satu julat frekuensi dari 3.1 GHz ke 10.6 GHz. Oleh sebab tiada gelombang pembawa diperlukan, Ultra Jalur Lebar boleh menggunakan kuasa yang tersangat rendah dan jangka hayat bateri adalah panjang. Dalam tesis ini, penguat Ultra Jalur Lebar direka cipta dan disimulasi dengan menggunakan perisian Radio Frequency (RF) Computer Aided Design (CAD) Tools - Advanced Design System 2004A (ADS2004A) untuk frekuensi operasi antara 3 GHz hingga 10 GHz. Penguat Ultra Jalur-Lebar juga telah direka dengan menggunakan peranti Pseudomorphic High Electron Mobility Transistor, iaitu model FPD6836P70 yang dibangunkan oleh syarikat Filtronic Semiconductor UK. Spesifikasi utama yang diperlukan untuk litar penguat adalah untuk mendapatkan satu gandaan rata sekitar $15 \text{ dB} \pm 5 \text{ dB}$ pada keseluruhannya dengan pekali pantulan dibawah 10 dB. Peringkat pertama untuk merekacipta penguat jalur lebar ialah dengan memilih jenis transistor yang sesuai untuk penguat hingar rendah. Kemudian, litar pincangan padanan masukan dan litar pincangan padanan keluaran direka. Keseluruhan simulasi untuk litar penguat dibuat dalam perisian ADS2004A dan juga termasuk analisa arus terus (AT) dan juga simulasi parameter-S. Optimisasi bagi litar telah dilakukan dengan mengubah nilai panjang dan lebar pada garisan jalur mikro.

CONTENTS

CHAPTER	TITLE	PAGE
	PROJECT TITLE	i
	REPORT STATUS APPROVAL FORM	ii
	DECLARATION	iii
	SUPERVISOR'S APPROVAL	iv
	DEDICATION	v
	ACKNOWLEDGEMENT	vi
	ABSTRACT	vii
	ABSTRAK	viii
	CONTENTS	ix
	LIST OF TABLE	xii
	LIST OF FIGURES	xiii
	LIST OF ABBREVIATION	xv
	LIST OF APPENDICES	xx
I	INTRODUCTION	
	1.1 Introduction	1

1.2	Problem Statement	3
1.3	Objectives	3
1.4	Scope of Work	4
1.5	Methodology	4
1.6	Thesis Structure	5
II	BACKGROUND STUDY	6
2.1	UWB Basics	6
2.2	UWB Applications	8
2.3	UWB Standards	9
2.4	Principles of CSSDA	12
2.5	Stage Design of CSSDA	16
2.6	Basic Concepts in Low Noise Amplifier Design	20
2.6.1	Characteristic of Microwave Transistors	20
2.6.2	DC Biasing	25
2.6.3	Two – Port Power Gain	28
2.6.4	Single Stage Amplifier	32
2.6.5	Stability Consideration	33
2.5.6.1	Consideration for Stability in High Frequency Amplifier Design	33
2.5.6.2 i)	Decision by Formula	33
ii)	Decision by Stability Circles	33
2.5.6.3	Stability Test	35
2.6.6	Input and Output Matching	35
2.6.6.1	Quarter-Wave Transformer	36
2.6.7	Low Noise Amplifier Design	40

III	PROJECT METHODOLOGY	41
3.1	Introduction	41
3.2	Transistor Selection	41
3.3	Design Calculation	43
3.3.1	Stability Consideration	44
3.3.2	Matching Point and Gain Calculation	45
3.3.3	Noise Figure Calculation	46
3.4	Design Simulation	48
3.4.1	Single Stage LNA Design	48
3.4.1.1	Stability Simulation	48
3.4.1.2	DC Biasing Simulation	49
3.4.1.3	Matching Network Simulation	51
3.4.1.4	Noise Figure Simulation	59
3.4.2	Two Stage LNA Design	61
3.4.3	Three Stage LNA Design	62
IV	RESULTS AND DISCUSSION	63
4.1	Design Calculation Result	63
4.1.1	Selection of Transistor	63
4.1.2	Stability Consideration	63
4.1.3	Gain Calculation	64
4.1.4	Constant Noise Circle	65
4.2	Design Simulation Result	66
4.2.1	Stability Simulation Result	66
4.2.2	DC Biasing Simulation Result	66
4.2.3	Matching Simulation Result	68
4.2.3.1	Single Stage LNA Design	69
4.2.3.2	Two Stage Design	77

	4.2.3.3 Three Stage Design	79
V	CONCLUSION AND SUGGESTION	82
	5.1 Conclusion	82
	5.2 Future Work	83
	REFERENCES	84
	APPENDICES	91

LIST OF TABLES

NO	TITLE	PAGE
2.1	Comparison of Gain and Noise Figure of Microwave Transistor	20
2.2	Curtice 3 model specification of the FPD6836 transistor	43
3.1	S-parameter data for frequency 3 GHz to 10 GHz at bias point $V_{DS}=5$ V and $I_{DS}=55$ mA.	45
3.2	S-parameter for transistor model at $V_{DS}=5$ V and $I_{DS}=55$ mA	51
4.1	K and Δ value for biasing at $V_{DS}=5$ V and $I_{DS}=55$ mA.	66
4.2	Gain Calculation Result	66
4.3	Center and radius for constant noise circle	67
4.4	Drain source current (I_{DS}) and Gate voltage (V_{GS}) respectively	69

LIST OF FIGURES

NO	TITLE	PAGE
2.1	Acceptable power levels for indoor and outdoor emissions	7
2.2	Power levels of UWB signal and a typical narrowband signal	8
2.3	Time and frequency waveforms of DS-CDMA proposal	10
2.4	Band plan of MB-OFDM proposal	11
2.5	Time and frequency waveforms of DS-CDMA proposal	11
2.6	The CSSDA	13
2.7	The small signal of n stage CSSDA	13
2.8	The different in small signal gain between CSSDA and TWA	14
2.9	Schematic diagram for first stage of CSSDA	16
2.10	Schematic diagram for second stage of CSSDA	17
2.11	Last stage of CSSDA	18
2.12	Two stage CSSDA	19
2.13	Physical Form of Transistor	21
	(a) Cross section of a GaAs FET	21
	(b) Top view, showing drain, and gate and source contacts.	22
2.14	Small-signal equivalent circuit for a GaAs FET in the common-source configuration	23
2.15	Transistor Structure	24
	(a): GaAs MESFET Structure	24
	(b): PHEMT Structure	24
2.16	Five basic dc bias networks	28

2.17	A two-port network with general source and load impedances	30
2.18	The general transistor amplifier circuit.	33
2.19	Output stability circle	35
2.20	Input stability circles	35
2.21	A lossless network matching networks arbitrary load impedance to a transmission line	37
2.22	Matching with a single section quarter-wave transformer	38
2.23	The quarter-wave transformer solution	40
3.1	P70 package model of the FPD6836P70 transistor	44
3.2	Calculation design process flow chart	49
3.3	The set-up for stability simulation	50
3.4	DC biasing simulation schematic.	52
3.5	Input matching network analysis	53
3.6	Matching network for S_{11}	54
3.7	S_{11} plotted on Smith chart.	55
3.8	Tune parameter to set-up length and width	55
3.9	Input Impedance result after adjusted	56
3.10	Input matching network schematic	57
3.11	Output matching network analyses	58
3.12	Output matching network.	58
3.13	S_{22} plotted on Smith chart	59
3.14	Tune parameter to set-up length and width.	59
3.15	Output Impedance result after adjusted.	60
3.16	Output matching network schematic.	61
3.17	Noise figure simulation schematic.	62
3.18	The flow chart of designed simulation process.	62
3.19	Two stage LNA design	63
3.20	Three Stage LNA design	64
4.1	Stability Simulation Result	68
4.2	Drain-source current (I_{DS}) versus Gate voltage (V_{GS}).	69
4.3	DC annotation with specific DC supply.	70

4.4	S_{12} and S_{21} result before matching.	71
4.5	S_{12} and S_{21} after input and output matching network included	72
4.6	S_{11} and S_{22} after input and output matching network included.	73
4.7	Minimum Noise Figure.	73
4.8	S_{12} and S_{21} after input and output matching network included.	74
4.9	S_{11} and S_{22} after input and output matching network included.	75
4.10	Minimum Noise Figure.	75
4.11	S_{12} and S_{21} after input and output matching network included.	76
4.12	S_{11} and S_{22} after input and output matching network included.	77
4.13	Minimum Noise Figure.	77
4.14	Input and output matching network schematic.	78
4.15	S_{21} and S_{12} for 2-Stage at 5.5 GHz and 6.5GHz.	79
4.16	S_{11} and S_{22} for 2 –Stages design at 5.5 GHz and 6.5 GHz.	80
4.17	Minimum noise figure for 2-Stage.	80
4.18	Input and output matching network schematic for 2-Stage Design at 5.5 GHz and 6.5 GHz.	81
4.19	S_{21} at 3-Stage Design.	81
4.20	S_{11} and S_{22} for 3-Stage Design.	82
4.21	Minimum Noise Figure for 3-Stage Design.	83
4.22	Input and output matching network schematic for 3-Stage Design.	83

LIST OF ABBREVIATIONS

ADS	- Advance Design System
B	- Bandwidth
CAD	- Computer Aided Tool
CMOS	- Complementary Metal-oxide Semiconductor
DC	- Direct current
F	- Noise Figure
BJT	- Bipolar Junction Transistor
FR4	- Flame Retardant 4
Freq	- Frequency
GaAs	- Gallium Arsenide
GHz	- Giga Hertz
IEEE	- Institute of Electrical and Electronic Engineering
K	- Rollet stability factor
k	- Boltzman's constant
LAN	- Local Area Network
LNA	- Low Noise Amplifier
mag	- Magnitude
MESFET	- Metal Semiconductor Field Effect Transistor
MHz	- Mega Hertz
MMIC	- Monolithic Microwave Integrated Circuit
MOSFET	- Metal Oxide Field Effect Transistor
N	- Noise Figure Parameter
P	- Power

pHEMT	- Pseudomorphic High Electron Mobility Transistors
R	- Resistance
RF	- Radio Frequency
RFIC	- Radio Frequency Integrated Circuit
UNII	- Unlicensed National Information Infrastructure
VSWR	- Voltage Standing Wave Ratio
WLAN	- Wireless Local Area Network
Γ	- Reflection Coefficient
Γ_{vt}	- Input reflection coefficient
Γ_{Λ}	- Load reflection coefficient
Γ_{Σ}	- Source reflection coefficient
*	- Multiply
λ	- Wavelength
Δ	- Determinant of the scattering matrix
Ω	- Ohm
$^{\circ}\text{C}$	- Celsius
K°	- Kelvin
<i>CF</i>	- Center of constant noise circle
dB	- Decibel
<i>E_{Eff}</i>	- Electrical length
<i>Freq</i>	- Frequency in ADS
<i>Fmin</i>	- Minimum noise figure (equivalent to NFmin from ADS)
g	- Gram
G	- Gain
GA	- Available gain
GT	- Transducer gain
<i>H</i>	- Substrate thickness
<i>l</i>	- Length of quarter-wave transformer
<i>L</i>	- Length
<i>Ni</i>	- Noise parameter
<i>RF</i>	- Radius of constant noise circle

<i>rms</i>	- Root mean square
V	- Volt
<i>W</i>	- Width
mA	- Milliampere
<i>ml</i>	- Milliliter
Z	- Impedance
Z _o	- Characteristic impedance
Z _T	- Transformer impedance
Z _{in}	- Input impedance
Z _L	- Load impedance
z _{in}	- Normalize value of input impedance
z _L	- Normalize value of load impedance
SiGe	- Silicon Germanium

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	Gantt chart	91
B	FPD6836P70 data sheet	92
C	Impedance Matching	93
D	FPD6836P70 Noise Data	94
E	Matching Network at Two Stage Design	95
F	Single Stage Transistor Calculations	96
G	Input and Output Matching Design Using Smith Chart.	97

CHAPTER I

INTRODUCTION

1.1 Introduction

Over recent years, the interest in microwave techniques for communication systems has grown tremendously and also the development and the performance of microwave active and passive circuits for wireless technologies has become extremely advanced. Microwave amplifiers have become among the most critical active circuits that are employed in many the system applications. Broadband amplifiers with good performance have been successfully realized in the past 3 decade in hybrid and monolithic technologies. Therefore, the wide bandwidth amplifiers have been firmly established in the fields of microwave, optical communication, instrumentation and Electronic War (EW) [1].

The implementation of Low Noise Amplifier (LNA) in the front-ends is one of the challenging aspects in emerging Ultrawideband (UWB) radio frequency (RF) systems. The design of broadband amplifier introduces new difficulties which require careful considerations. Basically, the design of amplifier over a broad frequency range is a matter of properly designing the reactively matched circuit, traveling wave circuit, cascade single stage distributed amplifier, feedback circuit or loss

matched circuit in order to compensate for the variations of frequency [6].

The Cascade Single Stage Distributed Amplifier (CSSDA) was one of the broadband amplifier techniques based on Traveling Wave Amplifier, which had been employed for the broadband systems as it was being firmly established, reliable and robust devices that can be realized in MMIC and UWB technologies. In this project this broadband amplifier had been chosen and designed using Advanced Design System 2004A (ADS 2004A) due to the excellent bandwidth performance, low noise figure and also its popularity. This is because the input and output capacitances of the active devices are absorbed in the distributed structures. As a result, the amplifier can exhibit very low sensitivities in process variations during designing and simulation.

As the first stage of the receiver, LNAs are required to have high gain and low Noise Figure (NF). Many implementations of narrow band LNAs are understood background study. From the perspective of a basic two-port, it can be shown that the optimum driving source susceptance for minimum NF is inductive in character, but has a capacitive variation. Furthermore, the optimum driving conductance should vary linearly with frequency. Achieving such a noise match, together with a good source impedance termination is especially difficult for wide-band systems as it involves synthesizing a network that provides these characteristics over a large frequency range.

Recently, several innovative wide-band LNA architectures have been proposed to take on this challenge. In this work, Cascade Single Stage Distributed amplifier (CSSDA) for broadband amplifier was introduced to replace the conventional distributed amplifier that suffered from relatively high power consumption. This work focuses on the design and analysis of CSSDA with emphasis on low power. The understandings the high gain, low noise figure and bandwidth of a CSSDA are discussed in detail in this report.

1.2 Problem Statement

In general, the RF performance of the Low Noise Amplifier is very good as it is able to achieve the required gain and provides low noise figure. But designing of the only single stage amplifier, the high gain, low noise figure and the stability of the amplifier cannot be achieved as we needed. Low Noise Amplifier usually implies RF/wireless applications. But noise is also a critical consideration for lower frequency analog applications.

In order to avoid this, the developing of amplifier based on Cascade Single Stage Distributed Amplifier (CSSDA) will solve the problem above. The reason why the devices are connected in cascade is so that the signal power injected at matched input port is coupled and amplified by Transconductance G_m of each device before at the end of the matched output is terminated. The concept of CSSDA was discussed in Chapter II. To select an appropriate amplifier, it is necessary to understand the noise parameters for a particular application and then determine whether the amplifier is indeed low noise.

1.3 Objectives

Ultrawideband Low Noise Amplifier (LNA) is an integrated component of most RF systems. The main purpose of this report is to document the learning process involved in the design and testing of a broadband amplifier for operating frequencies between 3 GHz and 10 GHz.

The objectives of this Ultrawideband amplifier design are to understand the concept of UWB communication and RF amplifier system, to know the difference between narrow band amplifier and broadband amplifier, to design a broadband Low Noise Amplifier based on CSSDA techniques and to design a Low Noise Amplifier that can operate in UWB frequency that is between 3 GHz -10 GHz.

The design will use transistor FPD6836PP70 that is manufactured by Filtonic Semiconductor. This project involves familiarization and utilization of a RF CAD tool, Advanced Design System ADS2004A.

1.4 Scope of Work

The scope of work involves with circuit level design of Low Noise Amplifier. The selection of transistor is studied to ensure all the specification requirements are meet. The computer aided design (CAD) tools are used to design and simulate UWB amplifier.

The design process is started with single stage design for single frequency. The second method is designing two stages and three stages of the low amplifier by cascading each stage at different frequency. Then, the forward gain, reverse gain, noise figure, matching network and stability discussed and analyzed.

1.5 Methodology

This project will start with background study of UWB communication system, LNA design and CSSDA concept. This is done by find out all the journal, articles and books that related to this project either in website or any materials. After understanding all concepts which is relating, the study of software is done. In this project, designing and simulation any circuit are done by using ADS2004A as CAD tools software. Then the calculation of single stage amplifier with using the appropriate formulas needs to be done. Next, simulate single stage amplifier design with using CAD tool. Then, stage design of the amplifier based on CSSDA. It also has two process that is, calculation and simulation. After all the designing process is done, the circuit then discussed and analyzed as in Chapter IV.